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Extending Operation of Free-Running Oscillator (FRO-250M)

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Document Information

Information	Content
Keywords	Free-Running Oscillator, FRO-250M, Performance Enhancement, Battery powered applications, i.MX RT500, RT595, RT500, MIMXRT595, i.MXRT595
Abstract	This document describes how the FRO-250M functionality is enabled and available to users to enhance the performance of battery powered applications.

1 Introduction

The i.MX RT500 family of MCUs offers a rich set of peripherals and very low power consumption for applications, such as, battery powered applications. The Free-Running Oscillator (FRO) is widely used in these applications because it helps to extend battery life as it consumes much less power than using the PLL.

With user demand requiring longer battery life for their applications and simultaneously increasing performance, the performance of the FRO has been extended from operating at a maximum of 192 MHz up to 250 MHz. It greatly opens up opportunities for applications that require higher performance while still meeting low power consumption requirements.

This document describes how the FRO-250M functionality is enabled and available to users.

2 FRO-250M frequency increase

Characterization was conducted to extend the frequency of the FRO. The standard reliability and qualification processes of NXP were utilized to ensure quality. This enhancement is made as a running change of existing product, meaning that any RT500 device can support this higher frequency.

The *i.MX RT500 Low-Power Crossover Processor* (document IMXRT500EC) includes the specification for the FRO-250M. Table 1 outlines the updated parameter values. For the latest specifications, see the data sheet.

Table 1. FRO-250M specifications [1]

Symbol	Characteristic	Min.	Typ.[2]	Max.	Unit
$f_{fro250m}$	FRO-250M frequency (nominal)		250		MHz
$\Delta f_{fro250m}$	• User trim close loop (Closed loop) using accurate `clk src`	—	—	±1	%
$t_{startup}$	Startup time	—	58	—	µs
jit_{cyc}	Cycle to cycle jitter	—	90	—	ps
$I_{fro250m}$	Current consumption (VDDCORE)	—	68	—	µA
$I_{fro250m}$	Current consumption (VDD1V8)	—	171	—	µA
V_{min}	Minimum voltage	0.85	—	—	V

[1] FBB is enabled. The logic in VDDCORE domain may require higher VDDCORE voltage to be clocked at 250 MHz. FRO divider options 2/4/8 can be used to reduce the FRO frequency to the VDDCORE logic. For specific Max. Freq vs VDDCORE limits, see Table 2.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Note: *Any divided versions of the FRO that are not being used anywhere should be turned off to save power.*

To minimize the power consumption of an application for a given frequency, set the supply voltage to the minimum voltage (V_{min}) for that maximum frequency (F_{max}). Table 2 in the *i.MX RT500 Low-Power Crossover Processor* (document IMXRT500EC) outlines these specifications for VDDCORE, the core supply voltage.

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Table 2. General operating conditions

Symbol	Parameter	Conditions	Min.	Type	Max.	Unit
VDDCORE	Core supply voltage. On-chip regulator not used. LDO_ENABLE=0. Power supplied by an off-chip Power Management IC (PMIC).	Retention mode	0.58	0.6	—	V
		Active Mode (M33/DSP Max. Freq = 60 MHz, FBB)	0.7	—	—	V
		Active Mode (M33/DSP/GPU Max. Freq = 100 MHz, FBB)	0.8	—	—	V
		Active Mode (M33/DSP/GPU Max. Freq = 192 MHz, FBB)	0.9	—	—	V
		Active Mode (M33/DSP/GPU Max. Freq = 230 MHz, FBB)	1.0	—	—	V
		Active Mode (M33/DSP/GPU Max. Freq = 250 MHz, FBB)	1.02	—	—	V
		Active Mode (M33/DSP/GPU Max. Freq = 275 MHz, FBB)	1.1	—	—	V

Table 2 applies to the PLL and FRO clock sources. In particular, we want to focus on the FRO where it shows that to drive a `main_clk` of 250 MHz a VDDCORE V_{min} of 1.02 V is required to meet this F_{max} across process, voltage, and temperature. For details of the RT500 clock tree, see **Section 6.1.4 Clock block diagram** in the *i.MX RT500 Low-Power Crossover MCU Reference Manual* (document IMXRT500RM).

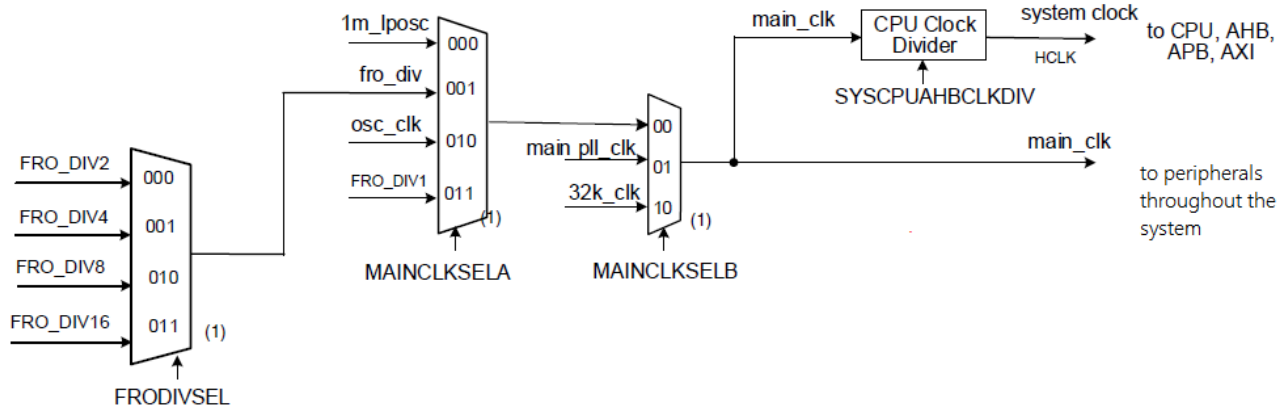

Figure 1. RT500 clock diagram

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3 FRO-250M enablement

The enablement for the FRO-250M is available in an FRO Tuning Function via MCUXpresso SDK 2.13.0 or later for the RT500 EVK. This function employs a closed-loop user trim technique using an accurate clock source.

For example, the function `CLOCK_FroTuneToFreq` (250000000) uses the FRO Tuner, and a hardware block that can tune the FRO with either the main crystal oscillator or the CLKIN function as the source for the internal `osc_clk` signal. For more details of the FRO Tuner, refer to **Section 6.4.1 FRO Tuner** in the *i.MX RT500 Low-Power Crossover MCU Reference Manual* (document IMXRT500RM).

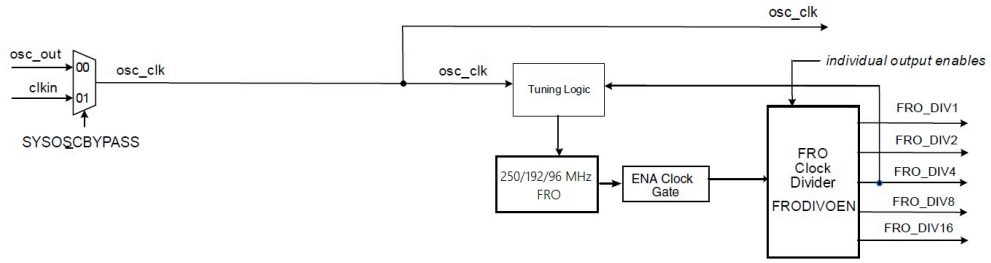

Figure 2. FRO tuner

The function resides in the *fsl_clock.c* driver:

- `status_t` **`CLOCK_FroTuneToFreq`**`(uint32_t targetFreq)`

This function can be used in an application to retrim the default FRO-192M to operate at 250 MHz allowing the user the ability to expand the capabilities of the internal FRO.

In order to do this, the

`#define CLK_FRO_HIGH_FREQ 192000000u /*High Frequency of Clock*/` found in the header file *system_MIMXRT595S_cm33.h* should be changed to `250000000u`.

4 Other considerations

The VDDCORE V_{min} required is not always limited by the frequency of `main_clk`. The data sheet also has restrictions on VDDCORE for specific peripherals, features, or use-cases of the MCU. The following items outline some additional limitations to consider, and provides some details from the data sheet. If there are multiple VDDCORE `Vmin` requirements in the data sheet that apply, the highest minimum must be used:

- FRO has `Vmin` VDDCORE requirements based on the trim frequency and dividers used.
- FlexSPI and SDHC have requirements based on the clock frequencies to these peripherals or their external memories.
- OTP fuses require a high VDDCORE voltage for reads.
- `MIPI_DSI_VDD11` is a power supply pin that requires at least 0.85 V when using the MIPI-DSI for a display. Although this pin is a separate power supply than VDDCORE, board designs typically short `MIPI_DSI_VDD11` to VDDCORE, as done on the RT500 EVK.

For further details of additional requirements for the above items and for those not outlined above, see the *i.MX RT500 Low-Power Crossover Processor* (document IMXRT500EC).

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5 Revision history

Table 3 summarizes the revisions to this document.

Table 3. Revision history

Revision number	Date	Substantive changes
0	14 June 2023	Initial release

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