

i.MX31 to i.MX35 Porting Guide

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This application note explains the main differences between the i.MX31 and the i.MX35 processors. This document helps the reader to identify the improvements, and also the new features available on the i.MX35. The migration from the i.MX31 processor is easily done, and detailed information for the new implementation with the i.MX35 processor is also available in this application note.

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1 i.MX31 Overview

The i.MX31 and i.MX31L multimedia application processors represent the next step in the low power, high performance application processors.

The i.MX31L does not include the Graphics Processing Unit (GPU).

Based on the ARM11 microprocessor core, the i.MX31 operates on low power, which is required for modern digital devices. The i.MX31 takes advantage of the ARM1136JF-S™ core running at 532 MHz, and is optimized for minimal power consumption using the most advanced techniques for power saving (DPTC, DVFS, power gating and clock gating).

With 90 nm technology and dual-Vt transistors (two threshold voltages), the i.MX31 provides the optimal performance versus leakage current balance.

The performance of the i.MX31 is boosted by a multi-level cache system. It supports the peripheral devices such as MPEG-4 Hardware Encoder (VGA, 30 fps), an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based SDMA controller.

The i.MX31 supports connections to various types of external memories which include DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The i.MX31 is also connected to a variety of external devices using technologies such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 i.MX31 Features

The features of the i.MX31 processor are as follows:

- 1-Wire Interface—Provides bidirectional communication between the ARM11 core and the external 1-Wire devices.
- Advanced Technology (AT) Attachment—An AT attachment host interface designed to interface with the IDE hard disk drives and the ATAPI optical disk drives.
- Digital Audio Multiplexer (AUDMUX)—Allows multiple, simultaneous audio or voice or data flows between the ports, in point-to-point or point-to-multipoint configurations.
- Clock Amplifier Module (CAMP)—Converts a square wave or a sinusoidal input into a rail-to-rail square wave. The output of CAMP is then fed to the pre divider.
- Clock Control Module (CCM)—Provides the clock, reset, and power management control for the i.MX31 processor.
- Configurable Serial Peripheral Interface (CSPI) (x 3)—Equipped with the data FIFOs. It is a master or slave configurable serial peripheral interface module, capable of interfacing to both the SPI master and slave devices.
- Digital Phase Lock Loop (DPLLs)—Produces high frequency on-chip clocks with low frequency and phase jitters.

NOTE

External clock sources provide the reference frequencies.

- Embedded Cross Trigger (ECT)—Composed of three CTIs (Cross Trigger Interface) and one CTM (Cross Trigger Matrix-key) in the multi-core and multi-peripheral debug strategy.
- External Memory Interface (EMI)—Includes the following:
 - Multi-Master Memory Interface (M3IF)
 - Enhanced SDRAM Controller (ESDCTL)
 - NAND Flash Controller (NFC)
 - Wireless External Interface Module (WEIM)
- Enhanced Periodic Interrupt Timer (EPIT)—A 32-bit set and forget timer, which starts counting after the EPIT is enabled by the software. It is capable of providing precise interrupts at regular intervals, with minimal processor intervention.

- Embedded Trace Macrocell (ETM)—Supports real-time instructions and data tracing, through the ETM auxiliary I/O port.
- Fast InfraRed Interface (FIR)—Capable of establishing a 0.576 Mbit per second, 1.152 Mbit per second or 4 Mbit per second half duplex link, through a LED and IR detector. It supports 0.576 Mbit per second and 1.152 Mbit per second Medium InfraRed (MIR) physical layer protocol. Also, it supports 4Mbit per second Fast InfraRed (FIR) physical layer protocol, defined by *IrDA, Rev. 1.4*.
- Fusebox—A ROM, that is factory configured by Freescale.
- General Purpose I/O Module (GPIO)—Provides several groups of 32-bit bidirectional, general purpose I/O. This peripheral provides dedicated general purpose signals, that can be configured as either inputs or outputs.
- General Purpose Timer (GPT)—A multipurpose module used to measure intervals or generate periodic output.
- Graphics Processing Unit (GPU)—Provides hardware acceleration for 2D and 3D graphics algorithms.
- Inter IC Communication (I²C)—Provides serial interface for controlling the Sensor Interface and other external devices. Data rates up to 100 Kbits per second are supported.
- IC Identification Module (IIM)—Provides an interface for reading the device identification.
- Image Processing Unit (IPU)—Processes video and graphics functions in the i.MX31 and provides interfaces to video, still image sensors, and displays.
- Keypad Port (KPP)—Either used for keypad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix.
- MPEG-4 Video Encoder (MPEG-4)—Accelerates video compression, by following the MPEG-4 standard.
- Memory Stick Host Controller (MSHC)—Placed in between the AIPS and the customer memory stick to support data transfer from the i.MX31 to the customer memory stick.
- Pads I/O (PADIO)—Serves as an interface between the internal modules and the external connections of the devices.
- PCM—PCMCIA host adapter provides the control logic for PCMCIA socket interfaces.
- Pulse-Width Modulator (PWM)—Has a 16-bit counter and is optimized to generate sounds from the stored sample audio images. It is also capable of generating tones.
- Random Number Generator Accelerator (RNGA)—A digital integrated circuit, capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards, for randomness and non-determinism.
- Real Time Clock (RTC)—Provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming and the RTC supports dates from the year, 1980 to 2050.
- Run-Time Integrity Checkers (RTIC)—Ensures the integrity of the peripheral memory contents and assists them with boot authentication.

- Security Controller Module (SCC)—A hardware component composed of two blocks: the Secure RAM module, and the Security Monitor. The Secure RAM module stores the sensitive information in a very secured manner.
- Secured Digital Host Controller (SDHC)—Controls the MMC (Multi-MediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to these cards and also performs data accesses to and from the cards.
- Smart Direct Memory Access (SDMA)—Maximizes the system's performance, by relieving the ARM core of bulk data transfer from memory to memory, or between memory and on-chip peripherals.
- Subscriber Identification Module (SIM)—Provides an interface to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication, and it is mainly used for e-commerce applications.
- Secure JTAG Controller (SJC)—Provides debug and test control with maximum security. It also provides a flexible architecture for future derivatives or future multi-core architectures.
- Synchronous Serial Interface (SSI)—A full-duplex serial port, that allows the device to communicate with a variety of serial devices, such as standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs, that implement the Inter-IC Sound bus standard (I²S) and Intel AC97 standard.
- Universal Asynchronous Receiver/Transmitter (UART)—provides serial communication capability with external devices, through an RS-232 cable (or) through the use of external circuitry, that converts infrared signals to electrical signals (for reception) (or) transforms electrical signals to signals, that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.
- Universal Serial Bus—Two Host Controllers and one OTG (On-The-Go):
 - USB Host 1 is designed to support, transceiver less connection to the on-board peripherals in Low Speed (LS) and Full Speed (FS) mode, and connection to the ULPI (UTMI + Low-Pin Count) and Legacy Full Speed transceivers.
 - USB Host 2 is designed to support transceiver less connection to the Cellular Modem Baseband Processor.
 - The USB-OTG controller offers HS or FS or LS capabilities in Host mode, and HS or FS in device mode. In Host mode, the controller supports direct connection to a FS or LS device (without external hub). In device (bypass) mode, the OTG port, functions as gateway between the Host 1 Port and the OTG transceiver.
- Watchdog Timer Module (WDOG)—Helps to protect against system failures, by providing a method for the system, to recover from unexpected events or programming errors.

1.1.1 i.MX31 Simplified Block Diagram

NOTE

There are no silicon differences between the revisions 2.0 and 2.0.1. The main difference is that, there is an updated iROM code which supports USB-HS, SD/MMC boot modes and corrects some boot mode related erratas.

Figure 1 shows the i.MX31 simplified block diagram.

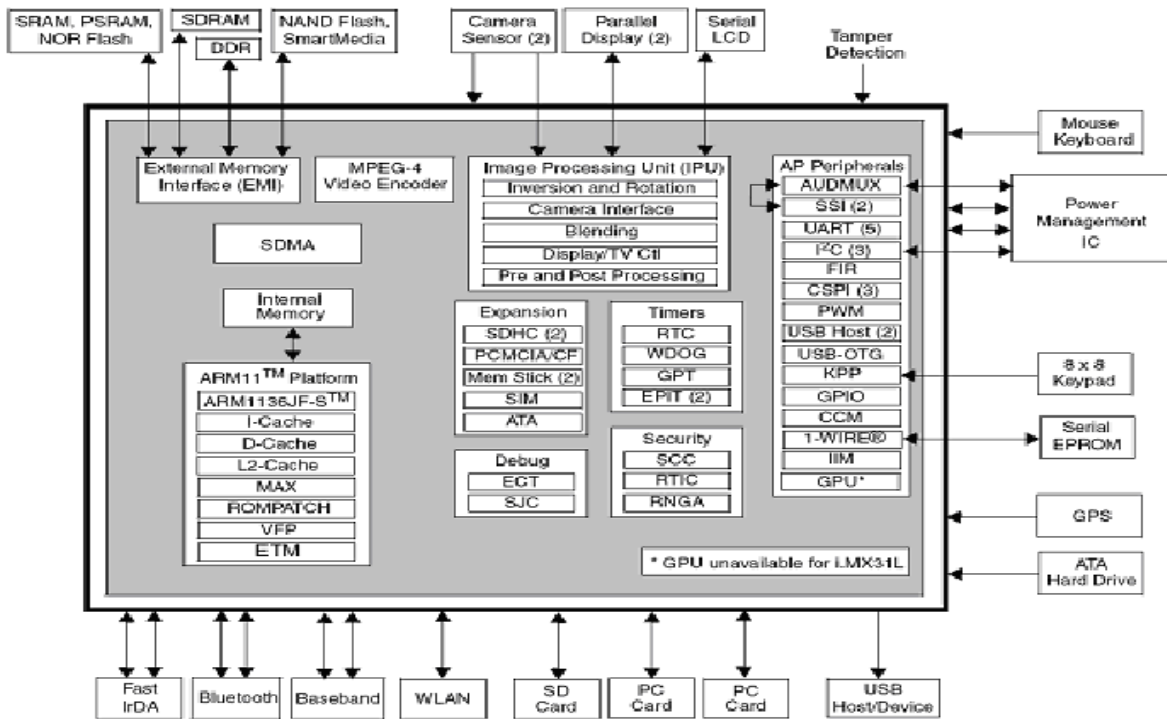


Figure 1. i.MX31 Block Diagram

2 i.MX35 Overview

2.1 i.MX35 Automotive Introduction

The i.MX35 auto application processor family is designed for automotive infotainment, and navigation applications. They are AECQ100 Grade 3 qualified, and rated for ambient operating temperatures up to 85° C. The i.MX35 multimedia application processor, represents the next step in low power, high performance application processors.

Based on an ARM11 microprocessor core running at 532 MHz, the device offers specific features, and optimized system cost, for the following target applications:

- Audio Connectivity and Telematics
 - Compressed audio playback from storage devices (CD, USB, HDD or SD card)
 - PlayFromDevice (1-wire and 2-wire support) for portable media players
 - iPod or iPhone control and playback
 - High-speed CD ripping to USB, SD or MMC or HDD for virtual CD changer
 - Audio processing for hands-free telephony: Bluetooth, AEC or NS, Microphone beam forming.
 - Speech recognition
- A/V Connectivity and Navigation
 - Includes audio connectivity and telematics features
 - Map display and route calculation
 - QVGA video decode and WVGA video display
 - Sophisticated graphical user interface

The i.MX35 processor takes advantage of the ARM1136JF-S™ core running at 532 MHz, which is boosted by a multi-level cache system. It also features peripheral devices such as, an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based DMA controller. The i.MX35 supports connections to various types of external memories, such as SDRAM, Mobile DDR and DDR2, SLC and MLC NAND Flash, NOR Flash, and SRAM. It is also possible to connect the device to a variety of external devices such as High-speed USB2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

2.2 i.MX35 Automotive Features

The automotive features of the i.MX35 processor are as follows:

- 1-Wire Interface—Provides the communication line to a 1-KBit Add-Only Memory and it sends or receives 1 bit at a time.
- Asynchronous Sample Rate Converter (ASRC)—Designed to convert the sampling rate of a signal associated to an input clock, into a signal associated to a different output clock. It supports a concurrent sample rate conversion of about -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates.
- ATA Module—An AT attachment host interface used to interface with IDE hard disk drives and ATAPI optical disk drives. It also interfaces with the ATA device over a number of ATA signals.
- Digital Audio Multiplexer (AUDMUX)—A programmable interconnect for voice, audio, and synchronous data routing between the host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
- CAN Module (x2)—Primarily designed to be used as a vehicle serial data bus, running at 1 Mbits per second.
- Clock Control Module (CCM)—Generates all clocks for the peripherals in the SDMA platform. The CCM also manages the ARM1136 platform low-power modes (WAIT, STOP), disables

peripheral clocks appropriately for power conservation, and provides alternate clock sources for the ARM1136 and SDMA platforms.

- Configurable Serial Peripheral Interface (CSPI) (x2)—A serial interface, equipped with data FIFOs. Each master or slave configurable SPI module is capable of interfacing to both serial port interface - master and slave devices. The CSPI Ready (SPI_RDY) and Slave Select (SS) control signals, enable fast data communication with fewer software interrupts.
- Embedded Cross Trigger (ECT)—An IP for real-time debug purposes. It is a programmable matrix, which allows several subsystems to interact with each other. ECT receives signals required for debugging purposes (from cores, peripherals, buses, external inputs, and so on) and propagates them (propagation programmed through software) to the different debug resources, available within the SoC.
- External Memory Interface (EMI)—Provides access to external memory, for the ARM and other masters. It is composed of the following main sub modules:
 - M3IF: Provides arbitration between the multiple masters, requesting access to the external memory.
 - SDRAM CTRL: Provides an interface to mDDR, DDR2 (4-bank architecture type), and SDR interfaces.
 - NANDFC: Provides an interface to NAND Flash memories.
 - WEIM: Provides an interface to NOR Flash and PSRAM.
- Enhanced Periodic Interrupt Timer (EPIT) (x2)—A 32-bit set and forget timer, that starts counting after the EPIT is enabled by the software. It is capable of providing precise interrupts at regular intervals, with minimal processor intervention. It has a 12-bit pre scaler to adjust the input clock frequency to the required time setting for the interrupts, and it also allows the counter value to be programmed on the fly.
- Enhanced Serial Audio Interface (ESAI)—Provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, with each section having its own clock generator.
- Enhanced Secure Digital Host Controller (eSDHC) (x3)—Consists of four main modules: CE-ATA, MMC, SD and SDIO.
 - CE-ATA: Hard drive interface, that is optimized for embedded applications of storage.
 - MMC: The Multi-Media Card (MMC) is a universal, low cost, data storage, and communication media, to applications such as electronic toys, organizers, PDAs, and smart phones.
 - SD: The Secure Digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements, which is inherent in emerging the audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables copyright protection mechanism, that complies with the SDMI security standard.
 - SDIO: Provides high speed data I/O (such as wireless LAN through SDIO interface) with low power consumption.

NOTE

CE-ATA module is not available for the i.MX351 processor.

- Ethernet Media Access Controller (MAC)—Designed to support both 10 and 100 Mbits per second Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver functions are required to complete the interface to the media.
- General Purpose I/O modules (GPIO) (x3)—Used for general purpose input or output to external ICs. Each GPIO module supports 32-bits of I/O.
- General Purpose Timers (GPT)—A 32-bit free running or set and forget timer, with a programmable pre scaler, and compare and capture registers. A timer counter value is captured using an external event, and is configured to trigger a capture event, on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set and forget mode, it is capable of providing precise interrupts at regular intervals, with minimal processor intervention. The counter has an output compare logic, to provide the status and interrupt at comparison. This timer is also configured to run on, either an external clock or an internal clock.
- Graphics Processing Unit 2Dv1 (GPU)—Accelerates the OpenVG and GDI graphics.

NOTE

The GPU module is not available for the i.MX351 processor.

- Inter-Integrated Circuit (I²C) (x3)—An industry-standard, bidirectional serial bus, that provides a simple and efficient method for data exchange, minimizing the interconnection between devices. I²C is suitable for applications which requires, occasional communication over a short distance, among many devices. The interface operates at 100 kbps, with maximum bus loading and timing. The I²C system is a true multiple-master bus, with arbitration and collision detection, that prevents data corruption, if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multi-processor control, and is used for rapid testing, and alignment of end products, through external connections to an assembly-line computer.
- IC Identification Module (IIM)—Provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals, requiring a fixed value.
- External Signals and Pin Multiplexing—Provides a flexible, scalable multiplexing solution with the following features: Up to eight output sources multiplexed per pin, up to four destinations for each input pin, and unselected input paths held at constant levels, for reduced power consumption.
- Image Processing Unit (IPU)—Supports video and graphics processing functions. It also provides the interface for image sensors and displays.

The IPU performs the following main functions:

- Pre processing of data from the sensor or from the external system memory
- Post processing of data from the external system memory
- Post filtering of data from the system memory, with the support of MPEG-4 and H.264 post filtering algorithms
- Displaying video and graphics on a synchronous (dumb or memory less) display
- Displaying video and graphics on an asynchronous (smart) display

- Transferring data between the IPU sub modules and to/from the system memory, with flexible pixel reformatting
- Keypad port—Used either for the keypad matrix scanning or general purpose I/O.
- Media Local Bus (MLB)—Designed to interface with an automotive MOST ring.
- OSC Audio Reference Oscillator (OSCAUDIO)—The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576 MHz crystal.
- OSC24M-24-MHz Reference Oscillator—The signal from the external 24 MHz crystal is the source for the CLK24M signal, which is fed into USB PHY as the reference clock, and to the Real Time Clock (RTC).
- Digital Phase-Locked Loops—Used to generate the clocks: MCU PLL (MPLL) - programmable and Peripheral PLL (PPLL) - programmable.

2.2.1 i.MX35 Automotive Ordering Information Simplified Block Diagram

See *i.MX35 Multimedia Applications Processor for Automotive Products Data Sheet* (MCIMX35SR2AEC) for information on the automotive version ordering, package, and operating temperature.

Figure 2 shows the i.MX35 automotive simplified block diagram.

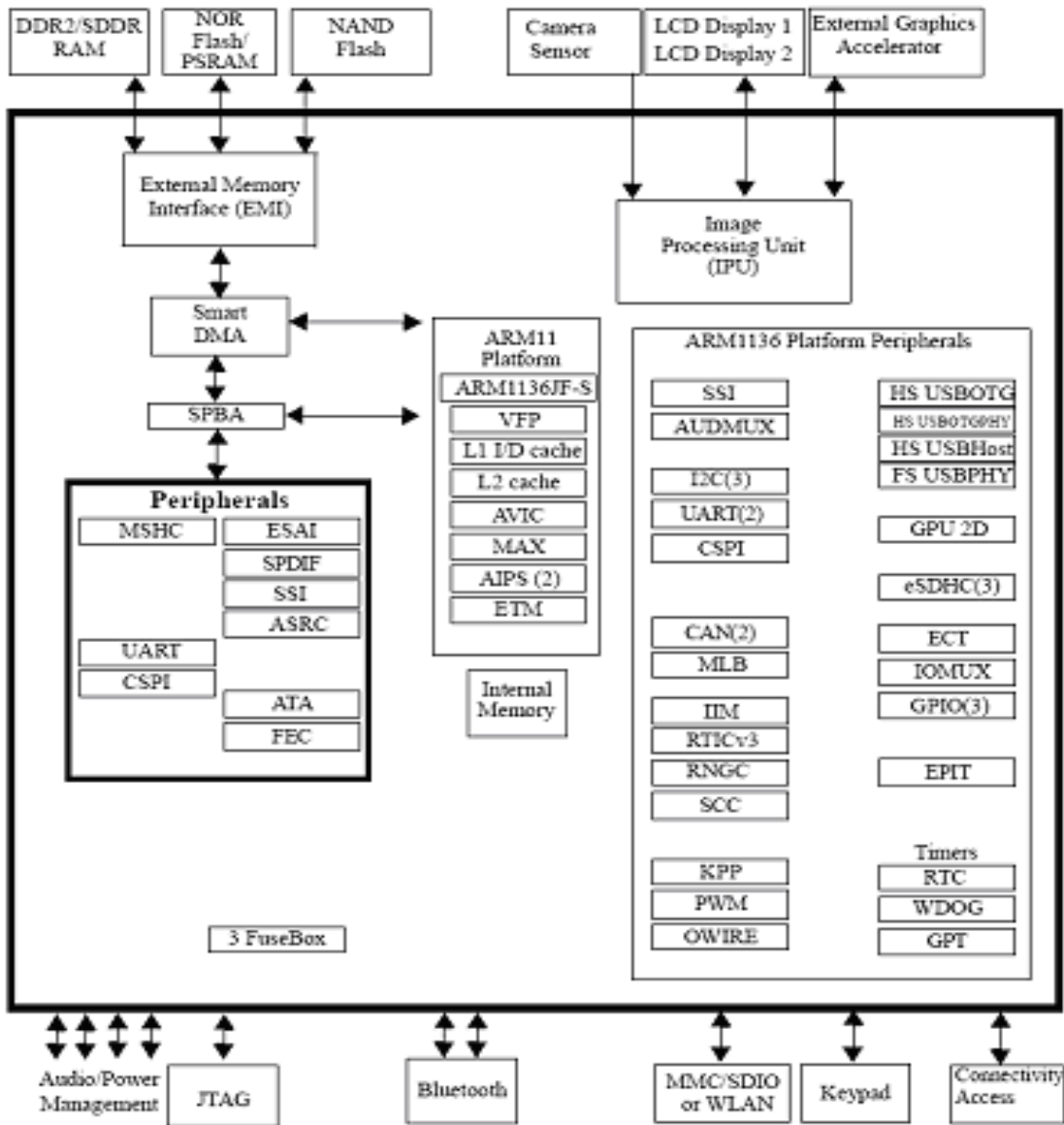


Figure 2. i.MX35 Automotive Simplified Block Diagram

2.3 i.MX35 Consumer Features

The i.MX353 and the i.MX357 multimedia application processors represent the next generation of ARM11 products, with the right performance and integration, to address applications within the industrial and consumer markets, for applications such as HMI and display controllers.

Unless specified, the information in the data sheet is applicable to both the i.MX353 and i.MX357 devices, and throughout this application note, it is referred singularly as i.MX35. The i.MX353 devices do not include a Graphics Processing Unit (GPU). For information on i.MX35 devices - automotive applications, refer to the document number *i.MX35 Multimedia Applications Processors for Industrial and Consumer*

Products Data Sheet (MCIMX35SR2CEC). The i.MX35 processor takes advantage of the ARM1136JF-S™ core running at 532 MHz, which is boosted by a multi-level cache system and integrated features, which includes LCD controller, Ethernet, and graphics acceleration for creating rich user interfaces.

The i.MX35 supports connections to various types of external memories, such as SDRAM, mobile DDR and DDR2, SLC and MLC NAND Flash, NOR Flash, and SRAM. The devices are connected to a variety of external devices, which includes USB 2.0 OTG, ATA, MMC or SDIO, and Compact Flash.

Generally, the consumer version has the same features as that of the auto version, but the MLB and automotive grade certification differs.

2.3.1 i.MX35 Consumer Ordering Information Simplified Block Diagram

See *i.MX35 Multimedia Applications Processors for Industrial and Consumer Products Data Sheet* (MCIMX35SR2CEC) for information on the consumer version ordering, package, and operating temperature.

Figure 3 shows the i.MX35 consumer simplified block diagram.

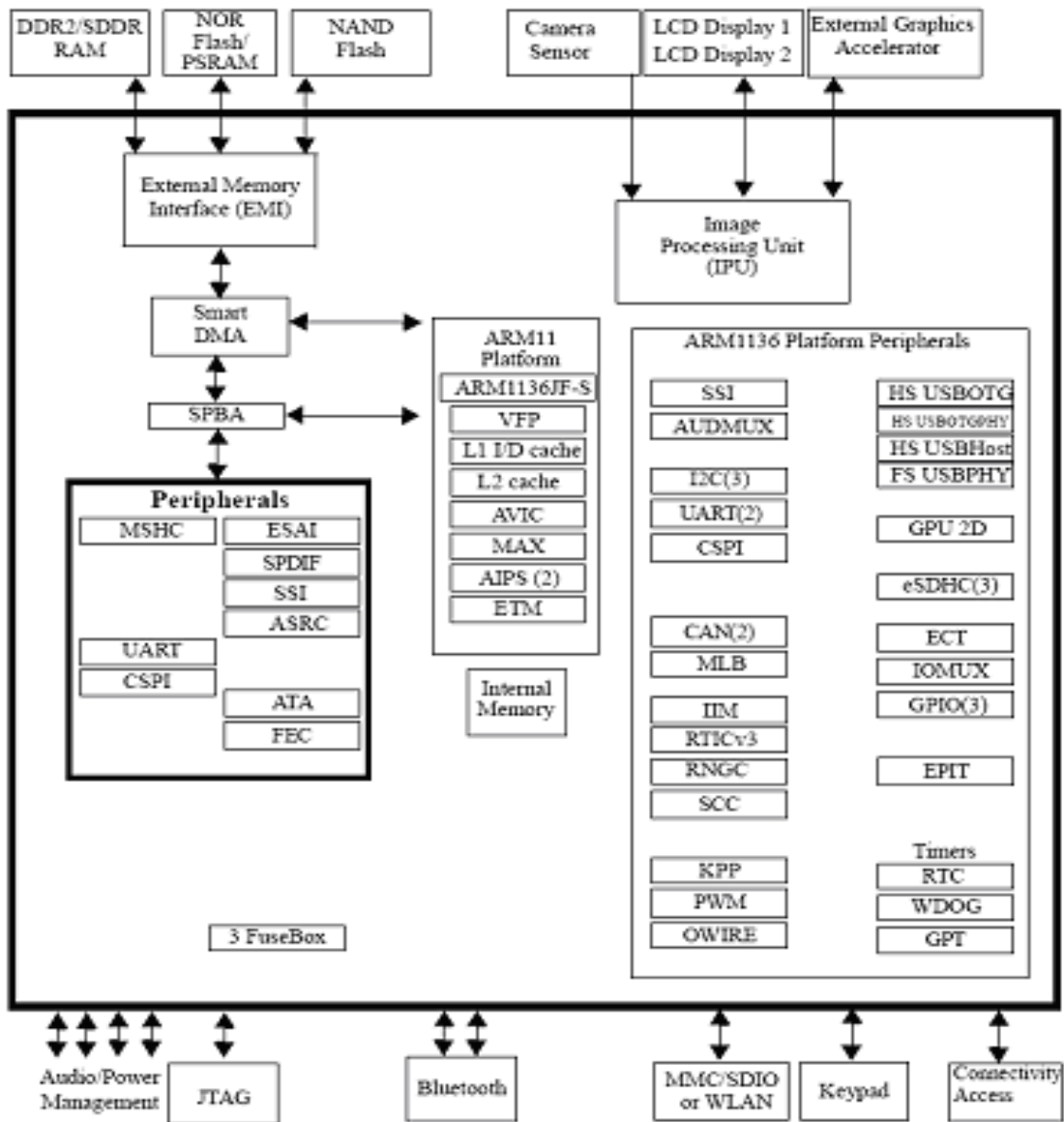


Figure 3. i.MX35 Consumer Simplified Block Diagram

2.4 i.MX35 Family Differences

Table 1 shows the differences between the various i.MX35 processor family.

Table 1. i.MX35 Family Differences

| Feature | i.MX351 | i.MX353 | i.MX355 | i.MX356 | i.MX357 |
|-----------------------------|--|---|---|---|--|
| Target Markets | Automotive | Consumer and Industrial | Automotive | Automotive | Consumer and Industrial |
| Example Applications | <ul style="list-style-type: none"> • Automotive Audio • Audio Connectivity | <ul style="list-style-type: none"> • HMI <ul style="list-style-type: none"> – Factory Automation – Building Control – Home Displays – Medical | <ul style="list-style-type: none"> • Automotive Audio • Audio Connectivity • Automotive Infotainment • Navigation • Speech Recognition | <ul style="list-style-type: none"> • Automotive Audio • Audio Connectivity • Automotive Infotainment • Navigation • Speech Recognition • Flash Accelerated UI | <ul style="list-style-type: none"> • PND • HMI • Factory Automation • Building Control • Home Displays • Medical |
| Core | ARM11™ | ARM11™ | ARM11™ | ARM11™ | ARM11™ |
| CPU Speed | 532 MHz | 532 MHz | 532 MHz | 532 MHz | 532 MHz |
| L1 I/D Cache | 16 K I/D | 16 K I/D | 16 K I/D | 16 K I/D | 16 K I/D |
| L2 Cache | 128 KB | 128 KB | 128 KB | 128 KB | 128 KB |
| OpenVG 1.1 | — | — | — | Y | Y |
| LCD Controller | — | Y | Y | Y | Y |
| Ethernet | 1-10/100 | 1-10/100 | 1-10/100 | 1-10/100 | 1-10/100 |
| CAN | 2 | 2 | 2 | 2 | 2 |
| USB + PHY | HS OTG HS Host | HS OTG HS Host | HS OTG HS Host | HS OTG HS Host | HS OTG HS Host |
| I2C | 3 | 3 | 3 | 3 | 3 |
| MLB | Y | — | Y | Y | — |
| SSI/I2S | 2 | 2 | 2 | 2 | 2 |
| SD/SDIO/MMC | 2 | 2 | 2 | 2 | 2 |
| SPI | 2 | 2 | 2 | 2 | 2 |
| UART | 3 | 3 | 3 | 3 | 3 |
| PATA/CEATA | -/- | Y/Y | Y/Y | Y/Y | Y/Y |

Table 1. i.MX35 Family Differences (continued)

| Feature | i.MX351 | i.MX353 | i.MX355 | i.MX356 | i.MX357 |
|-------------|-----------------------------|---------|---------|---------|---------|
| Package | 17 ×17 BGA 0.8mm 400 ball | | | | |
| Speed | 532 MHz @ -20 +70 C | | | | |
| Temperature | 400 MHz/532 MHz @ -40 +85 C | | | | |

1 The empty cells in the table indicate the features that are missing within each i.MX35 family.

3 i.MX31 versus i.MX35

This section displays the list of those features which differs between the i.MX31 and i.MX35 processors. It also includes improvements functionality, that has been removed.

3.1 i.MX35 Additional Supported Features over i.MX31

The additional supported features of the i.MX35 processor over the i.MX31 processor are as follows:

- More embedded SRAM (128 KB instead 16 KB)
- LPDDR and DDR2
- Open VG1.1 GPU (only for i.MX356 and i.MX357)
- Two CAN Channels
- One CE-ATA
- i.MX35 MLB for Auto versions (i.MX35-1-5-6)
- Fast Ethernet Controller (FEC)
- Enhanced Serial Audio Interface (ESAI)
- Sony or Philips Digital Transceiver Interface (S or PDIF)
- Smart, serial and parallel panels, TV output (can interface to an external TV encoder), parallel display (primary up to 24-bit, resolution SVGA 800x600)
- One USB 2.0 host with ULPI interface, or internal full speed PHY. Up to 480 Mbits per second, if external HS PHY is used
- One USB 2.0 OTG (up to 480 Mbits per second) controller with internal high speed OTG PHY
- Booting from MMC or SD and Serial or SPI
- One additional SDIO port (shared with memory stick)
- ASRC (Asynchronous Sample Rate Converter)
- Added support for MLC NAND Flash

3.2 i.MX31 Features not Supported on i.MX35

The features of the i.MX31 processor that are not supported on i.MX35 processor are as follows:

- i.MX35 with only three UART's versus i.MX31 with five

- i.MX35 with only two CSPI's versus i.MX31 with three
- i.MX35 does not support Fast IrDA module
- i.MX35 does not support Subscriber Interface Module
- i.MX35 does not support PCMCIA or Compact Flash
- No OpenGL ES 1.0 GPU
- No MPEG4 video encoder
- One fewer FS USB Host controller

4 Porting an Application from i.MX31 to i.MX35

4.1 Hardware and Software Concepts

In order to have a smooth migration from an i.MX31 application to an i.MX35, the hardware and software issues listed in the following sections should be considered.

4.2 Hardware Issues

The hardware issues to be considered are as follows:

- Define if automotive grade is really required
- Increased embedded SRAM is used to improve low power audio playback or similar applications (keeping critical routines running from internal memory)
- Mobile DDR and DDR2 (four banks and without ODT) are available
- Audio solution is improved with the addition of ESAI, ASRC, and S or PDIF modules
- Ethernet connectivity is available
- With new features available in OpenVG 1.1, graphic processing solution is improved
- USB transceiver is removed, since the internal PHY solution is available
- Power requirements have changed
- There is no MBX module for i.MX35

4.3 Software Issues

The software issues to be considered are as follows:

- Eventhough, several register locations and bit definitions are consistent between i.MX31 and i.MX35, one has to be cautious and check for changes in the registers, if any
- New modules and their drives are available
- New Booting options
- No support for OpenGL and Direct3D

5 Revision History

Table 2 provides a revision history for this application note.

Table 2. Document Revision History

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|-----------------------|
| 0 | 03/2010 | Initial release |

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