i.MX35 Memories
SCL and MCL NAND Flash, SDRAM (SDR, mDDR, DDR2, MMC/SDIO, SRAM, USB2.0 OTG, and ATA)

by   *Multimedia Applications Division*
       Freescale Semiconductor, Inc.
       Austin, TX

This application note describes the different memories available for the i.MX35 family. The i.MX35 offers several memories, that are flexible tools for implementing multimedia applications.

The i.MX35 supports connections to various types of external memories, such as:

- Synchronous dynamic random access memory (SDRAM)
- Mobile double data rate (DDR) and DDR2
- Single-level cell (SLC) and multi-level cell (MLC)
- NAND Flash
- NOR Flash
- Static random access memory (SRAM)

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The device can be connected to various external devices such as high-speed USB2.0 on-the-go (OTG), advanced technology attachment (ATA), MultiMediaCard (MMC)/secure digital input/output (SDIO), and compact Flash.

See the following chapters in the *i.MX35 (MCIMX35) Multimedia Applications Processor Reference Manual,* for more details about the booting modes:

- External Memory Interface (EMI)
- Enhanced Secured Digital Host Controller (eSDHC)
- Enhanced SDRAM Controller (ESDRAMC)
- Universal Serial Bus OTG and Host (USBOH)
- Configurable Serial Peripheral Interface (CSPI)
- Inter IC Module (I^2C)
- Memory Stick Host Controller (MSHC)

1   i.MX35 Flash Devices

The NAND Flash controller (NFC) provides system interface to standard NAND Flash devices, and hides the complexities of accessing the NAND Flash. The NFC provides a glueless interface to 8-bit and 16-bit NAND Flash parts with page sizes of 512 bytes, 2 Kbytes, or 4 Kbytes.

1.1   NFC Features

The NFC provides the following features:

- x8/x16 (pin-configurable) NAND Flash interface
- Internal RAM buffer (4 Kbytes, 512 bytes)
    - Can be configured as boot RAM
    - Operates as a buffer during normal operation
    - Registers and internal RAM buffer are memory-mapped to the same advanced high-performance bus (AHB) region
- Manual interface with NAND Flash devices
    - Supports all NAND Flash products up to 64 Kbyte blocks (for example, NFC supports SLC NAND Flash devices with 512 bytes per page, 16 Kbytes per block, and memory size up to 8 Gbits)
    - Supports SLC NAND Flash devices with 2 Kbytes per page, 128 Kbytes per block, and memory size up to 64 Gbits
    - Supports MLC NAND Flash devices with 4 Kbytes per page, 512 Kbytes per block, and memory size up to 256 Gbits
- Supports MLC NAND with two options for Reed-Solomon error correction (configurable):
    - Corrects four 9-bit symbol errors in 528 bytes (512 main bytes + 16 bytes spare)
    - Corrects eight 9-bit symbol errors in 538 bytes (512 main bytes + 26 bytes spare)
- AHB host interface

- — Supports read and write bursts
- — Supports 16-bit or 32-bit bus transfers
- Supports direct memory access (DMA) requests for page read, section read, and other read operations
- Supports error correction (ECC) mode and ECC mode bypass
- Supports multiple reset (reset of NFC and NAND Flash device)
- Internal boot code loader during power-up provides advanced data protection (can be enabled or disabled)
  - — Data protection
  - — RAM buffer write-protect mode provides write protection for the lower 2 Kbytes of RAM buffer) (see Section 39.4.3.6, Controller Status and Result of Flash Operation Register 2 (ECC_STATUS_RESULT2) in *i.MX35 (MCIMX35) Multimedia Applications Processor Reference Manual*)
  - — Write-protect mode for NAND Flash devices provides block-based write protection for NAND Flash
- Automatic write protection for RAM buffer and NAND Flash during power-up, in addition to run-time write protection modes for both the RAM buffer and the NAND Flash device
- Handshaking feature—INT pin indicates ready/busy status of NFC
- Special arbitration logic enables sharing of I/O pins with other memory controllers
- Electrically NAND Flash domain support from 1.75 V–3.6 V

1.2 NAND Flash Reference Application

Figure 1 shows the NAND Flash implementation according to the platform development kit (PDK) which uses the following features:

- 2 GByte Samsung MLC NAND Flash (K9LAG08UOM-2GB)
- NVCC_NAND = 3.3 V; NVCC_EMI3 = 1.8 V

    Since the chip select signals originate from the i.MX35 with 1.8 V logic, a level shifter is required to increase the voltage to 3.3 V and make the signals compatible with the NAND Flash device.
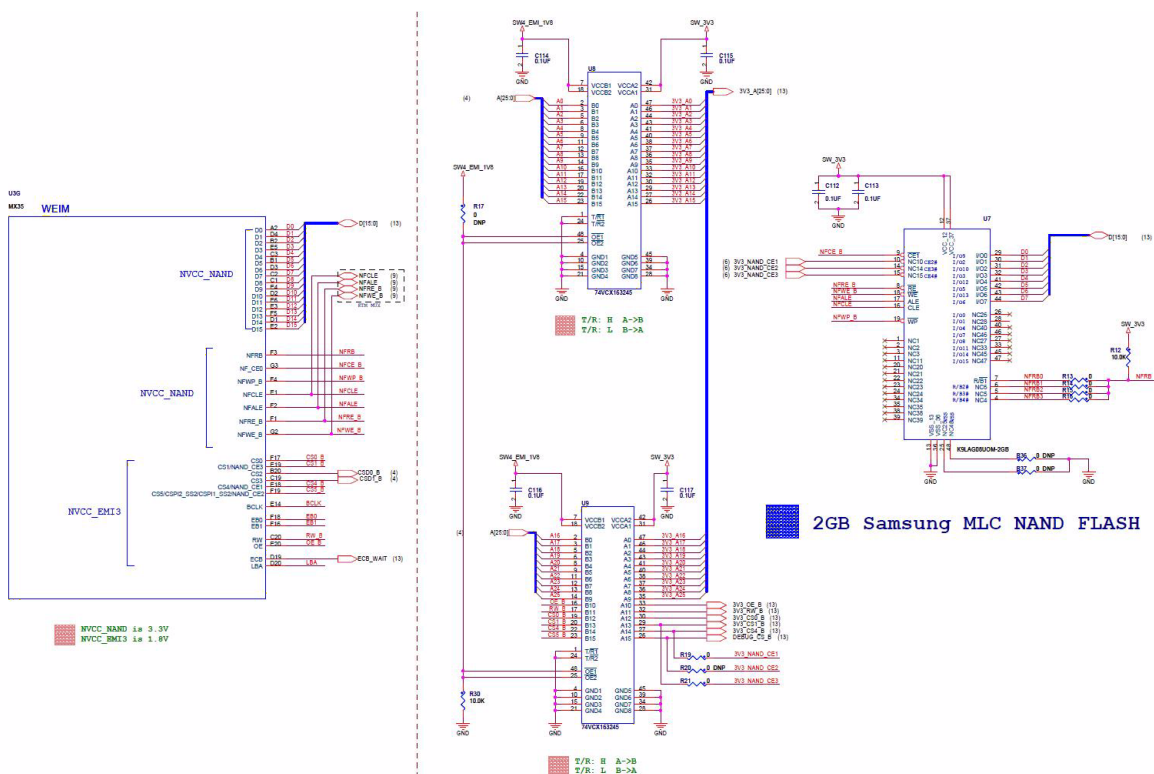

Figure 1. i.MX35 NAND Flash Reference Application

2 i.MX35 SDRAM Devices

The enhanced synchronous dynamic RAM controller (ESDRAMC) provides interface and control for synchronous DRAM (SDRAM) memories of the system. The SDRAM memories uses a synchronous interface with all signals registered on a clock edge. A command protocol is used for initialization, read, write, and refresh operations to the SDRAM. The protocol is generated on the signals by the controller when required due to external or internal requests. It has support for both single-data rate and double-data rate SDRAMs. It supports 64, 128, 256, or 512 Mbit and 1 or 2 Gbit 4-bank SDRAM by two independent chip selects up to 64 Mbytes addressable memory per chip select.

NOTE

The ESDRAMC and enhanced SDRAM controller (ESDCTL) mnemonics are equivalent. For historical reasons they are alternatively used throughout the document.

2.1   SDRAM Controller Features

The ESDRAMC includes the following features:

- Optimizes consecutive memory accesses through memory command anticipation (latency hiding)
  - Hides latency by optimization of the commands to both chip selects (command anticipation)
  - Keeps track of open memory pages
  - Bankwise memory address mapping
  - SDRAM burst length configuration of 4 or 8 (for 16-bit memory burst length, 4 is not supported) or full-page mode
  - Low power double data rate memory (LPDDR)/DDR burst length configuration of 8
  - Supports different internal burst lengths (1/4/8 words) by using burst truncate commands
  - ARM® AMBA AHB-lite compatible
  - Shared address and command bus to SDRAM/LPDDR
- Supports 64, 128, 256, or 512 Mbit and 1 or 2 Gbit sizes of 4-bank, single data rate, synchronous SDRAM, LPDDR and non-mobile DDR1 devices. Limited support for DDR2 devices (4 banks only, no ODT control signal)
  - Two independent chip selects
  - Up to 256 Mbytes per chip select
  - Up to four banks active simultaneously per chip select
  - JEDEC-standard pinout/operation
- Supports 16 and 32-bit mobile/low power DDR266 devices
- PC133-compatible interface
  - 133 MHz system clock achievable with **–7** option for PC133-compatible memories
  - Single fixed-length (4/8-word) burst or full-page access
  - Access time of 9-1-1-1-1-1-1-1 at 133 MHz (for read access, when memory bus is available, the row is open and the CAS latency is configured to 3 cycles). The access time includes the M3IF delay (assuming no arbitration penalty)
- Software-configurable for different system and memory devices requirements

- 16 or 32-bit memory data bus width (equal in both chip selects)
  — Number of row and column addresses
  — Row cycle delay (tRC)
  — Row precharge delay (tRP)
  — Row to column delay (tRCD)
  — Column to data delay (CAS Latency)
  — Load mode register to active command (tMRD)
  — Write to precharge (tWR)
  — Write to read (tWTR) for LPDDR memories only
  — LPDDR exit power-down to next valid command delay (tXS)
  — Active to precharge (tRAS)
  — Active to active (tRRD)
- Built-in auto-refresh timer and state machine
- Hardware- and software-supported self-refresh entry and exit
  — Data remains valid during system reset and low power modes
  — Auto-power-down timer (one per chip select)
  — Auto-precharge timer (one per bank in each chip select)

2.2 DDR2 Reference Application

Figure 2 show the DDR2 implementation according to the PDK that uses the following features:

- Four DDR2 memories 64 Mbyte = 2 Gbit
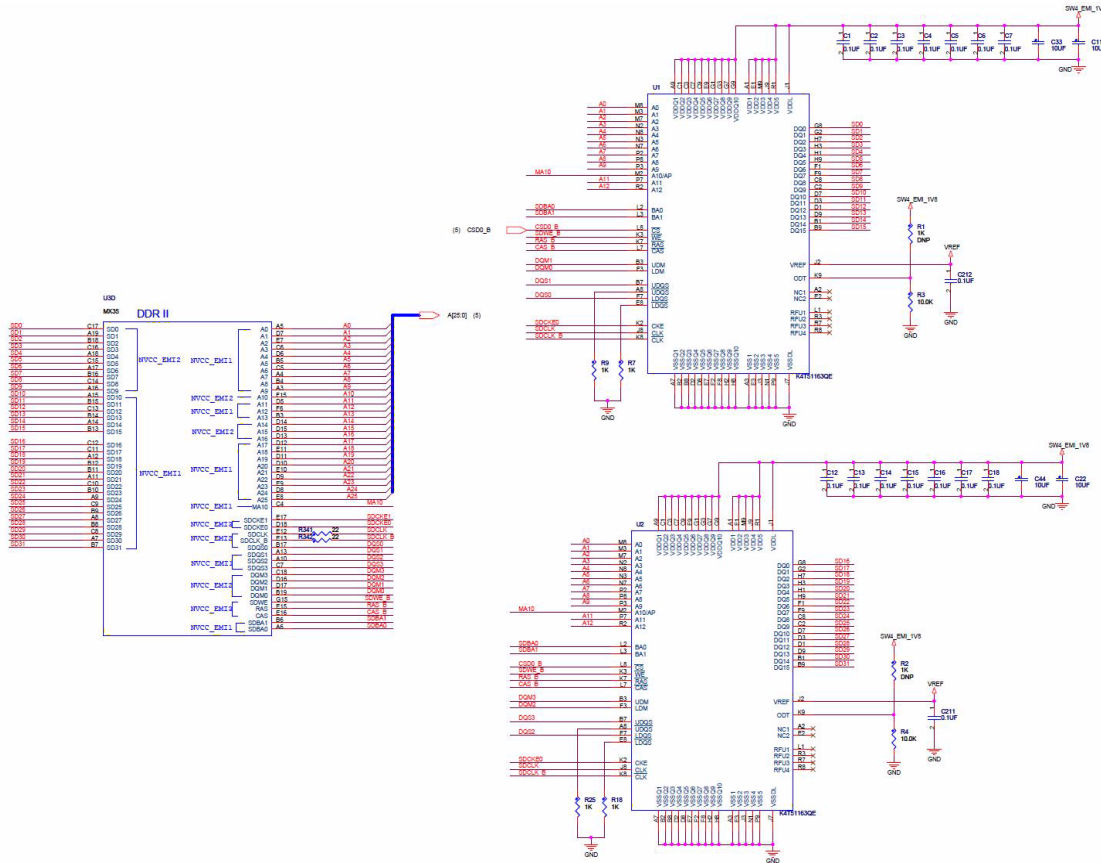- Two chip select, 32 data bit, 12 address bit; NVCC_EMIx = 1.8 V

Figure 2. i.MX35 DDR2 Application Reference

3 i.MX35 Memory Card/ATA Devices

The eSDHC provides interface between the host system and the SD/SDIO/MMC/CE-ATA cards. The eSDHC acts as a bridge, passing host bus transactions to the SD/SDIO/MMC/CE-ATA cards by sending commands and performing data accesses to/from the cards. It handles the SD/SDIO/MMC/CE-ATA protocols at the transmission level through the wireless external interface module (WEIM) interface located on chip select 0 (CS0).

Also, the MSHC is placed between the AIPS/AHB bus and the Sony Memory Stick PRO™ to support data transfer between the chip and the Memory Stick Pro.

3.1 Memory Card/ATA Device Features

The following sections discuss the features of memory card and ATA device.

3.1.1 eSDHC Features

The eSDHC includes the following features:

- Conforms to the SD host controller standard specification version 2.0 including test event register support
- Compatible with the MMC system specification version 4.2
- Compatible with the SD memory card specification version 2.0 and supports the high capacity SD memory card
- Compatible with the SDIO card specification version 2.0
- Compatible with the CE-ATA card specification version 1.0
- Designed to work with CE-ATA, SD memory, mini SD memory, SDIO, mini SDIO, SD combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 52 MHz
- Supports 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC modes, 1-bit/4-bit/8-bit
- CE-ATA devices
  - Up to 200 Mbps of data transfer for SD/SDIO cards using 4 parallel data lines
  - Up to 416 Mbps of data transfer for MMC cards using 8 parallel data lines
- Supports single block, multi block read and write
- Supports block sizes of 1–4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort
- Supports pause during the data transfer at block gap
- Supports SDIO read wait and suspend resume operations
- Supports auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period
- Represents a fully configurable 128×32 bit first-in, first-out (FIFO) for read/write data
- Supports internal and external DMA capabilities
- Supports advanced DMA to perform linked memory access

3.1.2 MSHC Features

The MSHC includes the following features:

- A gasket between IP bus and Sony memory stick host controller (SMSC)
  - IP interface transfer functionality as slave
  - Interrupts for transfer errors, or wait timeout

— Timeout function for abnormal transfer wait states

— Fixed 32-bit data bus

— Little-endian to IP data bus and big-endian to SMSC data bus

- SMSC to communicate to the Sony memory stick

— Registers structured in 64-bit format

— FIFO (4×64 bit)

— Interrupt after Memory Stick Pro communication completes

— DMA in dual address mode

- An embedded DMA controller through AHB bus

— DMA transfer through AHB interface as master

— Fixed burst length as INCR8

— Word alignment transfer size

- All functions controlled by fuse

- Test mode and DFT implementation

3.2 Memory Card/ATA Devices Reference Application

Figure 3 shows the multi-card combination implementation according to the PDK that uses the following features:

- SD+Memory Stick combo connector

  A switch is provided for SD2 signals as it is optional to communicate 4-bit to a Bluetooth transceiver on PDK.

- VDD_SD1_IO = 3.3 V

- NVCC_ATA = 3.3 V

- NVCC_SDIO = 3.3 V

- NVCC_CSI = 3.3 V

Figure 3 shows the i.MX35 memory card reference application.
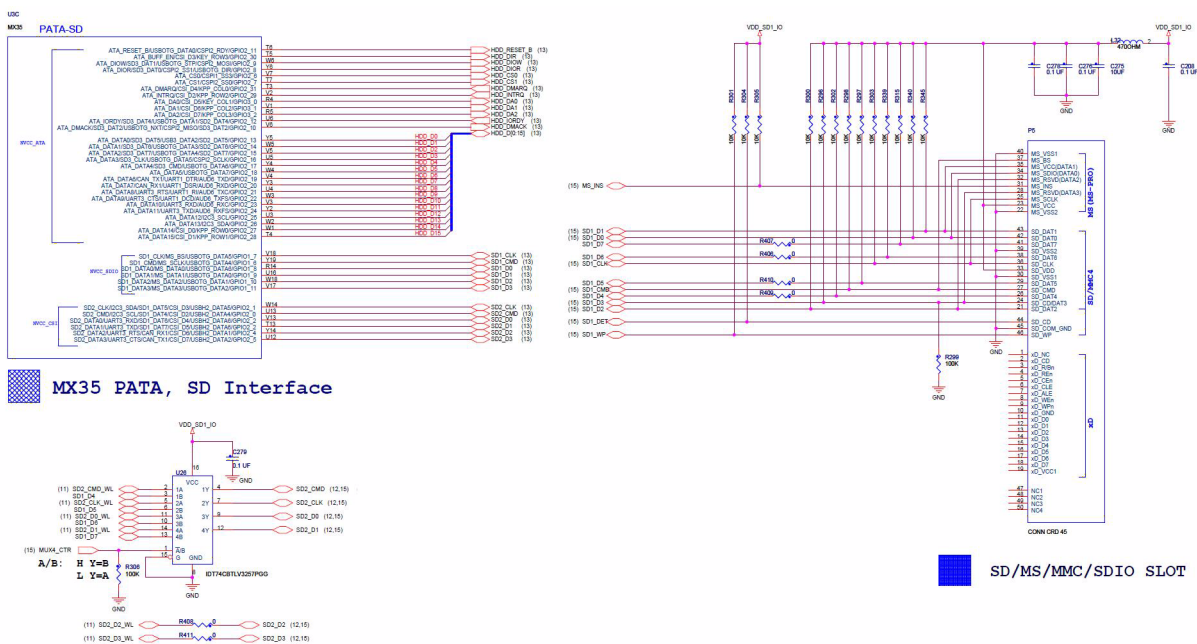
Figure 3. i.MX35 Memory Card Reference Application

Figure 4 shows the ATA implementation according to the PDK that uses the following features:

- 2×22 pin header connector (ASP-66686-20 from SAMTEC)
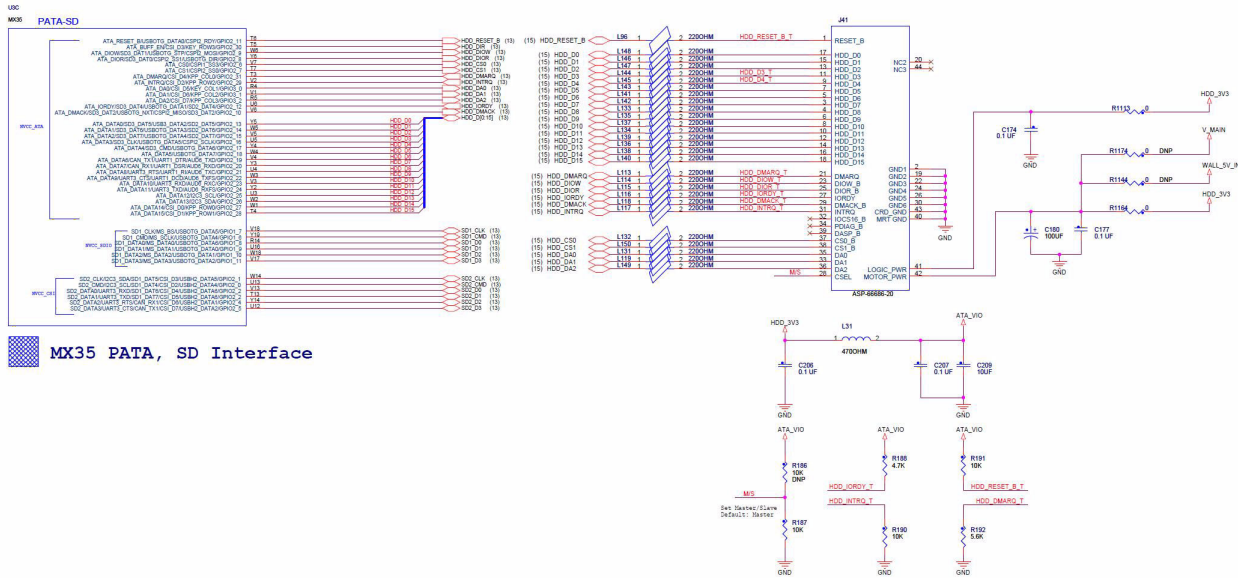- Ferrites for signal protection
- Voltage filtering

Figure 4. i.MX35 ATA Reference Application

4   i.MX35 NOR Flash Devices

The WEIM handles the interface for devices that are external to the chip, including generation of chip selects, clock, and control for external peripherals and memory. It provides asynchronous and synchronous access to devices similar to SRAM interfaces.

4.1   WEIM Features

The WEIM includes the following features:

- Six chip selects for external devices, with CS0 and CS1 each covering a range of 128 Mbytes and CS2–CS5 each covering a range of 32 Mbytes
- CS0 range can be increased to 256 Mbytes when collapsed with CS1
- Selectable protection for each chip select
- Programmable data port size for each chip select
- Asynchronous accesses with programmable setup and hold times for control signals
- Synchronous memory burst read mode support for AMD, Intel®, and micron burst Flash memory
- Synchronous memory burst write mode support for PSRAM (CellularRAMTM from Micron, Infineon, and Cypress), fixed write latency support
- Support for multiplexed address/data bus operation

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- External cycle termination/postpone with data transfer acknowledgment (DTACK) signal
- Programmable wait-state generator for each chip select
- Support for big-endian and little-endian modes of operation per access
- ARM AHB slave interface

4.2 NOR Flash Reference Application

Figure 5 shows the multi-card combination implementation according to the PDK that uses the following features:

- 64 Mbyte NOR FLASH spansion S29GL512P
- 16-bit data; 25-bit address
- NVCC_NAND = 3.3 V
- NVCC_EMI3 = 1.8 V
- NVCC_EMIx = 1.8 V

    Since address signals come from the i.MX35 with 1.8 V logic a level shifter is needed to increase the voltage to 3.3 V and to make the signals compatible with a NOR Flash device.
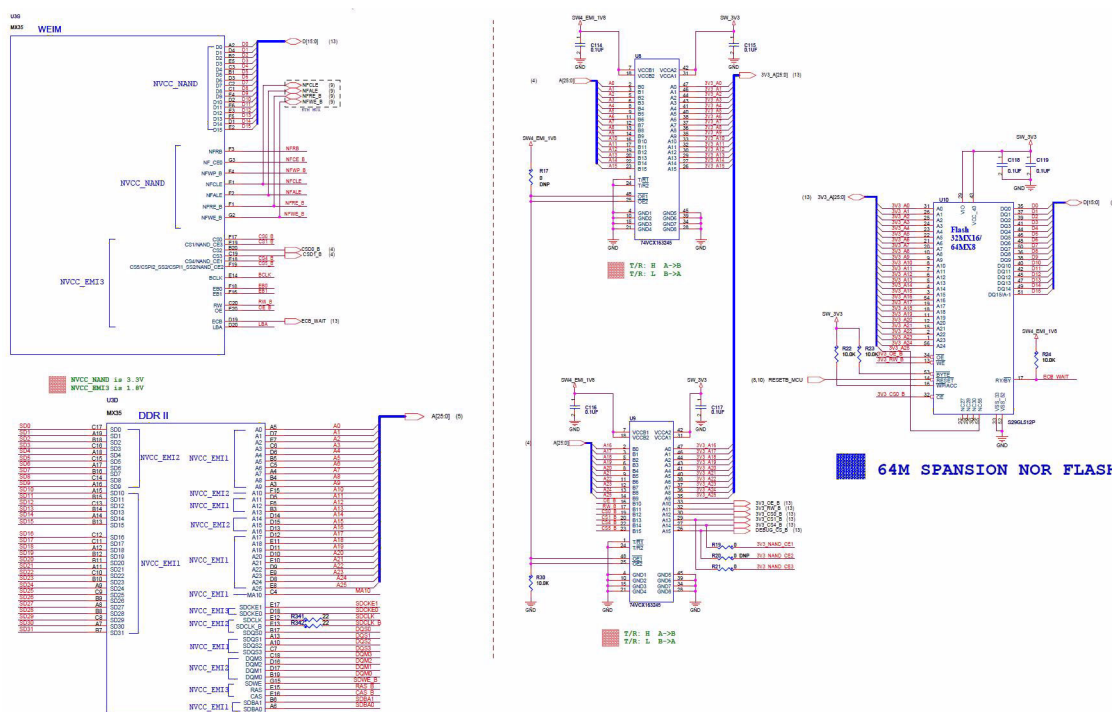
Figure 5. i.MX35 NOR Flash Reference Application

5 i.MX35 Inter IC (I²C) Devices

The I²C module provides functionality of a standard I²C slave and master. The I²C module is designed to be compatible with the standard Philips I²C bus protocol.

The I^{2}C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications that require occasional communication over a short distance between many devices. The flexible I^{2}C standard allows additional devices to be connected to the bus for expansion and system development.

The I^{2}C interface operates up to 400 Kbps, but it depends on the pin loading and timing characteristics. See *Philips I^{2}C-Bus Specification*, *Version 2.1,* for more information on pin requirements. The I^{2}C system is a true multiple-master bus including arbitration and collision detection that prevents data corruption, if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.

5.1   I^{2}C Features

The I^{2}C module includes the following key features:

- Compatibility with I^{2}C bus standard
- Multiple-master operation
- Software-programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

NOTE
There is no I^{2}C memory in the i.MX35 PDK.

6   i.MX35 Configurable Serial Peripheral Interface (CSPI) Devices

The CSPI module is a full-duplex, synchronous, four-wire serial communication module. The CSPI module contains a 8×32 receive buffer (RXFIFO) and a 8×32 transmit buffer (TXFIFO). The CSPI module allows rapid data communication with fewer software interrupts with data FIFOs.

6.1   CSPI Features

The CSPI module includes the following features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (CS) signals to support multiple peripherals

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- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 8-entry FIFO for both transmit and receive data
- Polarity and phase of the SS and SPI Clock (SCLK) are configurable
- DMA support
- Maximum operation frequency up to one-quarter of the reference clock frequency.

NOTE

There is no CSPI memory in the i.MX35 PDK.

7 i.MX35 Universal Serial Bus OTG and Host (USBOH)

The USBOH module provides high performance USB OTG functionality that compliants with the USB 2.0 specification, the OTG supplement, and the ULPI (USB 2.0 Transceiver Macrocell Interface (UTMI)+ Low Pin Interface) specification. The module consists of two independent USB cores—host core and OTG core, each with serial and ULPI USB ports.

In addition to the USB cores, the module provides a full-speed transceiverless link (TLL) operation on the OTG and the host ports. The OTG core also supplies the UTMI interface for the internal UTMI PHY.

7.1 USBOH Features

The USBOH module includes the following features:

- High-speed (HS)/full-speed (FS)/low-speed host-only core
  - HS/FS ULPI compliant interface
  - Software-configurable for full-speed/low-speed interface for serial transceiver
  - Full-speed transceiverless link logic (FS-TLL) for on-board connection to an FS/LS USB peripheral
  - Software-configurable interface for internal serial PHY (physical), external serial PHY, and ULPI (UTMI+ Low Pin Interface) PHY selection
- High-speed/full-speed/low-speed OTG core
  - HS/FS ULPI compliant interface
  - Software-configurable for ULPI or serial transceiver interface
  - High-speed (with ULPI transceiver), full-speed, and low-speed operation in host mode
  - High-speed (with ULPI transceiver), and full-speed operation in peripheral mode
  - Hardware support for OTG signaling, session request protocol and host negotiation protocol
  - Up to eight bidirectional endpoints
  - Software-configurable interface for internal UTMI PHY, external serial PHY, and external ULPI PHY selection
- Low power mode with local and remote wakeup capability
- Serial PHY interfaces configurable for bidirectional/unidirectional and differential/single ended
- Embedded DMA controller

7.2 USB OTG Reference Application

Figure 6 shows the USB OTG implementation according to the PDK that uses the following features:

- Electrostatic discharge (ESD) protection
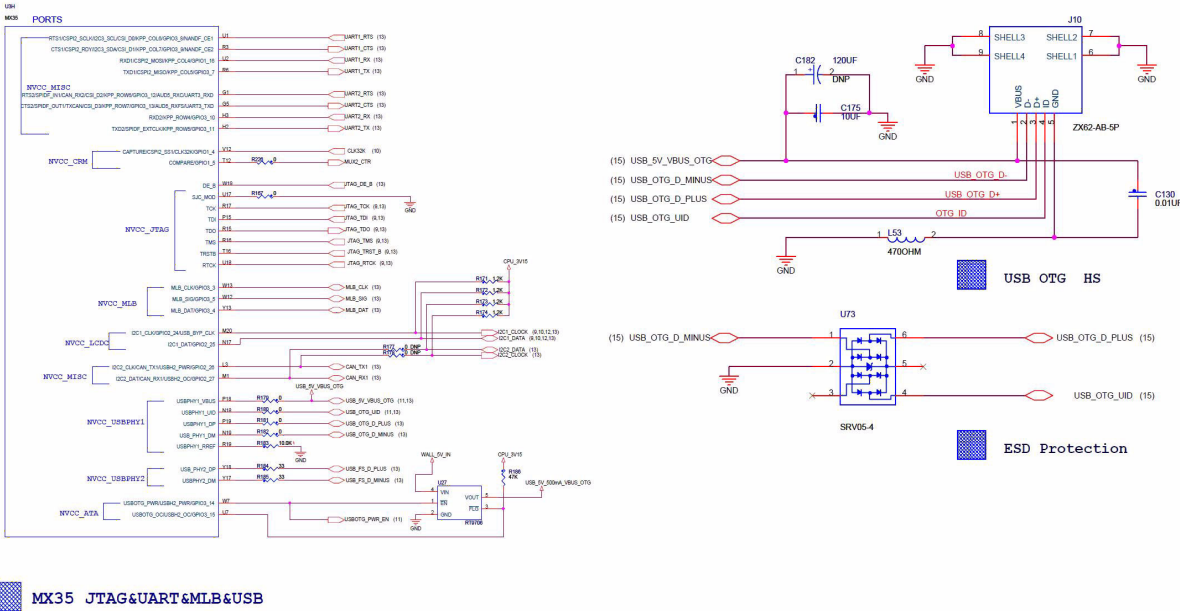- Internal PHY interface

Figure 6. USB OTG on i.MX35 Reference Application

8 References

The following complementary references for the i.MX35 are found at Freescale Semiconductor Inc. at http://www.freescale.com:

- *i.MX35 Multimedia Power Consumption Under Linux* (AN3876)

The following standard documentations are used as reference for this application note and are found at their respective Web sites:

- The I^2C-Bus Specification, Version 2.1 (January 2000) at http://www.nxp.com/acrobat_download2/literature/9398/39340011.pdf

9 Revision History

Table 1 provides a revision history for this application note.

Table 1. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	03/2010	Initial release.

i.MX35 Memories, Rev. 0

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Freescale Semiconductor, Inc.
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1-800-521-6274 or
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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
   Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
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   @hibbertgroup.com

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