Freescale Semiconductor
Application Note

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i.MX51 EVK Supply Current Measurements

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This application note aids the customer to design power management systems. By running several use cases, this document illustrates current drain measurements of the i.MX51 System on a Chip (SOC), taken on the i.MX51 EVK development system. Therefore, this document enables the customer to choose the appropriate power supplies for the i.MX51 SOC.

NOTE

The numbers presented are not guaranteed, as these are empirical numbers, based on a small sample size.

Contents

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1 Overview of i.MX51 Voltage Supply Rails

Before discussing current drain measurements on the i.MX51, an overview of the i.MX51 voltage supply rails is provided. Figure 1 illustrates a high level overview of each supply rail.

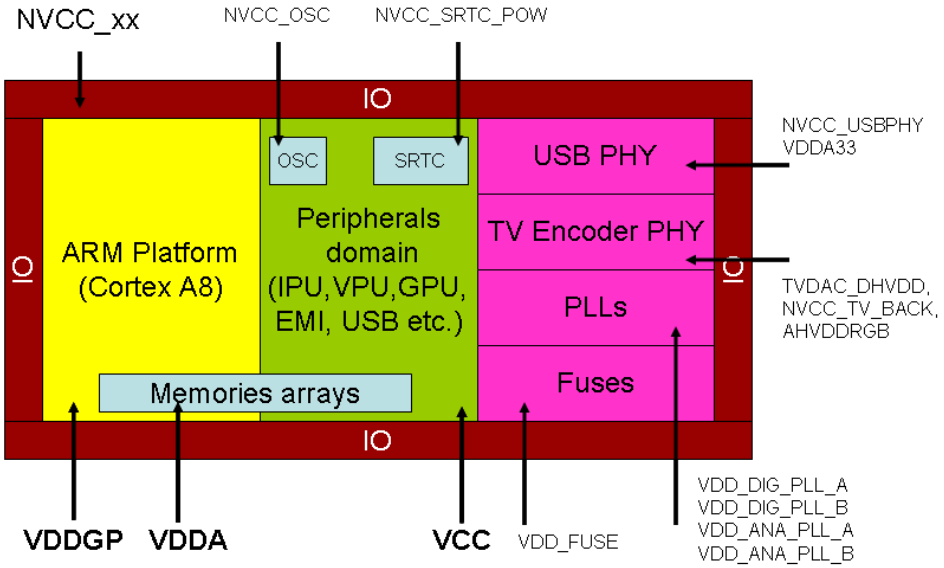

Figure 1. i.MX51 Power Rails

NOTE

See *i.MX51 Applications Processors for Consumer and Industrial Products* (IMX51CEC), for the recommended operating conditions of each supply rail and for a detailed description of the groups of I/Os (pins) each I/O voltage supply powers.

Table 1 provides a brief description of each supply rail.

Table 1. i.MX51 Supplies

Supply Name	Description	Nominal Voltage (V)[1]	Absolute Maximum (mA)[2]
VDDGP	ARM core supply voltage	1.0 for Automotive 1.1 for Consumer	TBD
VCC	Peripherals supply voltage—supply all the digital periphery inside i.MX51 (except of analog parts and IO)	1.225	700
VDDA	Supply of internal memories' arrays.	1.2	200
VDD_DIG_PLL_A, VDD_DIG_PLL_B	Supply of digital part of PLLs	1.2	10
VDD_ANA_PLL_A, VDD_ANA_PLL_B	Supply of analog part of PLLs	1.8	10
VDD_FUSE	Fuse box program supply (write only)	3.15	60

Table 1. i.MX51 Supplies (continued)

Supply Name	Description	Nominal Voltage (V)[1]	Absolute Maximum (mA)[2]
TVDAC_DHVDD, NVCC_TVBACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.75	200
NVCC_USBPHY	USB_PHY analog supply	2.5	30
VDDA33	USB_PHY_IO analog supply	3.3	100
NVCC_SRTC_POW	SRTC module and SRTC module IO supply (ultra low voltage IO cells)	1.2	Less than 1
NVCC_OSC	Internal oscillator supply	2.5	12
NVCC_EMI_DRAM	DDR and fuse read supply	1.8	Depends on load
NVCC_NANDF_x, NVCC_PER15/17	NAND flash I/O supplies and peripheral IO supplies (ultra high voltage IO cells)	1.875[3] 2.775 3.3	Depends on load
NVCC_EMI	EMI GPIO supplies	1.875 2.775	Depends on load
NVCC_I2C	1^2C and HS-I2C I/O supply	1.875 3.0	Depends on load
NVCC_PERxxx	Peripheral GPIO supplies	1.875 2.775	Depends on load
NVCC_HSxxx	HS_GPIO additional digital supplies	1.65 to 3.1	Depends on load
NVCC_IPUx	PU GPIO supplies	1.875 2.775	Depends on load
VREG	Internal unused logic (leave unconnected)	—	—
FASTR_ANA, FASTR_DIG	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND	—	—

1 The voltage numbers are for reference and convenience only. The official voltage numbers appear in *i.MX51 Applications Processors for Consumer and Industrial Products* (IMX51CEC) and *i.MX51A Automotive and Infotainment Applications Processors* (IMX51AEC).

2 Numbers presented here are for worst case conditions with some margin, intended for power management IC consideration. If the MC13892 power management device is used, refer to the to the internal bulletin titled *MC13892 and i.MX51 Systems* for connectivity recommendations.

3 There are several voltage options. The actual voltage levels that are used depend on which devices are connected.

2 Internal Power Measurement of the i.MX51 Processor

Several use cases (described in Section 3, “Use Cases and Measurement Results,”) are run on i.MX51 EVK board. The measurements are done for VDDGP and VCC, as those two supplies consume the majority of the internal power of the processor. For relevant use cases, the power of USB PHY and TVE DAC are added. However, the power of these supplies does not depend on specific use cases, but whether these modules are used or not. The power consumption of rest of the internal supplies from the Table 1 (OSC, SRTC, PLL) are comparatively negligible in all the modes, except in low power modes. The

NVCC_* power consumption is taken during the system level power measurements, as it mainly depends on the board level configuration and the components. Therefore, it is not included in the i.MX51 internal power analysis.

NOTE

Unless mentioned differently, all the measurements are done on typical process silicon, at room temperature (25 °C approximately).

The data for OS-less measurements is collected by running measurements on 3DS based PDK (FreeScale development board, non-public), using the internal diagnostic environment.

The software versions used for the measurement are as follows:

- WCE600_09.11.01_SS_RC1 (release of WinCE BSP)—The data for WinCE measurements is collected by running measurements on this software, using the Babbage EVK board.
- SDK1.7 Gnome mobile (release of Linux BSP)—The data for Linux measurements is collected by running measurements on this software, using the Babbage EVK board.

2.1 Voltage Levels and DVFS Usage in Measurement Process

The voltage levels of all the supplies, except for VDDGP and VCC, are set to the typical voltage levels as defined in *i.MX51 Applications Processors for Consumer and Industrial Products* (IMX51CEC).

The VDDGP and VCC supplies require special explanations. In order to save power, those voltages are changed using DVFS (dynamic voltage and frequency scaling), during the run time of the use cases or are reduced to standby voltage levels during low power modes.

2.1.1 VDDGP Voltage Levels

The target typical voltage levels for VDDGP are as follows:

- 0.85 V—For low frequency applications (below 167 MHz).
- 1.1 V—For high frequency applications (up to 800 MHz).

Most of the measurements are done using these voltage levels and the power data which appears in this document is according to these values. In case the measurement is done at different voltage levels, the results are scaled accordingly. In real applications when DVFS is applied, the frequency and voltage values are automatically adjusted based on the use case requirements. VDDGP DVFS voltage and voltage for STOP mode is 0.85 V.

2.1.2 VCC Voltage Levels

The target typical voltage levels for VCC are as follows:

- 1.05 V—For low frequency applications (below 44 MHz of bus frequency).
- 1.225 V—For high frequency applications (up to 166 MHz of bus frequency and 200 MHz for DDR).

Most of the measurements are done at 1.23 V and the power data which appears in the document is according to this value. In case the measurement is done at different voltage level, the results are scaled

accordingly. In real applications when DVFS is applied, the frequency and voltage values are automatically adjusted based on the use case requirements. VCC DVFS voltage is 1.05 V and for STOP mode is 0.95 V.

3 Use Cases and Measurement Results

3.1 Use Cases

The main use cases and subtypes, which form the benchmarks for i.MX51 internal power measurements, are as follows:

- Low power mode
  - Stop Mode
  - System Idle Mode
  - User Idle Mode
- General
  - Run Mode
- Audio playback
  - MP3 Audio Playback
  - WMA Audio Playback
- Video playback
  - H.264 Video Playback, 720p at 2771 Kbps
  - H.264 Video Playback, 720p at 4.5 Mbps on WVGA LCD
  - H.264 Video Playback, 720p at 9 Mbps on WVGA LCD
  - H.264 Video playback, D1 at 3.7 Mbps on WVGA LCD
  - H.264 Video playback on VGA LCD
  - WMV Video Playback, D1 at 4000 Kbps on WVGA LCD
  - WMV Video Playback, 720p at 2775 Kbps on WVGA LCD
  - H.264 Video playback, D1 at 3.7 Mbps on HD TV
- Video capturing
  - Video recording QCIF
  - Video recording D1
- Graphics
  - 3D Pinball demo
  - 2D Tiger demo

3.2 Low Power Mode Use Cases

3.2.1 Use Case 1—Stop Mode

The use case is as follows:

- ARM CORE is in the SRPG (state retention power gating) mode.
- L1 and L2 caches are power gated.
- IPU (image processing unit) and VPU (video processing unit) are in PG (power gating) mode.
- All PLLs (phase locked loop) and CCM (clock controller module) generated clocks are OFF.
- USBPHY PLL is OFF.
- CKIL (32 KHz) input is ON.
- All the modules are disabled.
- External high frequency crystal and on chip oscillator are powered down (by asserting SBYOS bit in CCM).
- Standby voltages are applied to VDDGP and VCC.

In this mode, no current flow is caused by external resistive loads. This use case simulates the situation when the device is in standby mode (commonly called suspend mode in OS).

Table 2 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 2. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	0.3	0.35	0.13	0.15
VCC	0.95	0.86	0.9	1.42	1.5
VDDA[2]	1.25	0.25	0.2	0.25	0.2
NVCC_OSC[3]	2.5	0.03	0.01	0.03	0.01
Total (mW)		1.44		1.83	

1 Use the following command to enter STOP mode in Linux: `echo mem > /sys/power/state`.
2 The power of VDDA is measured in the IC tester.
3 The power of NVCC_OSC is measured in OS-less configuration.

3.2.2 Use Case 2—System Idle Mode

The use case is as follows:

- ARM is in SRPG mode.
- Operating system is ON.
- LCD is turned OFF.
- Screen is not refreshed.

This use cases simulates the situation when the device is left idle for some time and the display is turned OFF after the timer expires.

Table 3 shows the measurement results when this use case is applied on the i.MX51 processor. To obtain these numbers for Linux the following conditions must be met:

1. If no devices connected to UART, require a baud rate greater than 1 Mbps, add `debug_uart=on` to the Linux boot command.
2. FEC and USB are suspended, either manually or automatically.

   To turn off the FEC use this command: `ifconfig eth0 down`

   To suspend the USB devices, use Linux commands to set the suspend state of all USB devices to automatic. USB-SATA should be suspended explicitly.
3. DVFS-Core is enabled or the ARM core frequency is set to 160 MHz through the CPUFREQ. To enable DVFS-CORE use the following command:

   ```
   echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable
   ```
4. The display turns off after some time in the idle state. To disable the display immediately, use the following command: `echo 1 > /sys/class/graphics/fb0/blank`
   where fb0 is the location of the frame buffer.
5. In this state all the peripheral domain clocks are sourced from the 24 MHz oscillator. To check if the clocks are setup correctly in this mode, use the following command: `cat /proc/cpu/clocks`
   The rate of main_bus_clk (and all the associated peripheral clocks) should be 24 MHz.

Table 3. Measurement Results

Domain	Voltage (V)	WinCE		Linux	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	0.34	0.4	0.3	0.35
VCC	1.23	10	8.1	8	5.5
Total (mW)		10.34		8.3	

3.2.3 Use Case 3—User Idle Mode

The use case is as follows:

- ARM is in SRPG mode most of the time.
- Operating system and LCD is on, but not in operation.
- The WVGA size screen refresh is done by IPU.

The use case simulates the situation when the device is left idle and no application is performed on the screen (like reading from the screen).

Table 4 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 4. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	0.34	0.4	0.36	0.43
VCC	1.23	75	61	49.9	40.5
Total (mW)		75.34		50.26	

1 Linux numbers are taken with both DVFS-CORE and DVFS-PER enabled. To enable DVFS-PER use this command: `echo 1 > /sys/devices/platform/mxc_dvfsper.0/enable`. The DVFS-CORE is enabled using this command: `echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable`

3.3 General Use Cases

3.3.1 Use Case 1—Run Mode (Dhrystone Benchmark)

In this use case, Dhrystone test is performed on an OS-less environment. The ARM processor runs the test in a loop at a frequency of 800 MHz, where the junction temperature is kept at 45 °C (app). Run power of VDDGP is monitored.

Table 5 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 5. Measurement Results

Domain	Voltage (V)	OS Less	
		P (mW)	I (mA)
VDDGP	1.05	504	480

3.4 Audio Playback Use Cases

3.4.1 Use Case 1—MP3 Audio Playback

The use case procedure is as follows:

6. MP3 (MPEG-1 audio layer 3) decoding on Cortex is run using WinCE player.
7. Audio playback is run through SSI (serial synchronous interface).
8. The stream 128 Kbps_44 KHz_s_mp3.mp3 is taken from the SD (secure digital) card.

The LCD is turned OFF after the timer expires.

Table 6 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 6. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	9.1	10.7	10.6	12.5
VCC	1.23	12.5	10.1	13.6	11
Total (mW)		21.6		24.2	

1 Linux numbers are taken using gst-player. To obtain these numbers, follow the instructions in Section 3.2.2, "Use Case 2—System Idle Mode," any time during audio playback.

3.4.2 Use Case 2—WMA Audio Playback

The use case procedure is as follows:

1. WMA (Windows media audio) decoding on Cortex is run using WinCE player.
2. Audio playback is run through SSI.
3. The stream 128kbps_44khz_s_wma.wma is taken from the SD card.

The LCD is turned OFF after the timer expires.

Table 7 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 7. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	8.7	10.2	9.5	11.2
VCC	1.23	12.3	10	12.9	10.5
Total (mW)		21		22.4	

1 Linux numbers are taken using gst-player. To obtain these numbers, follow the instructions in Section 3.2.2, "Use Case 2—System Idle Mode," any time during audio playback.

3.5 Video Playback Use Cases

3.5.1 Use Case 1—H.264 Video Playback, 720p at 2771 Kbps

This use case has the following features:

- The video source is H.264, 720p resolution, 15 fps (frames per second).
- The audio source is AAC (advanced audio coding), 48 KHz, 128 Kbps.
- For Windows, the display is of WVGA (wide video graphics array) resolution.
- For Linux, the resolution used is 1024×768, using DVI.

The video/audio stream is loaded into the SD card and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 8 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 8. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	28.5	33.5	29.2	34.3
VCC	1.23	124.6	101.3	102.7	83.5
Total (mW)		153.1		131.9	

1 Linux numbers are taken using gst-player. Frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 83.25 MHz and 66.5 MHz to 41.625 MHz respectively. To achieve these numbers, disable the FEC and USB, as described in Section 3.2.2, "Use Case 2—System Idle Mode." Also, enable software bus frequency scaling using the following command: `echo 1 > /sys/devices/platform/busfreq.0/enable`

3.5.2 Use Case 2—H.264 Video Playback, 720p at 4.5 Mbps on WVGA LCD

This use case has the following features:

- The video source is H.264, 720p resolution, 23 fps, 4.5 Mbps bitrate.
- The audio source is MP3, 64 Kbps.
- The display is of WVGA resolution.

The video/audio stream is loaded from the SD card and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to WVGA and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 9 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 9. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	34	40
VCC	1.23	135	110
Total (mW)		169	

3.5.3 Use Case 3—H.264 Video Playback, 720p at 9 Mbps on WVGA LCD

This use case has the following features:

- The video source is H.264, 720p resolution, 30 fps, 9 Mbps bitrate

- The audio source is MP3, 64 Kbps.
- The display is of WVGA resolution.

The video/audio stream is loaded into the DDR (double data rate) memory and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to WVGA in IPU and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 10 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 10. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	26	30.6
VCC	1.23	150	122
Total (mW)		176	

3.5.4 Use Case 4—H.264 Video Playback, D1 at 3.7 Mbps on WVGA LCD

This use case has the following features:

- The video source is H.264, D1 resolution, 30 fps, 3.7 Mbps bitrate.
- The audio source is MP3, 64 Kbps.
- The display is of WVGA resolution.

The video/audio stream is loaded from the SD card and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to WVGA in IPU and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 11 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 11. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	36	42.3	38.5	45.3
VCC	1.23	124	100.8	81	65.8
Total (mW)		160		119.5	

1 Linux numbers are taken using gst-player. Frequencies of AHB bus and peripheral bus are scaled from 133 MHz to 66.5 MHz and 66.5 MHz to 33.3 MHz respectively. DVFS-PER is enabled in this use case by the following command:
`echo 1 > /sys/devices/platform/mxc_dvfsper.0/enable`

3.5.5 Use Case 5—H.264 Video Playback on VGA LCD

This use case has the following features:

- The video source is H.264, 640 × 480 resolution, 30 fps.
- The audio source is AAC, 48 KHz, 128 Kbps, 2-channel CBR (constant bit rate).
- For Windows, the display is of WVGA resolution.
- For Linux, the resolution used is 1024 × 768, using DVI.

The video/audio stream is loaded into the SD card and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then rotated in the IPU and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 12 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 12. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	28.6	33.6	29.3	34.5
VCC	1.23	117.6	95.6	81.2	66
Total (mW)		146.2		110.5	

1 Linux numbers are taken using gst-player. Frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 83.25 MHz and 66.5 MHz to 41.625 MHz respectively. To achieve these numbers, disable the FEC and USB, as described in Section 3.2.2, “Use Case 2—System Idle Mode.” Also, enable software bus frequency scaling using the following command: `echo 1 > /sys/devices/platform/busfreq.0/enable`

3.5.6 Use Case 6—WMV Video Playback, D1 at 4000 Kbps on WVGA LCD

This use case has the following features:

- The video source is WMV (windows media video), D1 resolution, 30 fps, 4000 Kbps bitrate.
- The audio source is 96 Kbps, 44 KHz, stereo 2-pass VBR (variable bitrate).
- The display is of WVGA resolution.

The video/audio stream is loaded into the DDR memory from the SD card and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to WVGA in IPU and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 13 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 13. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	25	29.4
VCC	1.23	121	98.4
Total (mW)		146	

3.5.7 Use Case 7—WMV Video Playback, 720p at 2775 Kbps on WVGA LCD

This use case has the following features:

- Video source is WMV9, 720p resolution, 30 fps, 2775 Kbps bitrate
- Audio source is 96 Kbps, 44 KHz, stereo CBR (two channels)
- Display is of WVGA resolution

The video/audio stream is loaded from SD card to the DDR memory and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to WVGA in IPU and displayed on the LCD display with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 14 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 14. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	24	28.2
VCC	1.23	144	117
Total (mW)		168	

3.5.8 Use Case 8—H.264 Video Playback, D1 at 3.7 Mbps on HD TV

This use case has the following features:

- The video source is H.264, D1 resolution, 30 fps, 3.7 Mbps bitrate
- The audio source is MP3, 64 Kbps.
- The display is a 720p HD (high definition) TV set with a refresh rate of 50 Hz.

The video/audio stream is loaded from the SD card and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is taken by the IPU and is up-sized to 720p. It is then sent through the internal TV encoder and DAC to the TV set, which is in the component mode. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 15 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 15. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	30	35.3
VCC	1.23	135	109.7
TVDAC_DHVDD	2.75	455[1]	165.4
Total (mW)		620	

1 The number of 455mW is the result of the current required by standard for 720p TV.

3.6 Video Capturing Use Cases

3.6.1 Use Case 1—Video Recording QCIF

This use case has the following features:

- The coded video target is H.264, QCIF (quarter common intermediate format), 512 Kbps
- The coded audio target is MP3, 32 Kbps

The video signal is captured by a sensor and is coded by the VPU in H.264 format. Also the audio signal is captured by a microphone through the SSI and is coded by Cortex-A8 into MP3 format. The video and audio signals are muxed by Cortex-A8. The file is stored in the DDR memory.

Table 16 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 16. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	32	37.6
VCC	1.23	102	83
Total (mW)		134	

3.6.2 Use Case 2—Video Recording D1

This use case has the following features:

- The coded video target is H.264, D1 resolution, 2048 Kbps
- The coded audio target is MP3, 32 Kbps.

The video signal is captured by a sensor and is coded by the VPU in H.264 format. Also the audio signal is captured by a microphone through the SSI and is coded by Cortex-A8 into MP3 format. The video and audio signals are muxed by Cortex-A8. The file is stored in the DDR memory.

Table 17 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 17. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	0.85	52	61.2
VCC	1.23	173	140.6
Total (mW)		225	

3.7 Graphics Use Cases

3.7.1 Use Case 1—3D Pinball Demo

Pinball is a complex OpenGLES 2.0 3D animation of a pinball game, ongoing while the camera is panning around the room. In this use case, pinball is run, without DMI (display module interface, between GPU and IPU) synchronization. It has VGA resolution with a frame rate of 23 fps.

Table 18 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 18. Measurement Results

Domain	Voltage (V)	WinCE		Linux[1]	
		P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	1.1	207	188.2	447	406.4
VCC	1.23	286	232.5	352	281.6
Total (mW)		493		800	

1 Power optimizations are still on-going.

NOTE

Since the CPU is heavily loaded, applying DVFS has almost no effect on the power numbers.

3.7.2 Use Case 2—2D Tiger Demo

Tiger is a complex OpenVG vector graphics animation of a tiger head, redrawn from the vector data, by rotating each frame. In this use case, the tiger animation is run without DMI synchronization. It has VGA resolution with a frame rate of 28–30 fps.

Table 19 shows the measurement results when this use case is applied on the i.MX51 processor.

Table 19. Measurement Results

Domain	Voltage (V)	WinCE	
		P (mW)	I (mA)
VDDGP	1.1	471	428.2
VCC	1.23	178	144.7
Total (mW)		649	

NOTE

Since the CPU is heavily loaded, applying DVFS has almost no effect on the power numbers.

4 Comparison between Power Consumption and Exit Time in Low Power Modes

This part of document presents the trade-off between the power consumption in various low power use cases (modes) and the time required to return from this mode to the normal operation (exit time).

Some software delays can vary drastically depending on the OS power framework and the external hardware. OS power framework sequentially signals the drivers to resume the normal operation of the attached hardware. OS scheduler can then run the service thread, in response to the wake up request.

Figure 2 shows the dependence of power consumption with exit time. The Y-axis represents the power and the exit time and the X-axis represents the different modes in use.

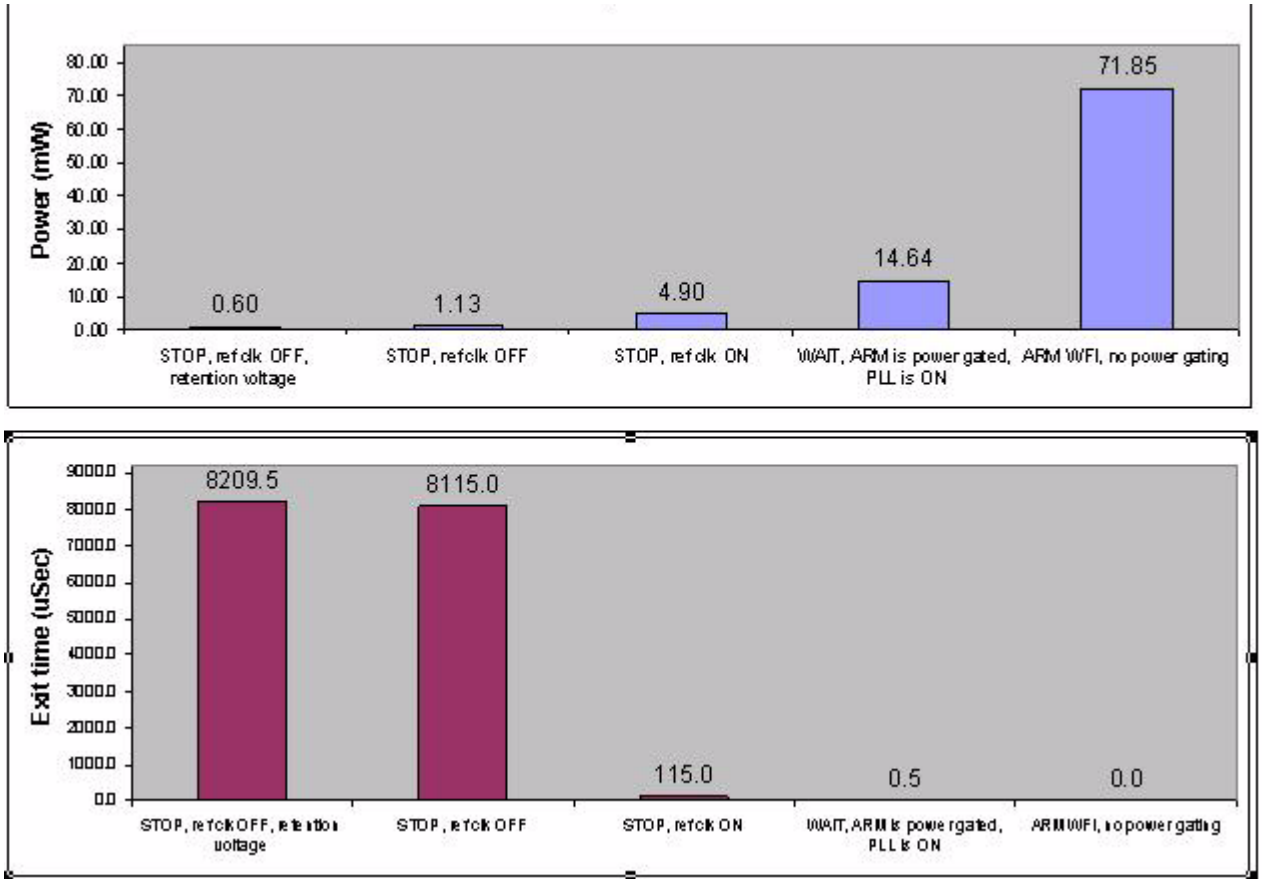

Figure 2. Graph between Power Consumption and Exit Time

The five modes shown in Figure 2 are explained as follows:

- Modes 1,2—*STOP, ref clk OFF, retention voltage* and *STOP, refclk OFF* are equal to the mode described in Section 3.2.1, "Use Case 1—Stop Mode."
- Mode 3—*STOP, refclk ON* is the same as described in Section 3.2.1, "Use Case 1—Stop Mode," but with the reference clocks remain ON for quicker exit. This mode is not implemented in the OS.
- Mode 4—*WAIT, ARM is power gated* is the mode when the peripheral domain is in IDLE state and the ARM platform is in SRPG mode
- Mode 5—*ARM WFI* is the mode where the system is ON, doing nothing and ready to start the task.

NOTE

The exit times indicated here is from the hardware perspective only—voltage ramp, OSC power up, PLL relock.

5 Revision History

Table 20 provides a revision history for this application note.

Table 20. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	02/2010	Initial Release.
1	05/2010	Updated Table 1 Updated table numbers in Section 3 Updated footnotes of Table 2, Table 4, Table 6, Table 7, Table 8, Table 12 Updated Linux field of VDDGP and VCC rows in Table 3 Added text before Table 3 about Linux conditions Updated WinCE I (mA) field of VCC row and Linux field of VDDGP and VCC rows in Table 4 Updated Linux field of VDDGP and VCC rows in Table 6 Updated Linux field of VDDGP and VCC rows in Table 7 Updated WinCE I(mA) field of VDDGP row in Table 10 Updated WinCE I (mA) field of TVDAC_DHVDD row in Table 15 Updated WinCE I (mA) field of VDDGP row in Table 18

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