

AN12446 从 RT1020 到 RT1010 的迁移指南

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1、引言

本文档介绍了用于嵌入式系统的开发从 i.MXRT1020 到 i.MX RT1010 跨界处理器进行迁移的关键点。它描述了硬件板的设计注意事项，软件和工具。

本文档未尝试比较这两个芯片的优缺点，因为它们有各自的目标市场。该文件是为那些使用 i.MX 1020 开发嵌入式系统并决定将项目迁移到 i.MX RT1010 的使用者。读者应具有 i.MX 1020 经验，并希望使用 i.MX RT1010 开始项目。

i.MX RT1020 通过在低成本 LQFP 封装中提供高性能功能集，扩展了 i.MX RT 跨界处理器系列，进一步简化了客户的电路板设计和布局。i.MXRT1020 在 Arm® Cortex® -M7 核心上以 500MHz 的频率运行。

i.MX RT1010 被定义为一个适用于低成本应用的价格优越的跨界处理器，具有更高性能和

更高实时响应至关重要。它包含运行频率高达 500 MHz 的单个 Arm Cortex-M7 内核以及 ADC , PWM , 计时器模块和 I2S 接口 , 使其成为 IOT 节点、电机控制、工业应用、和音频应用的理想解决方案。i.MX RT1010 为客户简化了电路板的设计和布局。i.MX RT1010 在 Arm Cortex-M7 核心上运行频率为 500 MHz。

2、概述

表 1 描述了 RT1010 和 RT1020 的功能差异。

表 1. RT1010 和 RT1020 的功能差异汇总

1. i.MX RT1020 功能集因封装而异。有关详细信息，请参阅 i.MX RT1020 数据表。

特点	i.MX RT1020 ¹	i.MX RT1010
CPU 核心	Arm Cortex-M7 500 MHz Double Precision FPU + MPU	Arm Cortex-M7 500 MHz Single FPU + MPU
PLL	PLL2 - System PLL (528 MHz) PLL3 - USB1 PLL (480 MHz) PLL4 - Audio PLL PLL6 - ENET PLL	PLL2 - System PLL (528 MHz) PLL3 - USB1 PLL (480 MHz) PLL4 - Audio PLL PLL6 - ENET PLL
能源管理	Integrated DCDC/LDO	Integrated DCDC/LDO
高速缓存	16 K/16 K L1 I/D-cache	16 K/8 K L1 I/D-cache
内存	256 KB FlexRAM(Bank0 - Bank7) (OCRAM+I/DTCM)	128 KB FlexRAM(Bank0 - Bank 3) (OCRAM+I/DTCM)
串行闪存接口	Dual-channel QSPI NOR and NAND Octal flash and RAM XIP supported	Dual-channel QSPI NOR Octal flash and RAM XIP supported
音频	Multi-channel I ² S × 1, SAI/I ² S × 2, SPDIF Tx/Rx, MQS	Multi-channel I ² S × 1, SAI/I²S × 1 , SPDIF Tx/Rx, MQS
ADC/ACMP	12-bits ADC × 2, ACMP × 4	12-bits ADC × 1
计时器和 PWM	GPT × 2, PIT × 4, QTimer × 2, FlexPWM × 2, QuadDecoder × 2, WDOG × 3, ETM × 1	GPT × 2, PIT × 1 , FlexPWM × 1 , WDOG × 3, ETM × 1

Connectivity	LPUART × 8, LPSPI × 4, LPI ² C × 4, FlexIO × 1, FlexCAN × 2	LPUART × 4, LPSPI × 2, LPI²C × 2, FlexIO × 1
安全系统	DCP, BEE, TRNG, SNVS, SJC	DCP, OTFAD , TRNG, SNVS, SJC
USB	USB OTG HS w/PHY × 2	USB OTG HS w/PHY × 1
高速 GPIO	NA	29 channels
DRAM 接口	SDRAM 8/16-bit, 133 MHz	NA
内存	8/16-bit parallel NOR flash 8/16-bit SLC NAND flash (SW ECC)	NA
eMMC/SD 接口	eMMC 4.5/SD 3.0 × 2	NA
以太网	10/100 with IEEE1588 × 1	NA
Boot Devices	Serial NOR flash via FlexSPI Interface Serial NAND Flash via FlexSPI Interface Parallel NOR flash with the Smart External Memory Controller (SEMC), located on CS0, 16-bit bus width. NAND Flash with SEMC interface, located on CS0, 8-bit/16-bit bus width. SD/MMC/eSD/SDXC/eMMC4.4 via uSDHC interface, supporting high capacity cards Serial NOR/EEPROM boot via LPSPI	Serial NOR flash via FlexSPI Interface

1. i.MX RT1020 功能集因封装而异。有关详细信息，请参阅 i.MX RT1020 数据表。

3、系统模块

3.1 时钟

RT1010 的 PLL 可从 RT1020 重复使用，这意味着 RT1010 可以直接重复使用 RT1020 的 PLL 配置。但是，CCM 的时钟树有所修改。表 2 描述了 RT1010 和 RT1020 的 CCM 时钟树差异。

有关详细信息，请参见《RT1010 和 RT1020 参考手册》。

表 2. RT1010 和 RT1020 的时钟树差异摘要

RT1010 removal	ARM_PODF DIV
	PERIPH_CLK2_PODF DIV

	USDHC1_CLK_ROOT
	USDHC2_CLK_ROOT
	SEMC_CLK_ROOT
	SAI2_CLK_ROOT
	CAN_CLK_ROOT
RT1010 add	FLEXSPI_CLK_SRC MUX
	ADC_ALT_CLK
	PII3_sw_clk as a source for SAI1 and SAI3
RT1010 update	AHB_CLK_ROOT -> CORE_CLK_ROOT
	FlexSPI CLK source: SEMC_CLK_ROOT_PRE -> PLL2

3.2 高速 GPIO

RT1010 提供 29 个高速 GPIO (HSGPIO) 的通道。可以以高频率访问 HSGPIO。HSGPIO 的最大触发频率是内核频率的一半,但焊盘的最大触发频率约为 200 MHz。因此, HSGPIO 的最大触发频率约为 200 MHz。

GPIO1 是通用 GPIO 端口, GPIO2 是 HSGPIO 端口, 如图 1 所示。所述 IOMUXC_GPR26 寄存器控制端口对应映射到焊盘, 如图 2 所示。

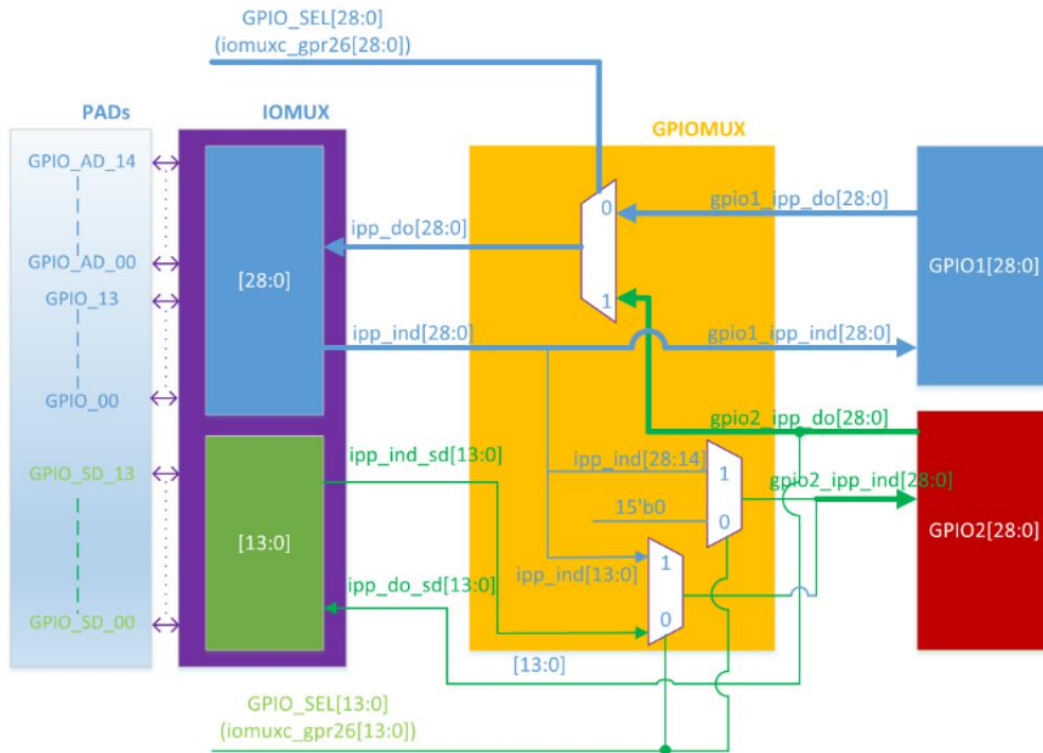


图 1. GPIOMUX 框图

GPR Register

Address: 400A_C000h base + 68h offset = 400A_C068h



IOMUXC_GPR_GPR26 field descriptions

Field	Description
GPIO_SEL	Select GPIO1 or GPIO2

图 2 IOMUXC_GPR26 字段描述

根据图 1 和图 2，可以得到表 3。

表 3.高速 GPIO 映射表

	GPIO	PAD
IOMUXC_GPR26[28:0] = 0	GPIO1[28:0]	GPIO[13:0],GPIO_AD[14:0]
	GPIO2[13:0]	GPIO_SD[13:0]
IOMUXC_GPR26[28:0] = 1	GPIO1[28:0]	NA
	GPIO2[28:0]	GPIO[13:0],GPIO_AD[14:0]

3.3 SAI

RT1020 中有三个 SAI，而 RT1010 中只有两个。RT1010 中删除了 SAI2，在 RT1010 中只提供 SAI1 和 SAI3。

3.4 OTFAD

对于实时解密和 XIP，RT1020 使用总线解密引擎（BEE），而 RT1010 使用实时 AES 解密（OTFAD）。如果使用 ROM 进行镜像解密，则无需更改软件或硬件。BEE 和 OTFAD 使用不同的 IP，它们间就存在一些差异。例如，BEE 通过 PRDB 加密参数，但 OTAFD 通过 Key Blob 加密。

- BEE

典型的 AES 引擎在 1-2 个机器周期内执行单轮操作。

- OTFAD

大量流水线化的 AES 引擎针对解密进行了优化，每个循环执行三轮。

4、硬件设计

RT1010 的硬件设计要点与 RT1020 几乎相同。有关详细信息，请参阅 RT1010 硬件设计指南。

5、修订历史

表 4.修订历史

Revision No.	Date	Description
0	May 2019	Initial release
1	November	Updated Table1

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