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如何在 **RT** 系列上使能扩频功能

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文档信息

信息	内容
关键词	i.MX RT, i.MX RT Crossover MCUs, 扩频, 通信技术, 频谱, 传输信号, 带宽, 无线通信, 电磁干扰, EMI, EMI 性能, System-on-Chip, SoC, 应用处理器
摘要	本文旨在介绍有关扩频的基本理论，以及如何为 RT 功能启用此功能以增强 EMI 性能。

1 背景

扩频是一种将传输信号的频谱转换为比其原始带宽更宽的通信技术，并广泛用于无线通信领域。

本文旨在介绍有关扩频的基本理论，以及如何为 RT 功能启用此功能以增强 Electro Magnetic Interference（EMI）性能。

2 扩频介绍

- 窄带介绍
  窄带信号的信号强度集中在 图 1。

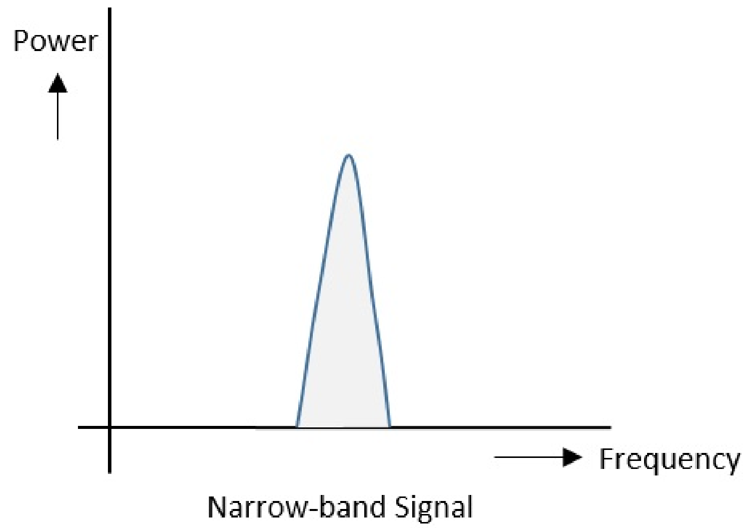

图 **1.** 窄带信号

  它有如下一些特性：
  -信号频带占用的频率范围很窄。
  -功率密度高。
  -能量扩散低且集中。
  这种信号很容易产生干扰。
- 扩频信号
  扩频信号具有 图 2 所示的信号强度分布。

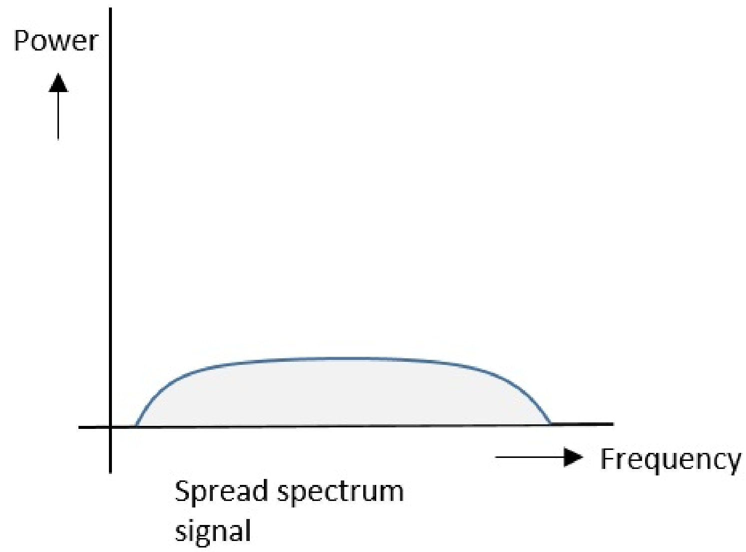

图 2. 扩频信号

它有如下一些特性：

-信号频带占据很宽的频率范围。

-功率密度很低。

-能量分布很广。

从上面的描述中可以看到扩频信号具有很高的抗干扰能力。

3 扩频配置

对于 RT 系列，SYS_PLL2，AUDIO_PLL 和 VIDEO_PLL 支持扩频（向下扩频）。要启用扩频功能，请使用如下扩频软件配置来配置 SDK 中的寄存器。

```
/*
    0x40c84260 is used to configure the value of
    STOP(bit[31-16]) and STEP(bit[14:0]). Bit 8
    is the enable bit.
    The Frequency change is:
        Frequency change = STOP/B *24MHz

    The Step value is :
        The max frequency change for each time = STEP/B * 24Mhz

    0x40c842a0 is used to configure the value of B.

    So that, the following configure is:
    STOP = 0x4B0;
    B = 0x960;
    STEP = 0x6;
    Frequency change = 12MHz
    The max frequency change for each time = 60KHz

    STOP = 0x258;
    B = 0x960;
```

```
    STEP = 0x6;
    Frequency change = 6MHZ

    The max frequency change for each time = 60KHz
*/
    *(uint32_t *)(0x40c84260) = 0x04B08006; //12MHz
    //*(uint32_t *)(0x40c84260) = 0x02588006; //6MHZ
    *(uint32_t *)(0x40c842a0) = 0x00000960;



/*! @brief Spread specturm configure Pll */
typedef struct _clock_pll_ss_config
{
    uint16_t stop; /*!< Spread spectrum stop value to get frequency change. */
    uint16_t step; /*!< Spread spectrum step value to get frequency change step.
 */
} clock_pll_ss_config_t;

/*! @brief PLL configure for Sys Pll1 */
typedef struct _clock_sys_pll1_config
{
    bool pllDiv2En;             /*!< Enable Sys Pll1 divide-by-2 clock or not. */
    bool pllDiv5En;             /*!< Enable Sys Pll1 divide-by-5 clock or not. */
    clock_pll_ss_config_t *ss; /*!< Spread spectrum parameter,
                                  it can be NULL, if ssEnable is set to false */
    bool ssEnable;              /*!< Enable spread spectrum flag */
} clock_sys_pll1_config_t;
```

以下 Phase Locked Loop （PLL） 在 RTXXXX 上支持扩频特性。

表 **1. RT1xxx** 上的 **PLL**

PLL	RT1170	RT1010	RT1015	RT1020/1024	RT1050	RT1060/1064
PLL528	✓	✓	✓	✓	✓	✓
PLL_528_ PFDn	✓	✓	✓	✓	✓	✓
Audio_PLL	✓	NA	NA	NA	NA	NA
Video_PLL	✓	NA	NA	NA	NA	NA
PLL_1G	✓	NA	NA	NA	NA	NA

当使能扩频功能时，需要注意两点：扩频范围和步长。

- 扩频范围是指PLL 向下扩展的频率大小。例如，6 MHz 扩频范围意味着 PLL 的频率将在目标频率和目标频率减 6 MHz 之间反复。
  计算频率范围的公式如下：

$$\text{Range} = \text{STOP}/\text{B} * 24\text{MHz} \tag{1}$$

- 频率步长是指频率变化步长的大小。
  计算频率步长的公式如下：

$$\text{Step} = \text{STEP}/\text{B} * 24\text{MHz} \tag{2}$$

例如PLL528 配置如下：

- STOP = 0x4B0
- B = 0x960
- STEP = 0x6

那么频率范围和步长如下：

- Range: 12 MHz
- Step: 60 kHz

此时 PLL528 将在 528 MHz 和 516 MHz 之间回扫，回扫的步长为 60 KHz。

对 RT10xx 系列产品，STOP, B 及 STEP 可以在 SYS_PLL2_SS 和 SYS_PLL2_MFD 中配置。

对 RT11XX 系列产品，STOP, B 及 STEP 可以在 CCM_ANALOG_PLL_SYS_SS 和 CCM_ANALOG_PLL_SYS_DENOM 中配置。

当初始化PLL 的时候，扩频功能可以同时配置。在代码中填写STOP,B 及STEP 进结构体来初始化PLL。一旦使能PLL，扩频功能同时打开。

4 扩频辐射比较

使用 EVK-MIMRT1170 平台进行此测试。使用非接触式探头和频谱分析仪，在不同配置下对扩频测试辐射值。

根据测试结果，在这种情况下建议使用 6 MHz 和 12 MHz 的停止值，以提高 EMI 性能。

表 **2.** 不同扩频配置下的测试结果

Spread spectrum (Hz)	0.75 M	1.5 M	3 M	6 M	12 M	24 M	-->	6 M and 12 MHz configuration is recommended.
Test result (dBm)	-46.2	-46.56	-49.85	-52.31	-53.35	-54.3		

图 **3. 3 MHz** 配置下的频谱

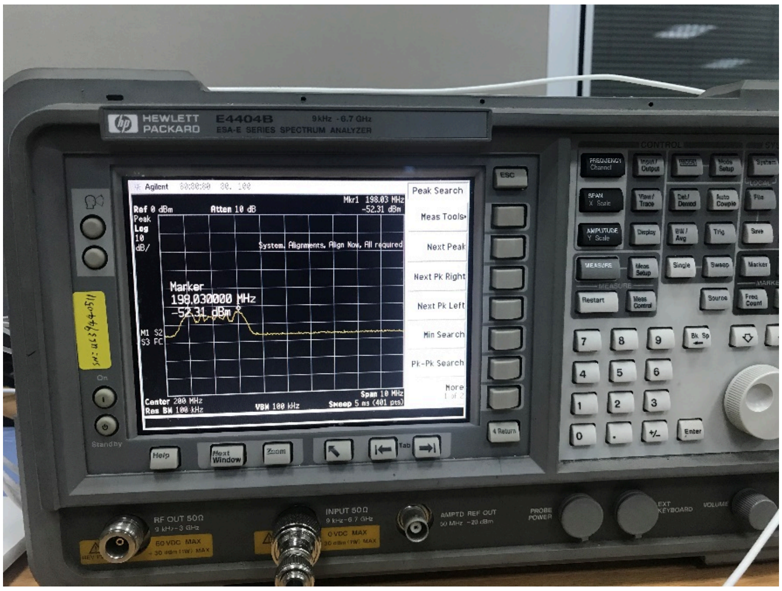

图 **4. 6 MHz** 配置下的频谱

5 频谱扩展下的可靠性测试

Synchronous DRAM（SDRAM）可靠性在 RT1170EVK 平台上启用的频谱扩展下进行了测试。有关测试模式，请参见 表 3。

表 **3.** 测试的基本配置

	Module	**Frequency**
Core	Cortex-M7	996 MHz
AXI to SEMC	32 bit	240 MHz
SEMC	32 bit	198 MHz
SDRAM chip	w9825g6kh	256 Mb/up to 200 MHz
L1 Dcache	Total 32 KB/One-line 32 B	—
Code	Text region in ITCM Data region in DTCM CStack region in DTCM	—

从测试结果来看，6 MHz 和12 MHz 配置都可以通过全温度测试下的压力测试，这意味着为 SDRAM 时钟启用频谱扩展功能非常可靠。

```
DRAM test setting:
                  Base Address: 0x80000000;
                  Test Size: 67108864 Bytes;
                  Test Loop: 1;
                  DRAM Freq: 198010624;
                  Fail Stop: 0;
                  Enable Cache: 0;
                  Core clock: 996056064;
                  AHB clock: 120006784;
                  SEMC clock: 198010624;


memtester version 4.3.0 (32-bit)
Copyright (C) 2001-2012 Charles Cazabon.
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want 64MB (67108864 bytes)
Loop 1/1:
  Stuck Address: ok
  Random Value: ok
  Compare XOR: ok
  Compare SUB: ok
  Compare MUL: ok
  Compare DIV: ok
  Compare OR: ok
  Compare AND: ok
  Sequential Increment: ok
  Solid Bits: ok
  Block Sequential: ok
  Checkerboard: ok
  Bit Spread: ok
  Bit Flip: ok
  Walking Ones: ok
  Walking Zeroes: ok
  8-bit Writes: ok
  16-bit Writes: ok

Done and Passed!
exit_code 0x0
```

图 **5. Reliability test result**

6 频谱扩展下的**SEMC** 时序配置

还需要注意频谱扩展下的 Smart External Memory Controller（SEMC）时序配置，请检查以下几点:

- 为了提高 SDRAM 的稳定性，可以基于工作时钟速度以更大的余量设置 SEMC 时序配置.
- 参考 表 4 所示的 SDRAM 芯片时序要求，可以在 SEMC 寄存器 SDRAMCR1 和 SDRAMCR2 中将 tRC，tRAS，tRP，tRCD，tRW，tRRD 的最小值设置一个或两个以上的周期。例如，标准的 tRC 是 6 个周期（在 166 MHz 时至少为 60 ns），我们可以在频谱扩展模式下将其设置为 7（或 8）个周期。
- 对于 tREF（刷新周期时间），应将其设置为小于最大刷新周期（64 ms）。 这可以在 SEMC 寄存器 SDRAMCR3 中实现。在 NXP SDK 中，tREF 设置为小于最大刷新周期的一半。
- 有关 SEMC 时序的详细配置，请参考 NXP SDK。

表 **4. SDRAM** 设备时序

Symbol	Parameter	Minimum	Maximum	Minimum	Maximum	Unit
t_{RC}	Command period (REF to REF / ACT to ACT)	60	—	60	—	ns
t_{RAS}	Command period (ACT to PRE)	42	100 K	37	100 K	ns

表 **4. SDRAM** 设备时序...续上页

Symbol	Parameter	Minimum	Maximum	Minimum	Maximum	Unit
t_{RP}	Command period (PRE to ACT)	18	—	15	—	ns
t_{RCD}	Active command To read/write command delay time	18	—	15	—	ns
t_{RRD}	Command period (ACT [0] to ACT[1])	12	—	14	—	ns
t_{DPL}	Input data to precharge command delay time	12	—	14	—	ns
t_{DAL}	Input data to active / refresh command delay time (during auto-precharge)	30	—	30	—	ns
t_{MRD}	Mode register program time	12	—	14	—	ns
t_{DDE}	Power down exit setup time	6	—	7	—	ns
t_{XSR}	Exit self-refresh to active time (4)	66	—	70	—	ns
t_T	Transition time	0.3	1.2	0.3	1.2	ns
t_{REF}	Refresh cycle time (8192)					
	$T_a <= 70\ ^oC$ Com.,Ind., A1, A2	—	64	—	64	ms
	$T_a <= 85\ ^oC$,Ind., A1, A2	—	64	—	64	ms
	$T_a <= 85\ ^oC$ A2	—	32	—	32	ms

7 扩频下的性能测试

性能测试是在频谱扩展下进行的，请检查以下测试环境和测试结果。可以得出结论，频谱扩展对 SDRAM 读/写性能影响很小，对应用程序没有影响。

- 项目配置：`sdram_debug`
- SDRAM MPU 配置：non-shareable/cacheable/wb/disable Dcache
- 测试环境：Initial，6 MHz，12 MHz，24 MHz
- 测试结果: 测试几秒钟的 16 KB 和 32 KB 数据写入/读取性能，结果显示读取性能均为 22 MB / s，写入性能如图 10 所示。

表 **5.** 扩频下的 **SDRAM** 性能测试

		Initial	6 M	12 M	24 M
Average write	Perf (MB/s)	693	689	685	677
	Reduction percentage	—	-0.6%	-1.2%	-2.3%

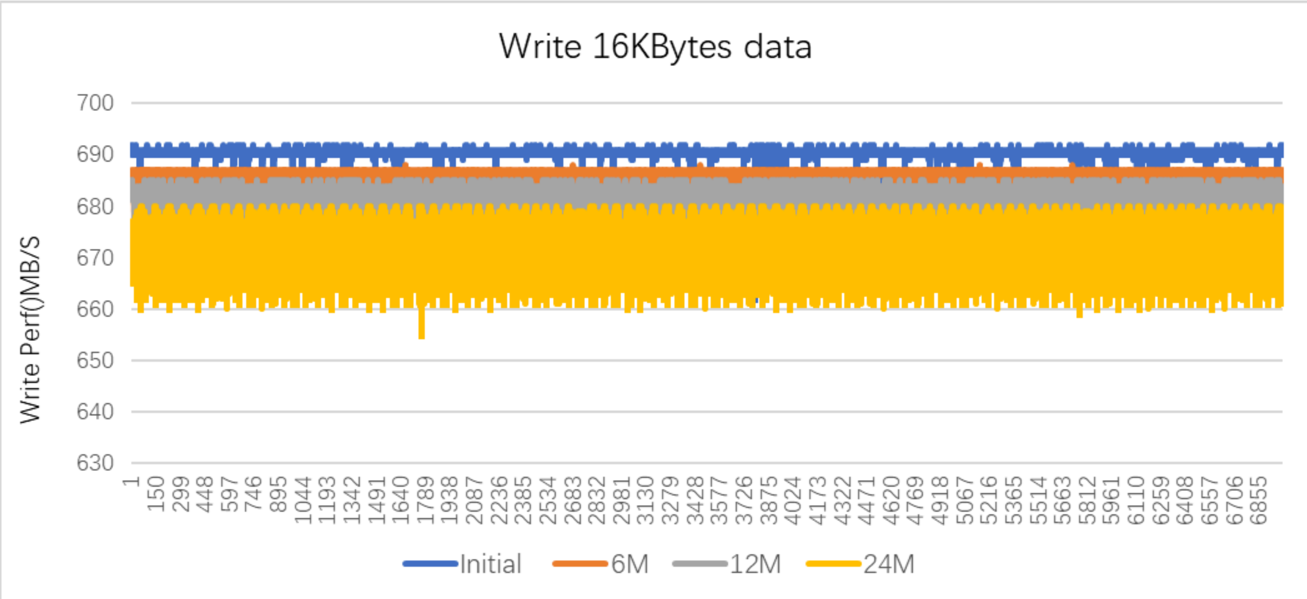

图 **6.** 扩频下的 **SDRAM** 性能测试

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9 修订记录

表 6 汇总了自初始版以来对本文档所做的更改。

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版本号	日期	说明
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0	2020 年 6 月	初次发布

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