AN12239

如何在 i.MX RT 上使用 HyperRAM

Rev. 4 — 29 September 2022 **Application note**

Document information

Information	Content
Keywords	MIMXRT1050 EVKB, HyperRAM, FlexSPI, HyperBus, Memory region and Look-Up-Table, LUT, i.MX RT, i.MX RT Crossover MCUs, System-on-Chip, SoC, application processors
Abstract	本应用笔记描述了如何在i.MXRT 上使用HyperRAM，包括硬件连接，HyperRAM 协议，源代码和性能。

1 简介

i.MX 系列微控制器是 NXP 的跨界产品。它包含一个支持 HyperBus 设备（HyperFlash/HyperRAM）的 FlexSPI 控制器。本应用笔记描述了如何在 i.MX RT 上使用 HyperRAM，包括硬件连接，HyperRAM协议，源代码和性能。

本应用笔记中使用的 SDK 版本是 SDK_2.3.1_EVKB-IMXRT1050。开发环境是 IAR 8.22.1IDE。硬件环境是 MIMXRT1050-EVKB开发板。其中用于示例的 SDK 是 SDK_2.3.1_EVKB- IMXRT1050。HyperRAM 芯片是 Cypress 厂家的 S27KS0641。

2 MIMXRT1050 EVKB 板卡设置

MIMXRT1050-EVKB 板卡上的 FlexSPI 接口默认连接的是 HyperFlash 芯片（Cypress S26KS512SDPBHI02）。因此需要将 HyperFlash 芯片替换成 HyperRAM，如Figure 1所示。

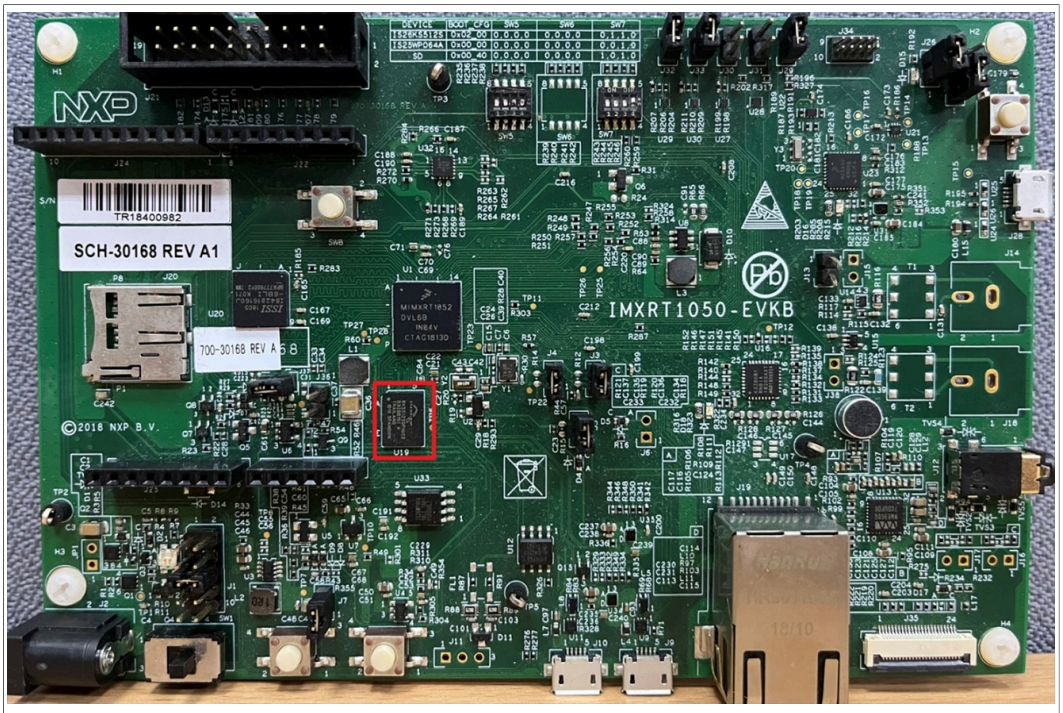

Figure 1. 用 **HyperRAM** 替换 **HyperFlash**

2.1 针对 HyperRAM 的板卡 rework

Cypress S27KS0641 的 HyperRAM 与默认的板载 HyperFlash（CypressS26KS512SDPBHI02）具有相同的封装，除了用 HyperRAM 替换 HyperFlash，还要更改以下硬件：拿掉R425，R426电阻，焊上R424, R427电阻。Figure 2 给出了替换的详细的 PIN 脚图。

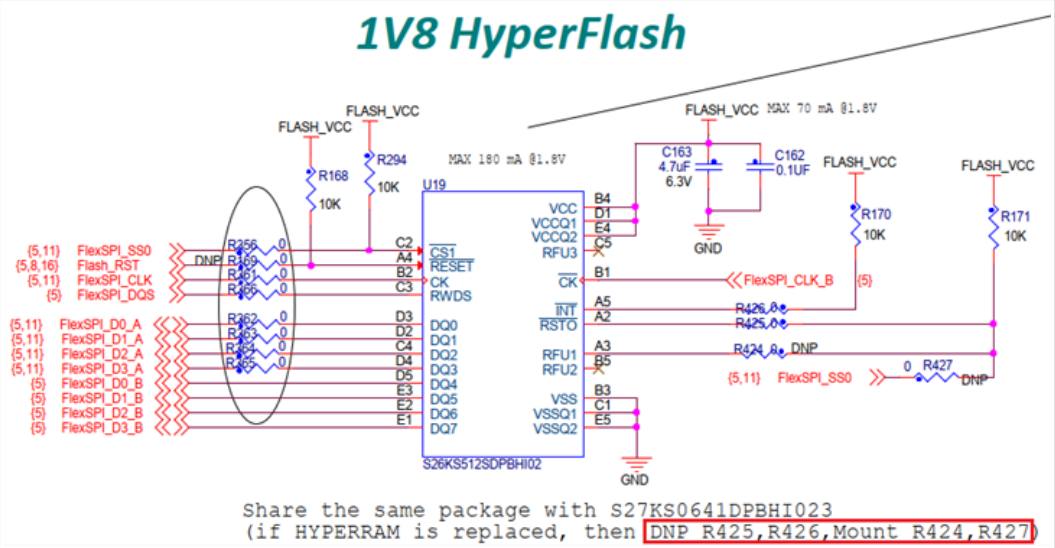

Figure 2. HyperRAM 设备 rework

2.2 HyperRAM 设备

Cypress S27KS0641 HyperRAM 有如下特点:

- 64-Mb (8-MB) 自刷新 DRAM.。
- 3.0-VI/O，11路总线信号（CK）#1.88-VI/O，12路总线信号（差分时钟(ck，CK#)）。
- 1.8-VVCC 时的 166-MHz 时钟速率（333 MB/s）#3.0-VVCC 时的 100-MHz时钟速率（200 MB/s）。
- 双数据速率（DDR）——每个时钟两次数据传输。
- 8 位数据总线（DQ[7:0]）。
- 读写数据选通（RWDS）。
- 顺序突发传输。
- 可配置的突发传输。
- 低功耗模式。

Table 1 描述了 CypressS27KS0641 HyperRAM 的相关信号。

Table 1. S27KS0641 HyperRAM 信号描述

Symbol	Type	Description
CS#	Master Output Slave Input	**Chip Select** Bus transactions are initiated with a HIGH-to-LOW transition. Bus transactions are terminated with a LOW-to-HIGH transition. The master device has a separate CS# for each slave.
CK, CK#	Master Output Slave Input	**Differential Clock** Command, Address, and Data information are output regarding the crossing of the CK and CK# signals. Differential clock is used on 1.8 V I/O devices. **Single Ended Clock** CK# is not used on 3.0 V devices. Only a single ended CK is used. The clock is not required to be free-running.

Table 1. S27KS0641 HyperRAM 信号描述*...continued*

Symbol	Type	Description
DQ[7:0]	Input/Output	**Data Input/Output** Command, Address, and Data information are transferred on these signals during Read and Write transaction.
RWDS	Input/Output	**Read Write Data Strobe** During the Command/Address portion of all bus transactions, RWDS is a slave output. It indicates whether additional initial latency is required. Slave output is during the read data transfer. Data is edge aligned with RWDS. Slave input is during the data transfer in write transactions to function as a data mask. (HIGH = additional latency, LOW = no additional latency)
RESET#	Master Output Slave Input Internal Pull-up	**Hardware RESET** When LOW, the slave device self-initializes and returns to the **Standby** state. Place **RWDS** and **DQ[7:0]** into the HI-Z state when **RESET#** is LOW. The slave **RESET#** input includes a weak pull-up. If **RESET#** is left unconnected, it is pulled up to the HIGH state.
V_{cc}	Power Supply	**Power**
$V_{cc}Q$	Power Supply	**Input/Output Power**
V_{ss}	Power Supply	**Ground**
$V_{ss}Q$	Power Supply	**Input/Output Ground**
RFU	No Connect	**Reserved for Future Use** May or may not be connected internally. The signal/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The signal/ball is used by a signal in the future.

有关 CypressS27KS0641 HyperRAM 的更多信息，请参见数据手册。

3 FlexSPI 控制器和 HyperBus

3.1 FlexSPI 主机控制器

FlexSPI 是一个灵活的 SPI（串行外设接口）主机控制器，支持两个 SPI 通道和最多四个外设。每个通道支持单/双/四线数据传输模式（1/2/4 双向数据线）。i.MX RT1050 通过组合 SIOA[3:0]和 SIOB[3:0]可以支持八线模式。Figure 3给出了 FlexSPI 主机控制器的框图。

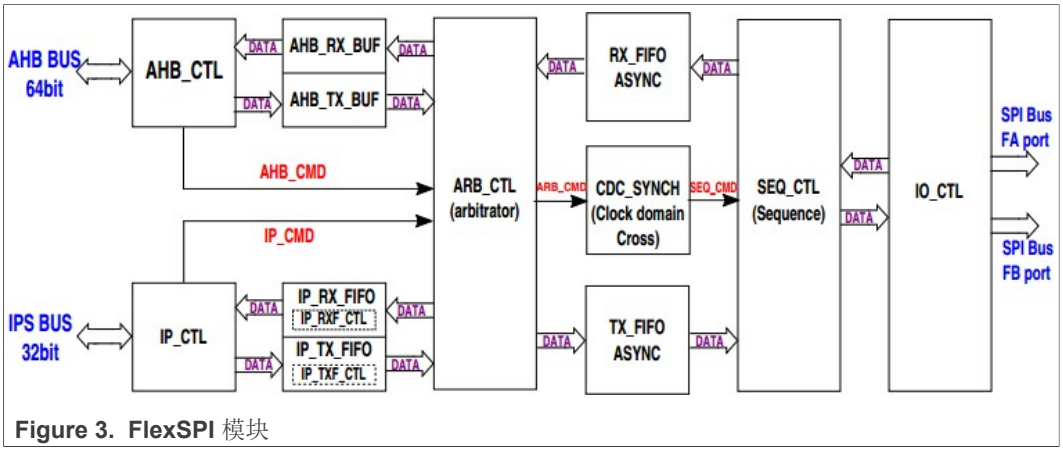

Figure 3. FlexSPI 模块

FlexSPI主机控制器具有以下特点:

- 灵活的序列引擎（LUT表）以支持不同供应商设备。
- Flash 访问模式:单/双/四/八线模式、单倍速率/双倍速率模式、单独/并行模式。
- 读选通时钟采样。
- 通过 AHB总线进行内存映射读/写访问:
  - AHB接收缓冲区用于减少读延迟。AHB接收缓冲区的总大小为 128* 64 位。
  - AHB发送缓冲区用于缓冲一个 AHB突发写传输的所有数据。AHB发送缓冲区大小为 8* 64位。
- 通过 IP总线进行软件触发的 flash读/写访问：
  - IP接收缓冲区用于缓冲来自外设的所有数据。它的大小是 16* 64 位。
  - IP发送缓冲区用于将所有数据缓冲到外设。它的大小是 16* 64 位。

3.2 HyperBus 协议

HyperBus 具有低信号计数和双倍数据速率（DDR）接口，可实现高读写吞吐量，同时减少系统中的设备 I / O 连接数和信号路由拥塞。

HyperBus 接口有如下特点:

- 3.0-VI/O，11路总线信号，单端时钟（CK）。
- 1.8-VI/O，12路总线信号，差分时钟（CK，CK#）。
- 芯片选择（CS#）。
- 8 位数据总线（DQ[7:0]）。
- 读写数据选通（RWDS）。
- 双倍数据速率（DDR）— 每个时钟两次数据传输。
- 在 1.8 V/3.0 VVCC 下，时钟速率高达 200 MHz（400 MHz/s）。
- 顺序突发传输，可配置突发长度。

HyperBus 协议中，前三个时钟周期传输命令/地址（CA0，CA1，CA2，共 48 bit）信息来定义传输特性。 命令/地址信息是以 DDR模式在六个时钟沿进行传输的。Table 2给出了由命令/地址信息定义的传输特性。Figure 4 给出了命令/地址信息的时钟序列。

Table 2. CA 位特性

CA Bit#	Bit name	Bit function
47	R/W#	Identifies the transaction as Read or Write. R/W# = 1 indicates a Read transaction. R/W# = 0 indicates a Write transaction.
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS = 0 indicates the memory space. AS = 1 indicates the register space. The register space is used to access device ID and Configuration registers.
45	Burst Type	Indicates whether the burst is linear or wrapped. Burst Type = 0 indicates wrapped burst. Burst Type = 1 indicates linear burst.
44-16	Row & Upper Column Address	Row & Upper Column component of the target address: System word address bits A31-A3. Any upper Row address bits not used by a particular device density should be set to 0 by the host controller master interface. The size of Rows and therefore the address bit boundary between Row and Column address is slave device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are not cared in current HyperBus devices but set to **0** by the host controller master interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-0 selecting the starting word within a half-page.

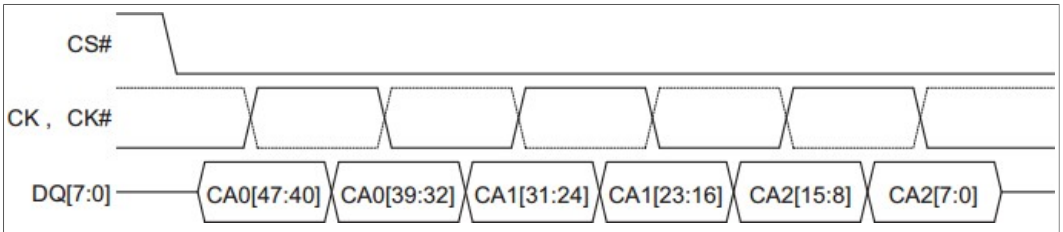

Figure 4. 命令/地址序列

Figure 5和Figure 6显示了具有单个初始延迟的 HyperBus 读/写序列。

具有单个延迟的读取时序如Figure 5所示。

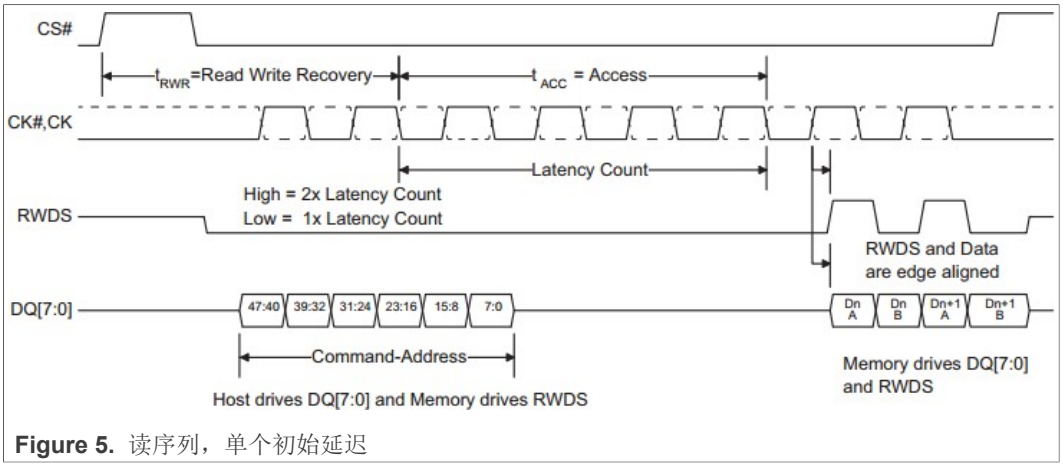

Figure 5. 读序列，单个初始延迟

具有单个延迟的写时序如Figure 6所示。

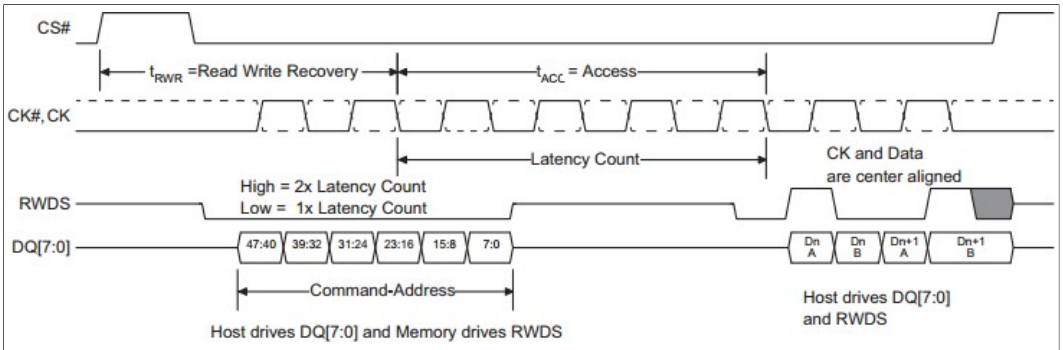

Figure 6. 写序列，单个初始延迟

有关 HyperBus 协议的更多信息，请参见Specifications。

4 内存区域和 LUT (查找表)

i.MXRT1050 中有四个与 FlexSPI 控制器和 HyperRAM 访问相关的关键内存区域。其中最重要的内存区域是 LUT。

4.1 FlexSPI 寄存器内存区

- 基址：0x402A_8000h
- 大小：16 KB

FlexSPI 控制器寄内存区包括所有的配置寄存器。第一步就是在控制器内存区域内设置正确的 FlexSPI 控制器模式、flash参数、AHB/IP模式以及 LUT表等。

4.2 AHB 访问内存区

- 基址：0x6000_0000h
- 大小：512 MB

在 AHB 地址空间 0x60000000~0x8000000 内，可以通过 AHB 总线直接访问 HyperBus 设备。该地址空间映射在 FlexSPI的串行 flash 或 RAM 中。AHB 总线对该地址空间

的访问根据需要触发 flash或 RAM访问命令序列。对于串行 flash/RAM的 AHB读访问，FlexSPI从 flash/RAM获取数据到 AHB 接收缓冲区，然后将数据返回到 AHB 总线。对于串行 flash/RAM 的 AHB 写访问， FlexSPI 从 AHB 总线获取数据缓冲到 AHB 发送缓冲区，然后将其发送给 flash/RAM。除了 FlexSPI 初始化之外，AHB 命令不需要任何软件配置或轮询。

AHB总线访问有如下特征：

- Cacheable和非 Cacheable的读访问。当设置为 Cacheable时，FlexSPI会首先检查读取地址是否命中 AHB 发送缓冲区。
- 可缓冲和不可缓冲的写访问。
- 预取启用/禁用。
- 突发大小：8/16/32/64 位。
- 所有突发类型:SINGLE/INCR/WRAP4/INCR4/WRAP8/INCR8/WRAP16/INCR16

4.3 IP 命令访问内存区域

- IP RX FIFO 基址：
  - 0x402A_8100h – 0x402A_817Ch（IPS 总线）
  - 0x7FC0_0000h – 0x7FC0_007Ch（AHB 总线）
- 大小：128 B

FlexSPI 将从外部设备读取的数据存入 IPRX FIFO 中 。数据可以从上述两个地址空间中读出。

MCR0[ARDPEN] 定义了读取内存空间和方式。

- IP TX FIFO 基址：
  - 0x402A_8180h – 0x402A_81FCh（IPS 总线）
  - 0x7F80_0000h – 0x7F80_007Ch（AHB 总线）
- 大小：128 B

写数据存入 IPTX FIFO，然后通过 IP命令发送到外部设备。数据可以被写入上述两个地址空间中。

MCR0[ATDFEN] 定义了写内存空间和方式。命令访问包含以下关键步骤：

1. 如果是写命令，用写数据填充 IP TX FIFO。
2. 设置 flash/RAM 访问起始地址（IPCR0）、读取/写入数据大小、LUT 序列索引和序列号（IPCR1）。
3. 通过将IPCMD[TRG]位域置**1**来触发flash命令。
4. 轮询 IPCMDDONE 寄存器位，等待 IP 命令完成。

4.4 LUT 内存区域

- 基址：0x402A_8200h
- 大小：256 B

LUT是一个内部存储区域，用于存储多个预编程序列。每个序列最多由八条顺序执行的指令组成。当通过 IP 命令或 AHB 命令触发 flash/RAM 访问时，FlexSPI 控制器根据配置寄

存器中的索引/编号值从 LUT 内存区获取定义的序列，并执行该序列以在 SPI 接口上进行有效的 flash/RAM传输。Figure 7 显示了 LUT 表，序列和指令。

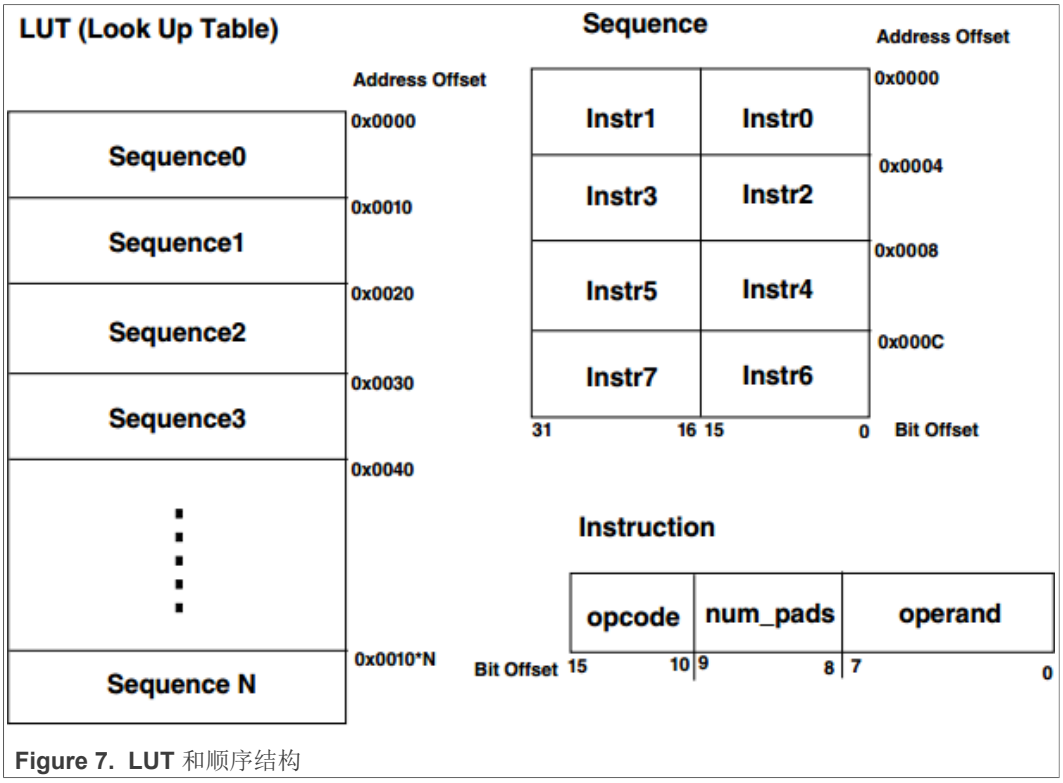

Figure 7. LUT 和顺序结构

更多详细信息，请参见 i.MXRT1050 参考手册的 30.7.8章节（文档 IMXRT1050RM）。

5 源代码和性能

5.1 运行 HyperRAM 例程

HyperRAM 例程源代码基于 i.MXRT1050 SDK V2.3.1。 从 NXP网站下载代码 hyper_ram.zip。

1. 设置硬件环境。
   Rework MIMXRT1050 EVKB 板卡，如Section 2所示，将 Cypress S26KS512SDPBHI02 HyperFlash 更换为 CypressS27KS0641 HyperRAM。然后将 OpenSDA/UART接口连接到主机，并确保它能正常开机。

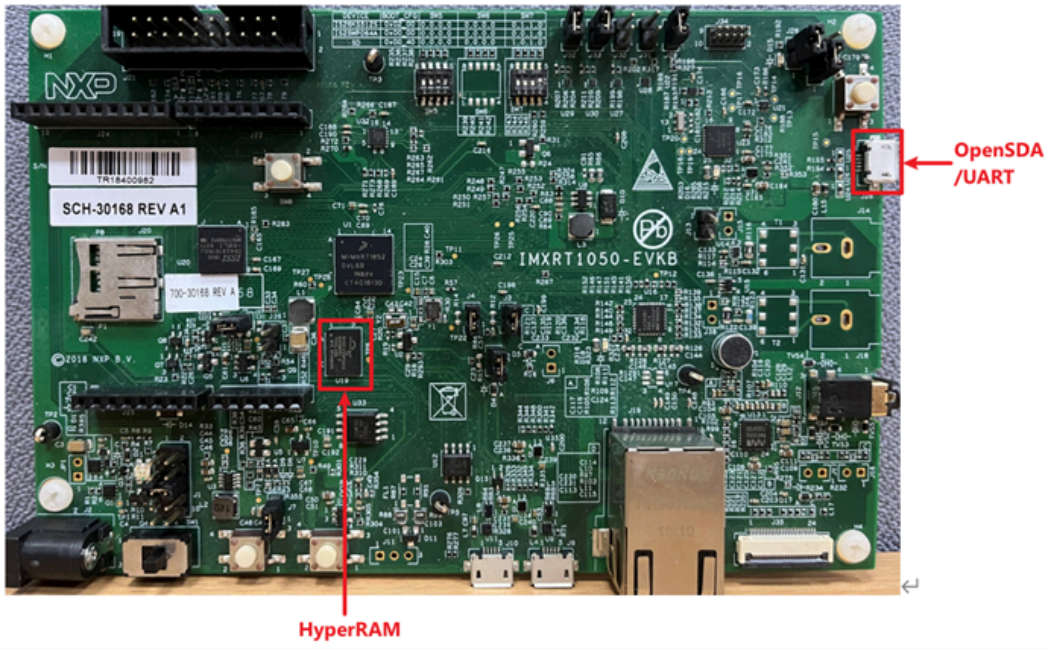

Figure 8. HyperRAM 测试板卡

2. 创建 HyperRAM 工程。
   解压缩 hyper_ram.zip，复制 hyper_ram 文件夹到 SDK_2.3.1_EVKB-IMXRT1050\boards\evkbimxrt1050\driver_examples\flexspi 文件夹中。

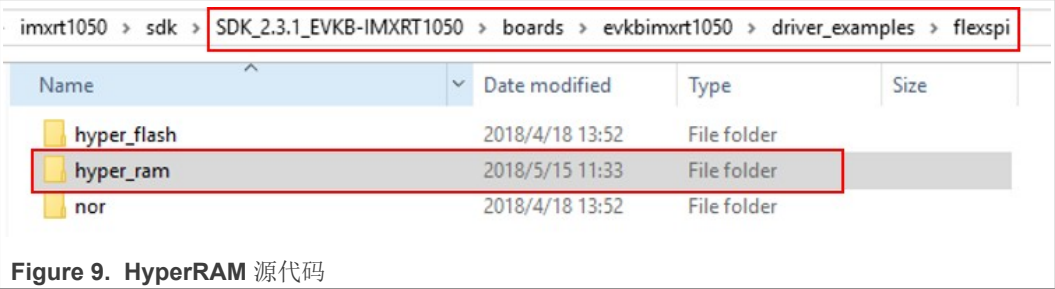

Figure 9. HyperRAM 源代码

3. HyperRAM 例程的主要模块。
   在本例程中，FlexSPI发送数据并操作连接到 FlexSPI接口的外部 HyperRAM设备。首先，该例程实现了 i.MX RT1050 平台的必要配置，并根据 HyperRAM 设备配置了 FlexSPI 控 制器。其次，该例程使用 AHB 和 IP 命令实现了对 HyperRAM 设备

的读/写操作。最后，实现了一个简单的性能测试，结果通过 UART 终端显示。双击 flexspi_hyper_ram_polling_transfer.eww 文件打开 HyperRAM IAR 工程。

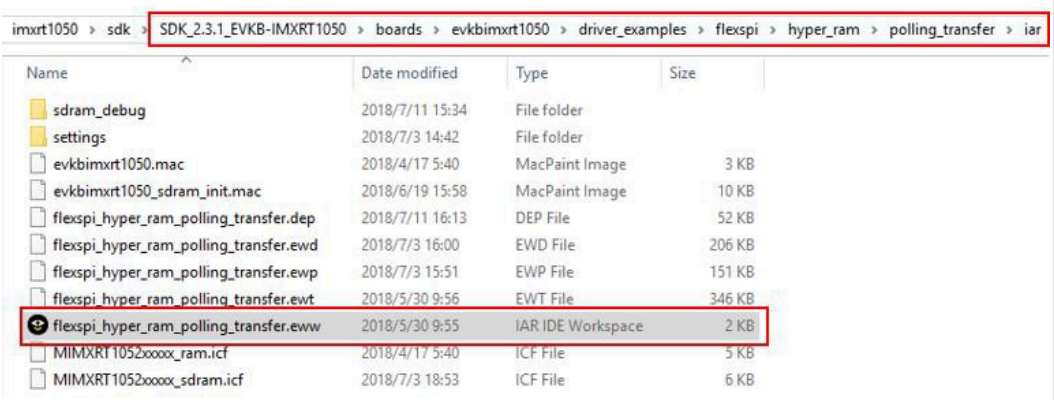

Figure 10. HyperRAM IAR 工程

4. 编译运行例程。

   在主机上找到 MIMXRT1050 EVKB 的 UART端口，打开一个串行终端，并按以下配置进行设置：

   - 115200 波特率。
   - 八个数据位。
   - 无奇偶校验。
   - 一个停止位。
   - 无流控制。

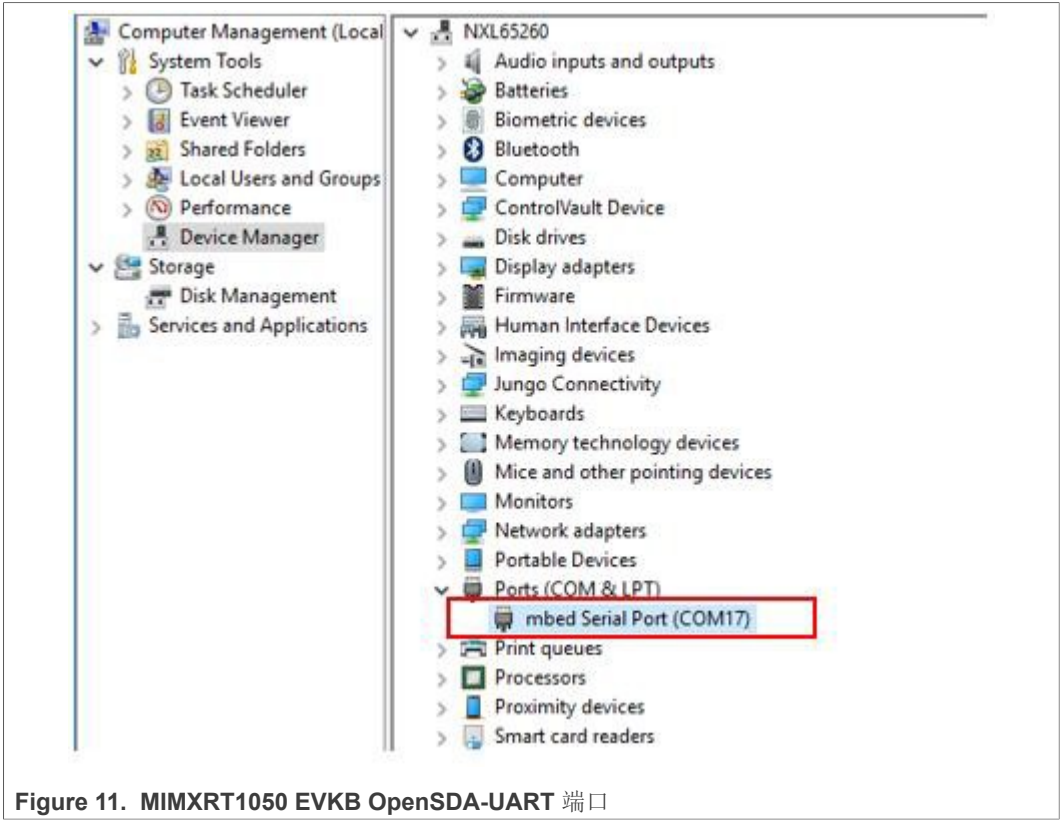

Figure 11. MIMXRT1050 EVKB OpenSDA-UART 端口

5. 将编译优化级别设置为 **None**。

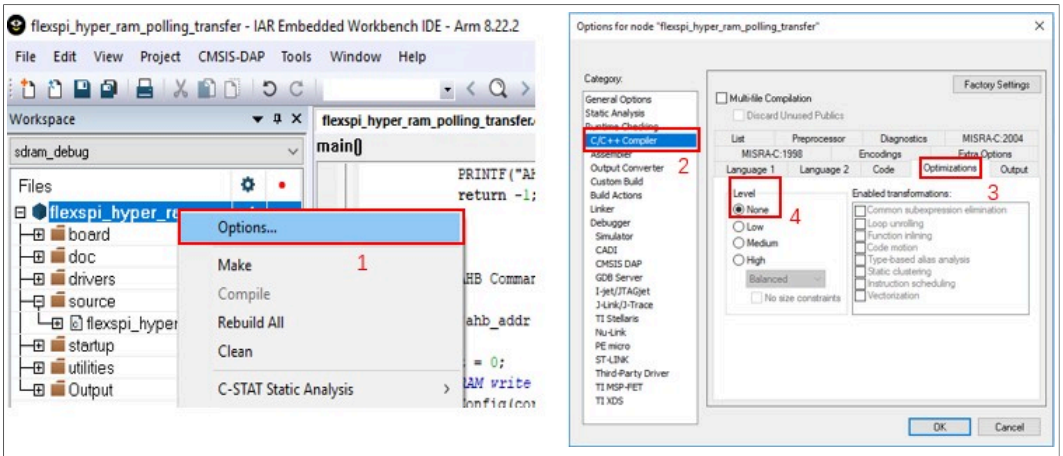

Figure 12. 设置编译优化等级为 **None**

6. 编译、下载和调试。

   如Figure 14所示，串行终端将打印出相关调试信息。

   a. 选择 **debug** 工程，以确保测试数据在 DTCM中，代码在 ITCM中。

   b. 编译工程。

   c. 下载并调试。

   d. 点击 **Go** 运行工程。

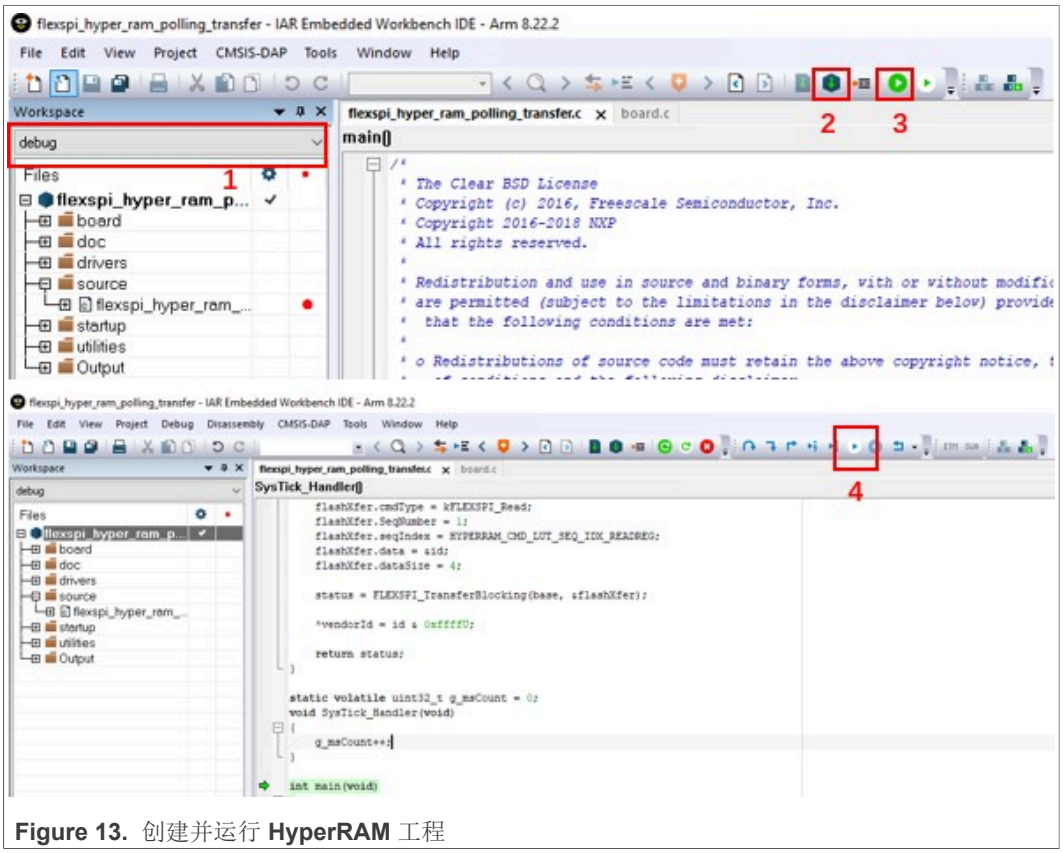

Figure 13. 创建并运行 **HyperRAM** 工程

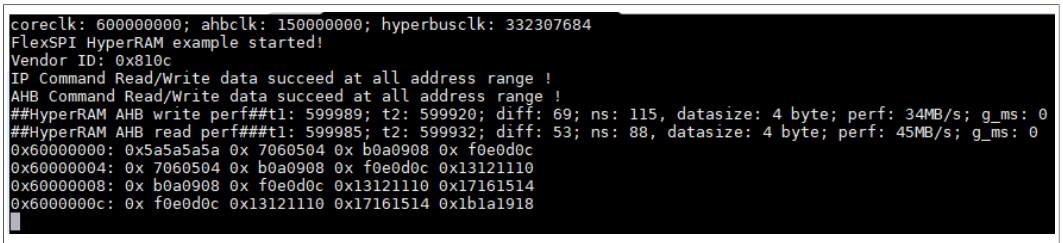

Figure 14. HyperRAM 样本打印演示

5.2 性能分析

上述的 HyperRAM工程包括性能测试。性能测试的相关配置如 Table 3 所示。

Table 3. HyperRAM 测试环境

—	模块	速率
内核	Arm® Cortex®-M7	600 MHz
AHB 到 **FlexSPI**	64-bit	150 MHz
IPS 到 **FlexSPI**	32-bit	150 MHz
HyperRAM 芯片	S27KS0641 @ 1.8 V	166 MHz (332 MB/s)
L1 Dcache	共 32 KB/每行 32 B	—
HyperRAM 空间设置	MPU（内存保护单元） 标准内存类型 Non-shareable/cacheable/wb	—
FlexSPI 控制器设置	读取：启用预期 写入：启用缓冲	—
代码	Text 段在 ITCM 中 Data region in HyperRAM CStack 段在 DTCM 中 启用/禁用 Dcache 关闭编译优化	—

注：HyperRAM工程中的测试用例会相互影响，因此需禁止除目标测试用例以外的其他用例。例如，要测试 HyperRAM 的读性能，则需禁用 AHB 访问验证、IP 访问验证和写性能用例。

性能测试用例有两种设置：**Dcache disable** 和 **Dcache enable**。

- **Dcache disable** 测试了 FlexSPI和 HyperRAM的纯性能。对结果的分析阐明了改善性能和基本配置的机制。
- **Dcache enable** 测试用例展示了如何通过 Dcache提升读取性能，以及为什么性能可以得到如此显著的提升。

根据上述测试用例，可以根据特定用例选择不同的配置。Table 4 和 Figure 15 给出了 **Dcache disable** 时的性能测试结果

Table 4. Dcache disabled 时 HyperRAM 读/写性能

—	Byte	4	8	32	128	512	1024	16 K	32 K
Read	Time (ns)	278	338	696	2140	7896	15576	248876	497730
	Perf (MB/S)	14	23	45	59	64	65	65	65
Write	Time (ns)	115	121	188	1075	4648	9401	152155	304415
	Perf (MB/S)	34	66	170	119	110	108	107	107

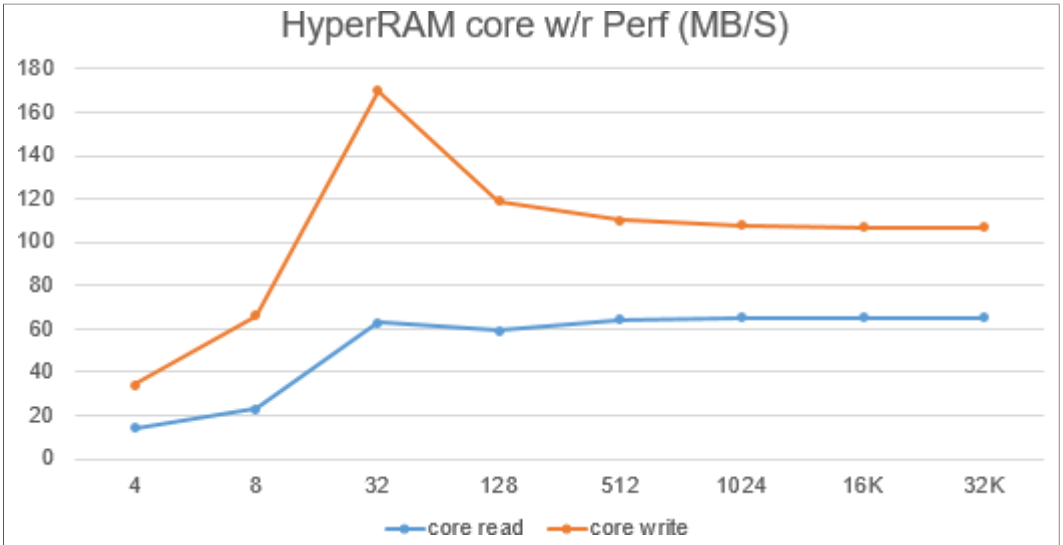

Figure 15. Dcache disabled 时 HyperRAM 性能图

以下分析基于上述性能测试结果：

- 在 MPU模块中定义的 HyperRAM内存空间属性：
  原始的 SDK 代码将 HyperRAM 内存类型设置为“Device”模式。这将限制 AHB 突发写为单一模式，从而导致非常差的写入性能。在 MPU 中将 HyperRAM 内存空间类型更改为“Normal”模式，可以将 AHB 突发写序列发送到 INCR，从而大大提高写性能。在 board.c 文件中：

```
/* Setting Memory with Normal type, not shareable, outer/inner
 write back. */
MPU->RBAR = ARM_MPU_RBAR(2, 0x60000000U);
MPU->RASR = ARM_MPU_RASR(0, ARM_MPU_AP_FULL, 0, 0, 1, 1, 0,
 ARM_MPU_REGION_SIZE_512MB);
```

- 启用 FlexSPI 写访问可缓冲功能：
  FlexSPI 可以选择缓冲 AHB 写入，以便当仲裁授予 AHB 命令时，写入将返回 AHB 总线就绪状态，而不会等待 AHB 命令完成。 使用此功能可提高写性能。
  FlexSPI AHB 发送缓冲区有 64 字节，内部 AHB 可以实现最大 32 字节的突发写访问。因此，当传输 32 字节时，写访问性能更高。
  在 flexspi_hyper_ram_polling_transfer.c 文件中：

```
config.ahbConfig.enableAHBBufferable = true;
```

- 启用 FlexSPI 读访问预取功能：
  启用 FlexSPIAHB 读预取时，FlexSPI将获取比当前 AHB突发所需的更多的 flash/RAM数据。这减少了下一次 AHB 读访问的延迟，提高了读访问性能。

在 flexspi_hyper_ram_polling_transfer.c 文件中：

```
config.ahbConfig.enableAHBPrefetch = true;
```

即使启用了 FlexSPI读预取，读访问性能也不如预期。关键原因是内部 AHB突发读访问无效。禁用 Dcache 将限制 AHB读访问。当使能 Dcache 时，AHB读访问可以在 INCR突发模式下实现，性能会有一定的提高，如 Table 5 和 Figure 16 所示。

在 flexspi_hyper_ram_polling_transfer.c 文件中：

```
/* SCB_DisableDCache(); */
```

Table 5. HyperRAM 在启用 Dcache 的读性能对比

—	Byte	4	8	32	128	512	1024	16 K	32 K
Read (Disable DCache)	Time (ns)	278	338	696	2140	7896	15576	248876	497730
	Perf (MB/S)	14	23	45	59	64	65	65	65
Read (Enable DCache)	Time (ns)	275	285	351	671	1955	3661	58248	116501
	Perf (MB/S)	14	28	91	190	261	279	281	281

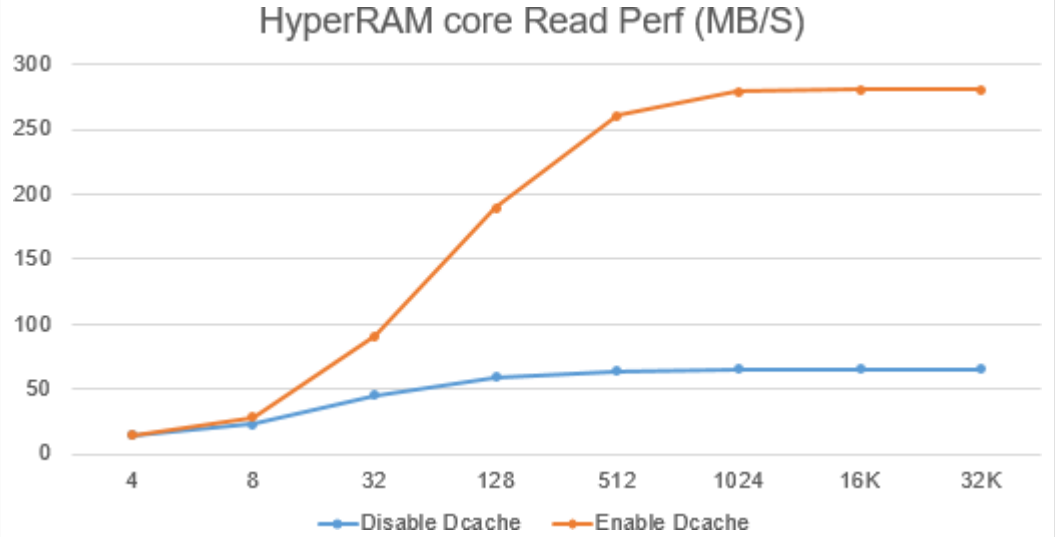

Figure 16. HyperRAM 在启用 Dcache 时的读性能图

6 验证的 HyperRAM 设备

我们在 i.MX RT 系列上压力测试了不同厂商的 HyperRAM 设备。

Table 6 列出了所有 HyperRAM 器件的测试结果。如Table 6 所示，某些 HyperRAM 设备，例如 7KS0641DPHI02，无法通过测试。 因此，在 i.MX RT 系列上使用 HyperRAM 时，建议使用Table 6 中测试通过的设备。

Table 6. HyperRam 设备测试结果

RT Part Number	HyperRAM Vendor	HyperRAM Part Number	Results
PIMXRT1176DVMAA	Cypress	7KL0642DPHB02 (8 MB)	PASS
PIMXRT1064DVL6A	Cypress	7KS0642GAHI02 (8 MB)	PASS
PIMXRT1052DVL6B	Cypress	7KS0641DPHI02 (8 MB)	FAIL
PIMXRT1064DVL6A	Cypress	7KS0641DPHI02 (8 MB)	FAIL
PIMXRT1064DVL6A	Winbond	W956x8MBYA (8 MB)	PASS

Table 6. HyperRam 设备测试结果...*continued*

RT Part Number	HyperRAM Vendor	HyperRAM Part Number	Results
PIMXRT1064DVL6A	ISSI	IS66WVH32M8DALL (32 MB)	PASS
PIMXRT1176DVMAA	ISSI	IS66WVH32M8DALL (32 MB)	PASS

7 总结

本应用笔记描述了如何在 i.MXRT1050 上通过 FlexSPI 接口使用 HyperRAM 设备，提供了例程源代码供进行参考，并根据测试结果分析了 HyperRAM 访问的性能。有关更多详细信息，请参见以下内容：

- i.MX RT1050 参考手册（文档 IMXRT1050RM）
- HyperBus TM Specification Low Signal Count High Performance DDR Bus
- Cypress 上的 S27KS0641 用户手册

8 版本历史

版本号	日期	说明
4	2022年9月29日	• 将 MIMXRT1050 EVK 更新为 MIMXRT1050 EVKB。 • 更新了 Section 2.1 中的描述。 • 更新了 Figure 1，Figure 1，和Figure 8。
3	2021年11月29日	更新了 Section 6
2	2021年5月7日	增加了 Section 6
1	2020年8月	增加了 Section 6
0	2018年8月	首次发布

9 Legal information

9.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

9.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

内容

1 简介 **2**
2 **MIMXRT1050 EVKB** 板卡设置 **2**
2.1 针对 HyperRAM 的板卡 rework 2
2.2 HyperRAM 设备 3
3 **FlexSPI** 控制器和 **HyperBus** **4**
3.1 FlexSPI 主机控制器 4
3.2 HyperBus 协议 5
4 内存区域和 **LUT (**查找表**)** **7**
4.1 FlexSPI 寄存器内存区 7
4.2 AHB 访问内存区 7
4.3 IP 命令访问内存区域 8
4.4 LUT 内存区域 8
5 源代码和性能 **9**
5.1 运行 HyperRAM 例程 9
5.2 性能分析 13
6 验证的 **HyperRAM** 设备 **15**
7 总结 **16**
8 版本历史 **16**
9 **Legal information** **17**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 29 September 2022
Document identifier: AN12239