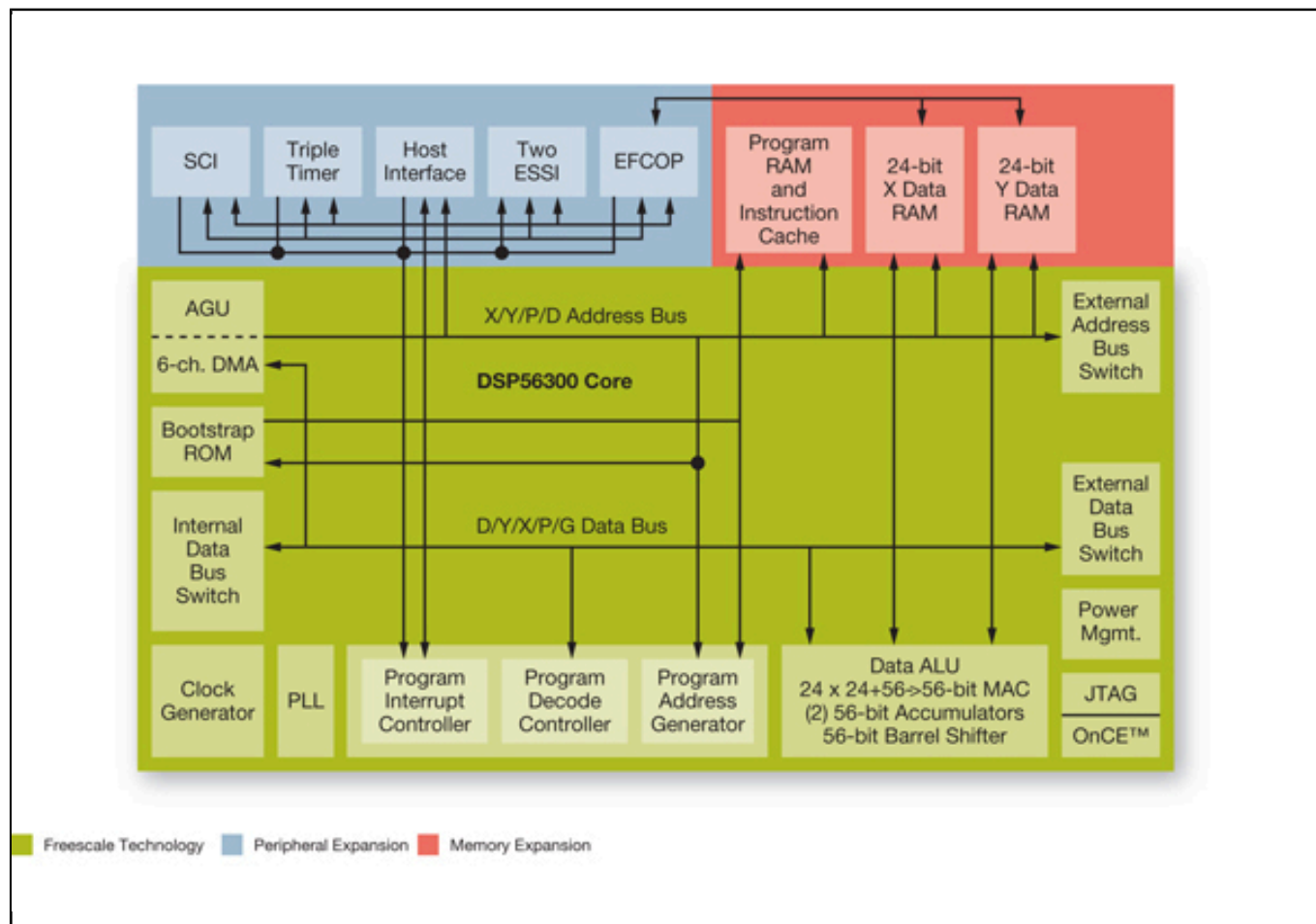# 24-bit General Embedded DSP

DSP56311

Last Updated: Apr 8, 2022

The DSP56311 is designed with developers of multi-channel communication and networking systems in mind. With 300 million multiply accumulates per second (MMACS) operating performance, the 24-bit DSP56311 DSP offers excellent performance density characteristic of DSP56300 devices—maximizing the number of channels processed in a very small space while providing low power dissipation and excellent thermal performance at a competitive price. The DSP56311 maintains compatibility with all other DSP56300 devices, including application code, simulation models and system development tools.

The DSP56311 features the same enhanced filter coprocessor (EFCOP) found on the DSP56L307 to process filter algorithms such as echo cancelling and voice coding to run in parallel with the core. It is ideal for wireless and wireline infrastructure and Internet telephony applications where a single DSP handles several voice and data channels. Additional performance gains can be achieved through the use of the large on-chip RAM, thus reducing wait state penalty incurred when accessing external memory.

The DSP56311 uses split power supplies to separate the input/output (I/O) and peripheral sections, which operate at 3.3 volts, from the processor core, which runs at 1.8 volts. This approach allows the rest of the system to maintain a 3.3-volt external I/O environment while minimizing voltage and power dissipation in the chip internal logic.

DSP56311 Block Diagram Block Diagram

View additional information for 24-bit General Embedded DSP.

Note: The information on this document is subject to change without notice.