Quad GTL/GTL+ to LVTTL/TTL bidirectional non-latched translator

GTL2005PW

Last Updated: Jun 15, 2022

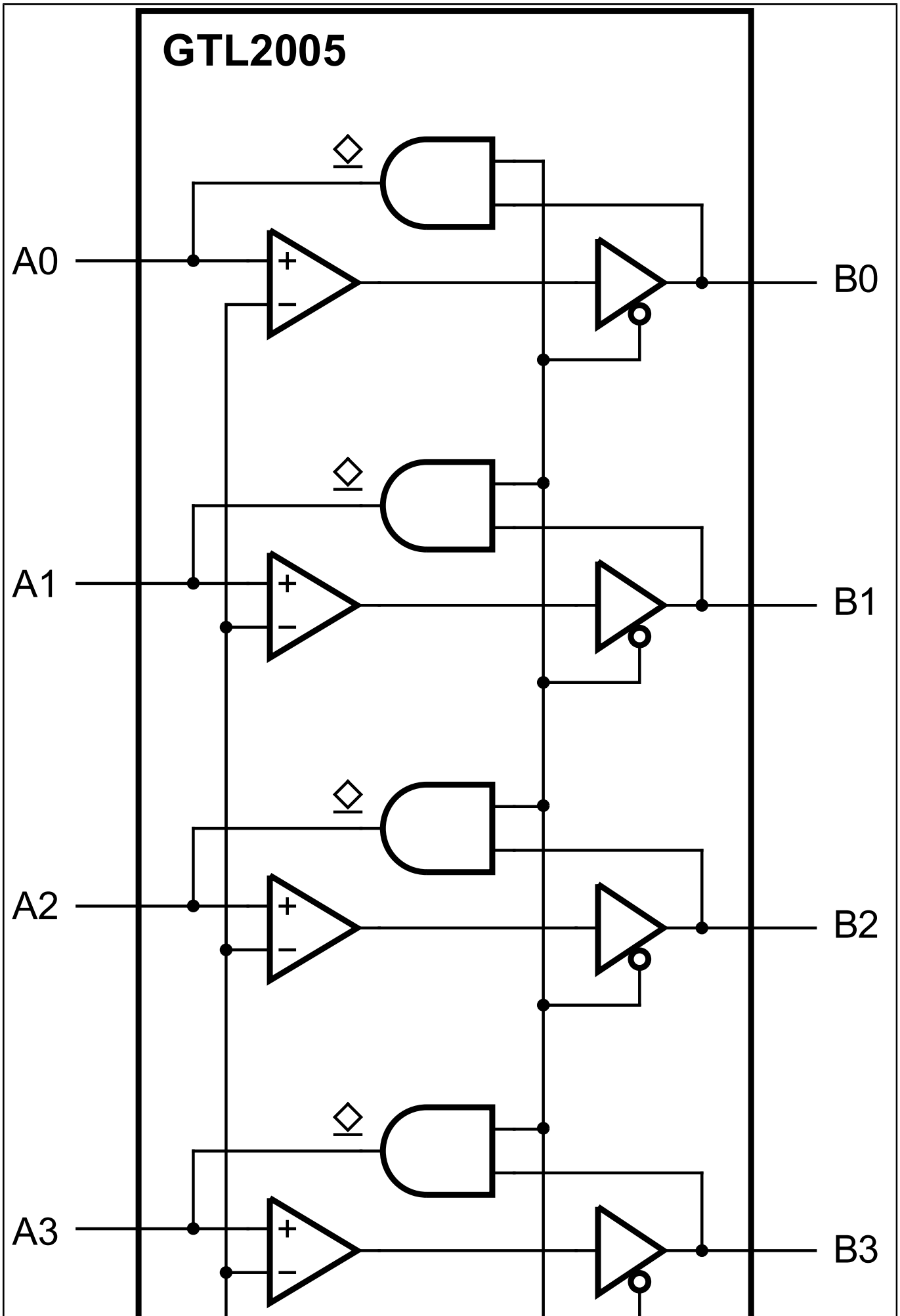
The GTL2005 is a quad translating transceiver designed for 3.3 V system interface with a GTL/ GTL+ bus.

The direction pin (DIR) allows the part to function as either a GTL-to-TTL sampling receiver or as a TTL-to-GTL interface.

The GTL2005 LVTTL interface is tolerant up to 5.5 V allowing direct access to TTL or 5 V CMOS outputs.

The GTL2005 Vref linearity degrades below 0.8 V (see Section 10.1). If the application allows, use the GTL2014, otherwise more closely review noise margins.

GTL2005 Block Diagram Block Diagram


GTL2005
A0
A1
A2
A3
B0
B1
B2
B3

View additional information for Quad GTL/GTL+ to LVTTL/TTL bidirectional non-latched translator.

Note: The information on this document is subject to change without notice.