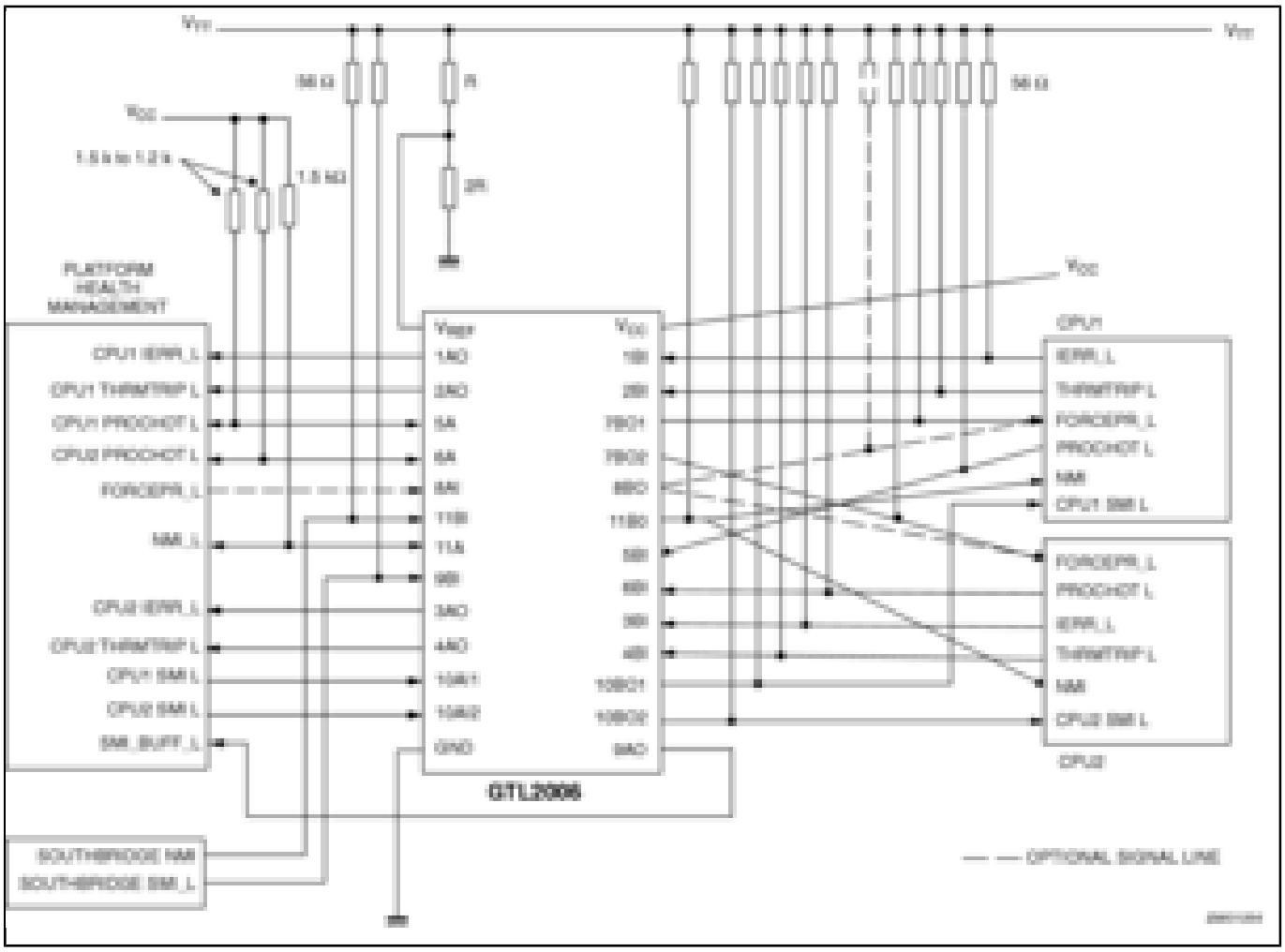
13-Bit GTL-/GTL/GTL+ to LVTTL Translator

GTL2006PW

Last Updated: Jan 20, 2023

The GTL2006 is a 13-bit translator to interface between the 3.3 V LVTTL chip set I/O and the Xeon™processor GTL-/GTL/GTL+ I/O. The GTL2006 is designed for platform health management in dual processor applications.

Block diagram: GTL2006PW Block Diagram



View additional information for 13-Bit GTL-/GTL/GTL+ to LVTTL Translator.

Note: The information on this document is subject to change without notice.