Kinetis® K11-50 MHz, Anti-Tamper Microcontrollers (MCUs) based on Arm® Cortex®-M4 Core

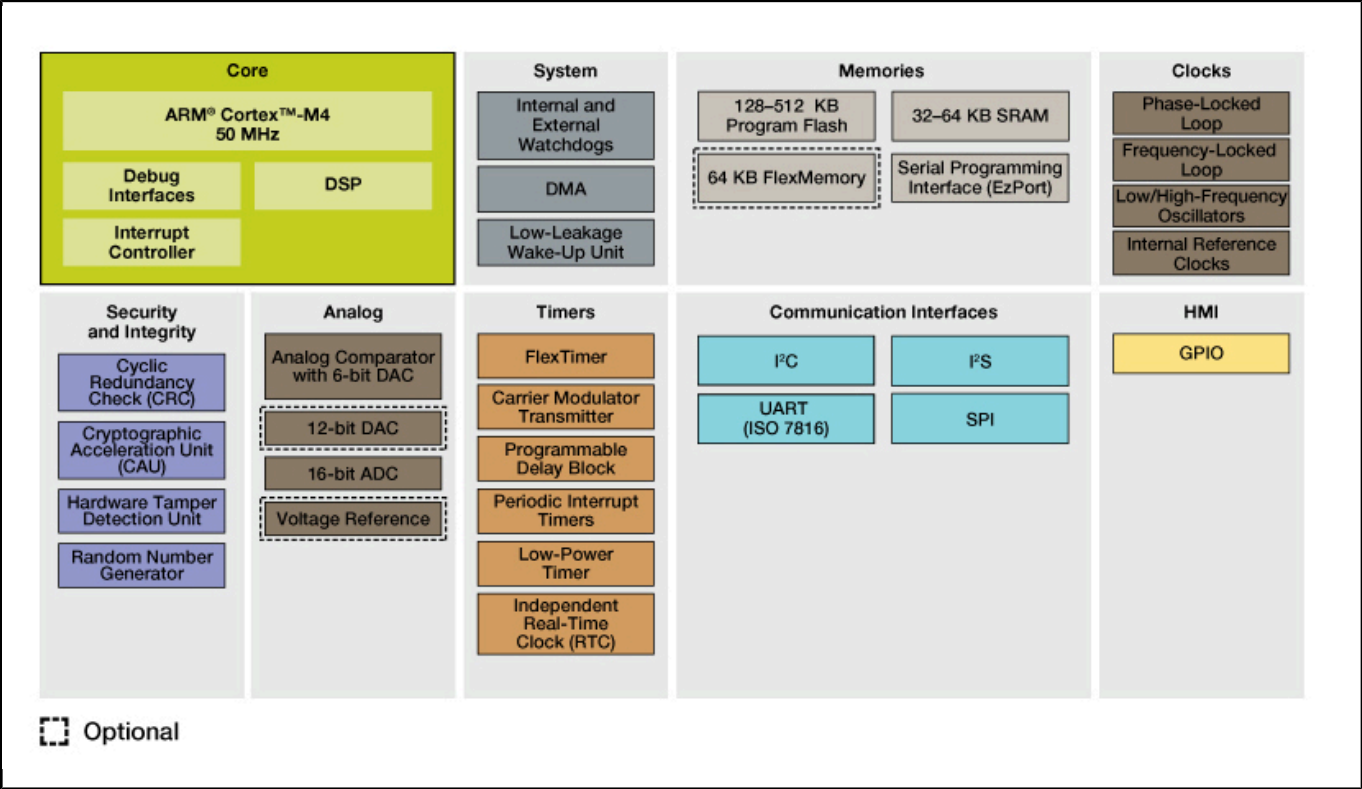## K11_50

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The Kinetis® K11 50 MHz baseline MCUs, built on the Arm® Cortex®-M4 core, are optimized for cost-sensitive applications requiring low-power, security encryption, tamper detection and processing efficiency. This family shares the comprehensive enablement and scalability of the Kinetis portfolio.

Please contact your local NXP representative to download the K11 Security Data sheet and Reference Manual documents (under NDA).

Kinetis K11 50 MHz Baseline MCUs Block Diagram Block Diagram

Core
- ARM® Cortex™-M4 50 MHz
- Debug Interfaces
- DSP
- Interrupt Controller

System
- Internal and External Watchdogs
- DMA
- Low-Leakage Wake-Up Unit

Memories
- 128–512 KB Program Flash
- 32–64 KB SRAM
- 64 KB FlexMemory
- Serial Programming Interface (EzPort)

Clocks
- Phase-Locked Loop
- Frequency-Locked Loop
- Low/High-Frequency Oscillators
- Internal Reference Clocks

Security and Integrity
- Cyclic Redundancy Check (CRC)
- Cryptographic Acceleration Unit (CAU)
- Hardware Tamper Detection Unit
- Random Number Generator

Analog
- Analog Comparator with 6-bit DAC
- 12-bit DAC
- 16-bit ADC
- Voltage Reference

Timers
- FlexTimer
- Carrier Modulator Transmitter
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock (RTC)

Communication Interfaces
- I²C
- I²S
- UART (ISO 7816)
- SPI

HMI
- GPIO

[ ] Optional

View additional information for Kinetis® K11-50 MHz, Anti-Tamper Microcontrollers (MCUs) based on Arm® Cortex®-M4 Core.

Note: The information on this document is subject to change without notice.