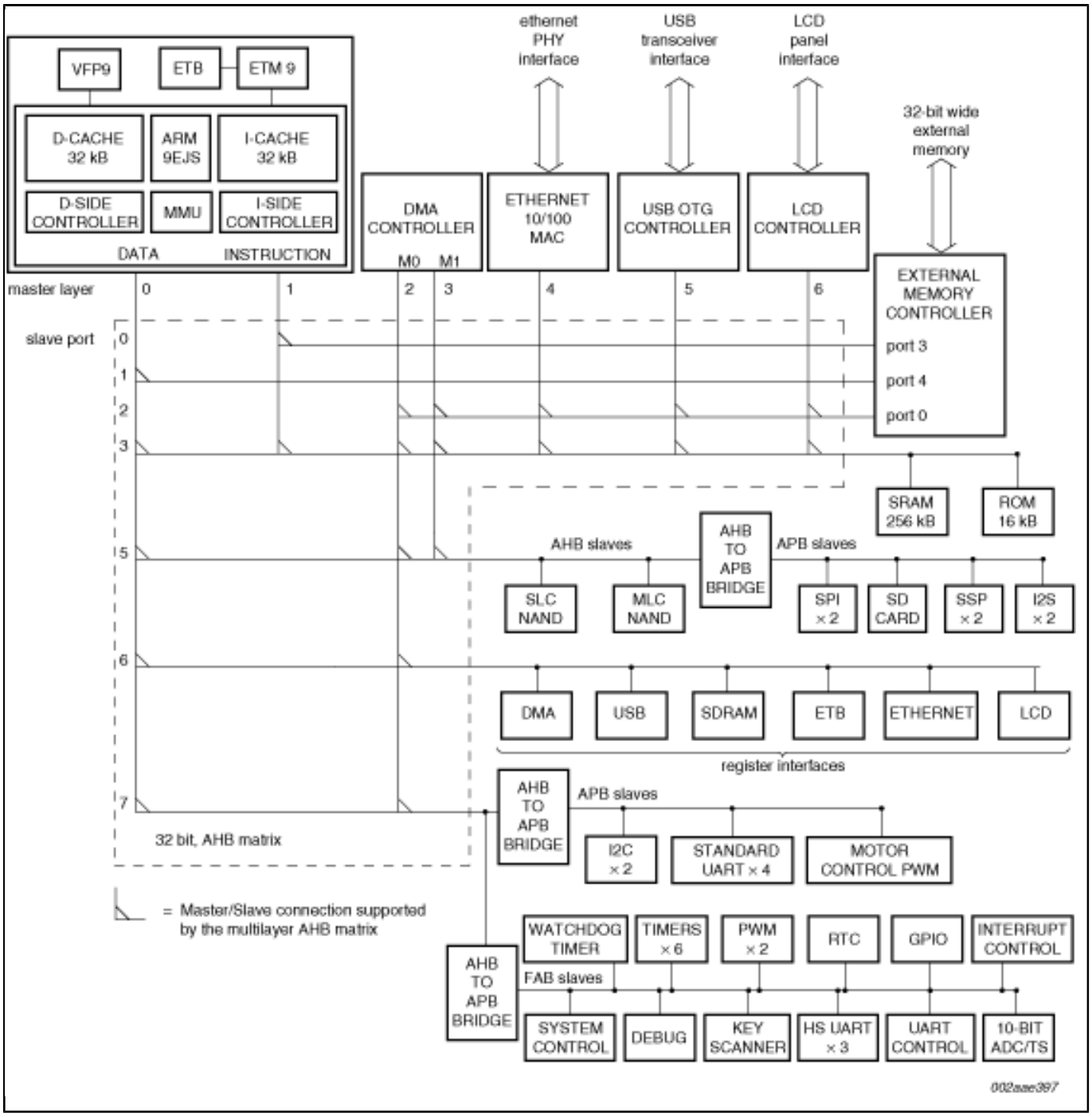
Arm926EJ-S™ with 256 KB SRAM, USB High-Speed OTG, SD/MMC, Nand Flash Controller, Ethernet, LCD Controller

LPC3250FET296

Last Updated: Jan 8, 2026

The LPC3250 operates at CPU frequencies of up to 266 MHz. The NXP® implementation uses an ARM926EJ-S CPU core with a Harvard architectur, 5-stage pipeline, and an integral Memory Management Unit. The LPC3250 also includes 256 kB of on-chip static RAM, a NAND flash interface, an Ethernet MAC, an LCD controller that supports STN and TFT panels, and an external bus interface that supports SDR and DDR SDRAM, as well as static devices. In addition, the LPC3250 includes a USB 2.0 full-speed interface, seven UARTs, two I2C-bus interfaces, two SPI/SSP ports, two I2S-bus interfaces, two single output PWMs, a motor control PWM, six general purpose timers with capture inputs and compare outputs, a Secure Digital interface, and a 10-bit Analog-to-Digital Converter with a touch screen sense option.

Block diagram: LPC3220FET296, LPC3230FET296, LPC3240FET296, LPC3250FET296 Block Diagram



View additional information for Arm926EJ-S™ with 256 KB SRAM, USB High-Speed OTG, SD/MMC, Nand Flash Controller, Ethernet, LCD Controller.

Note: The information on this document is subject to change without notice.

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