

## LPC553x/S3x: Advanced Analog Arm®Cortex®-M33-Based MCU Family

## LPC553x

Last Updated: Dec 24, 2025

The LPC553x/S3x MCU family further expands the general purpose Cortex-M33-based MCU series, offering significant performance enhancement, all on-chip RAM with Parity or ECC, renewed security features and precision analog additions, leveraging the cost-effective 40-nm NVM process technology.

The LPC553x/S3x family includes a proprietary DSP accelerator offering 10x clock cycle reduction, bringing significant signal processing efficiency gains.

## LPC553x/55S3x MCU Block Diagram

|   | Timers                           |                                      |                                       |                   |              |                             |  |
|---|----------------------------------|--------------------------------------|---------------------------------------|-------------------|--------------|-----------------------------|--|
| Arm® Cortex®-M33<br>Up to 150 MHz<br>TrustZone, MPU, FPU, SIMD, DSP                     |                                  |                                      | 5 x 32b Timers                        |                   | SCTimer/PWM  |                             |  |
|   |                                  |                                      | Multi-Rate Timer                      |                   | Windowed WDT |                             |  |
| DSP Accelerator<br>(PowerQuad)  |                                  |                                      | RTC                                   |                   | Micro Timer  |                             |  |
| System Control  |                                  |                                      | OS Event Timer                        |                   |              |                             |  |
| Power Control   |                                  |                                      | Interfaces                            |                   |              |                             |  |
| Single V <sub>dd</sub> power supply, POR, BOD, reduced power modes – DC converter + LDO |                                  |                                      | 8 x FlexComm<br>Supports UART, SPI, F | 8 x FlexComm      |              | FlexSPI<br>B CACHE + PRINCE |  |
| Clock Generation Unit<br>FROs, 2x PLLs, XTAL32k/32m, Clock Out                          |                                  |                                      | HS LSPI                               |                   |              | FS USB + PHY                |  |
| Secure Secure   |                                  | Secure                               | 13C                                   |                   | DMIC         |                             |  |
| DMA0  | DMA1                             | AHB Bus                              | CAN-FD                                | CAN-FD            |              | Flex-PWM                    |  |
| Memory  |                                  |                                      | Security                              |                   |              |                             |  |
| Flash and Flash Cache<br>256 KB w Cache 8 KB  |                                  | ROM<br>Boot + Secure Boot (LPC55S3x) | AES-256                               | Code WDG          |              | DICE + UUID                 |  |
| <b>RAM</b><br>112 KB Parity + 16 KB ECC   | SC .                             |                                      | SRAM PUF                              | SHA-512           |              | Tamper Detect and Response  |  |
| Analog  |                                  |                                      | Debug Auth.                           | PRINCE            |              | PKC                         |  |
| 4x ADC 16b 2MSPS  |                                  | 4x CMP                               | PFR + OTP                             | RNG               |              | ECC                         |  |
| 3x DAC 12b 1MSPS  | 3x DAC 12b 1MSPS 2x Temp Sensors |                                      | Motor Control Subsystem               |                   |              |                             |  |
| 3x OpAMP + 1x VREF  |                                  |                                      | 2x FlexPWM Time                       | 2x FlexPWM Timers |              | 2x QEIs, 2x AOI             |  |

View additional information for LPC553x/S3x: Advanced Analog Arm®Cortex®-M33-Based MCU Family.

Note: The information on this document is subject to change without notice.

## www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.