Low-Power PowerQUICC® II Pro Processor with DDR2, TDM, PCI, Security, USB, QUICC Engine® with UTOPIA

MPC8323E

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The MPC8323E PowerQUICC® II Pro family includes the MPC8323E, MPC8323, MPC8321E and MPC8321. This cost-effective communications processor family meets the requirements of several small office/home office (SOHO), access, IP service and industrial control applications. It provides better CPU performance, additional functionality and faster interfaces than current PowerQUICC II processors while addressing important time to market, price, power consumption and board real estate requirements

Core Complex The MPC8323E incorporates a unique configuration of the e300c2 (MPC603e-based) core. While this version of e300 core does not have a floating point unit (FPU), it has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in significant performance improvement. The core also includes 16 KB of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a flexible local bus and a 32-bit DDR-1/DDR-2 SDRAM memory controller.

QUICC Engine® Technology A new single-reduced instruction set computing (RISC) version of the QUICC Engine communications engine forms the heart of the networking capability of the MPC8323E. The QUICC Engine block contains several peripheral controllers and a single 32-bit RISC controller. Unique microcode packages provide support for network address port translation (NAT), firewall, IPsec, and advanced quality of service (QoS). Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Each of the five UCCs can support a variety of communication protocols:

- 10/100 Mbps Ethernet
- Asynchronous transfer mode (ATM) support up to OC-3 speeds
- Serial ATM
- Multi-physical layer (PHY) ATM
- High-level data link control (HDLC)
- Time division multiplexing (TDM)

- Binary synchronous communications protocol (BISYNC)
- UCC can also support USB 2.0 (full/low-speed).

In addition, the QUICC Engine can also support a universal test and operations PHY interface for ATM (UTOPIA) level 2 for up to 31 multi-PHY.

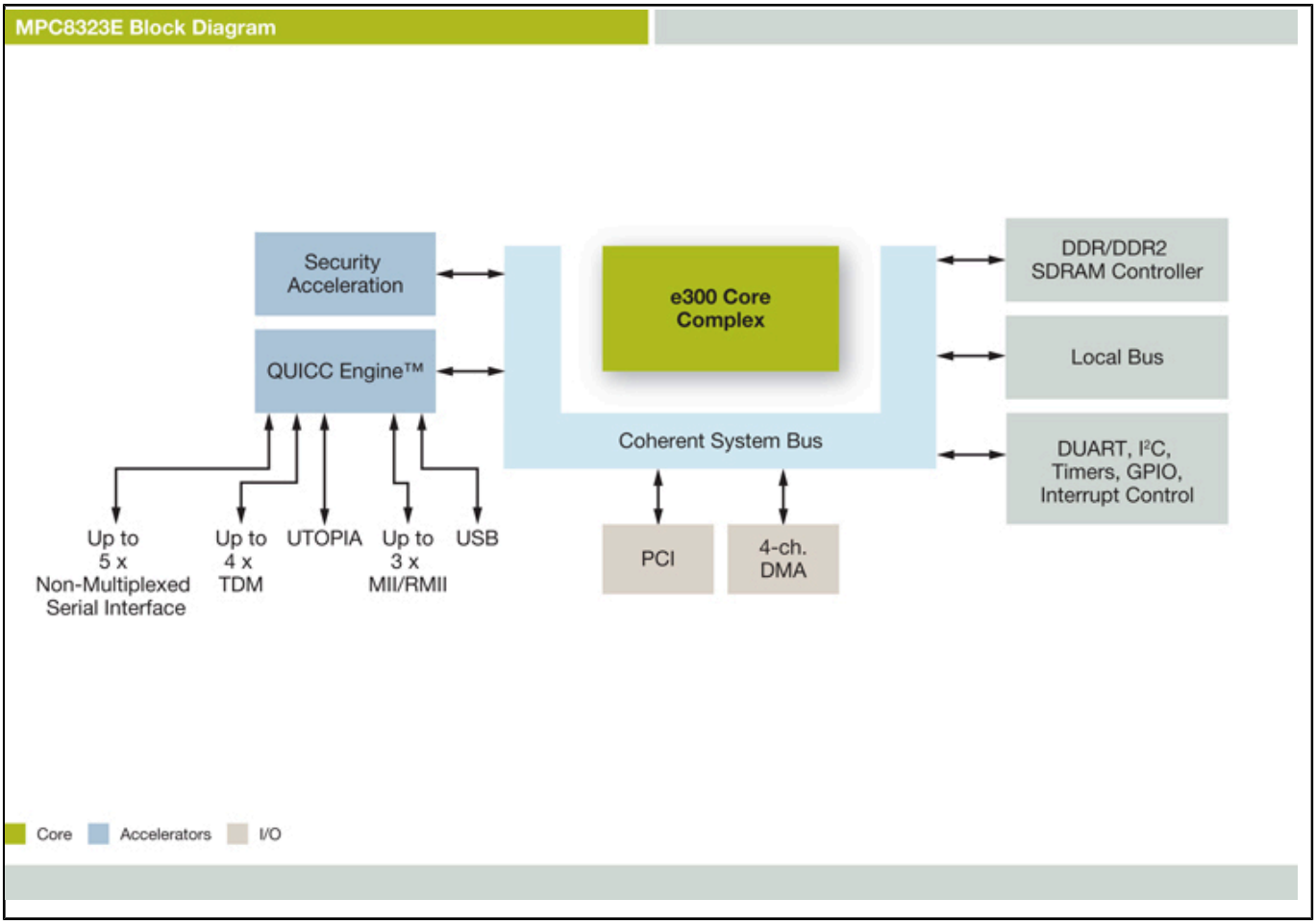
Hardware Security Engine The security engine (SEC 2.2) on the MPC8323E and MPC8321E allows CPU-intensive cryptographic operations to be off-loaded from the main CPU core. The security-processing accelerator provides hardware acceleration for DES, 3DES, advanced encryption standard (AES), secure hash algorithm (SHA)-1 and MD-5 algorithms.

System Interface Unit The MPC8323E family also includes a 32-bit double data rate (DDR)-1/ DDR/2 memory controller, a 32-bit peripheral component interconnect (PCI) controller, a 16-bit local bus and four direct memory access (DMA) channels

Typical Applications

- Residential gateways
- SOHO networking
- VPN routers
- Access points
- DSLAM line cards
- Industrial control
- Test and measurement equipment

NXP PowerQUICC MPC8323E Communications Processor Block Diagram Block Diagram



View additional information for Low-Power PowerQUICC® II Pro Processor with DDR2, TDM, PCI, Security, USB, QUICC Engine® with UTOPIA.

Note: The information on this document is subject to change without notice.