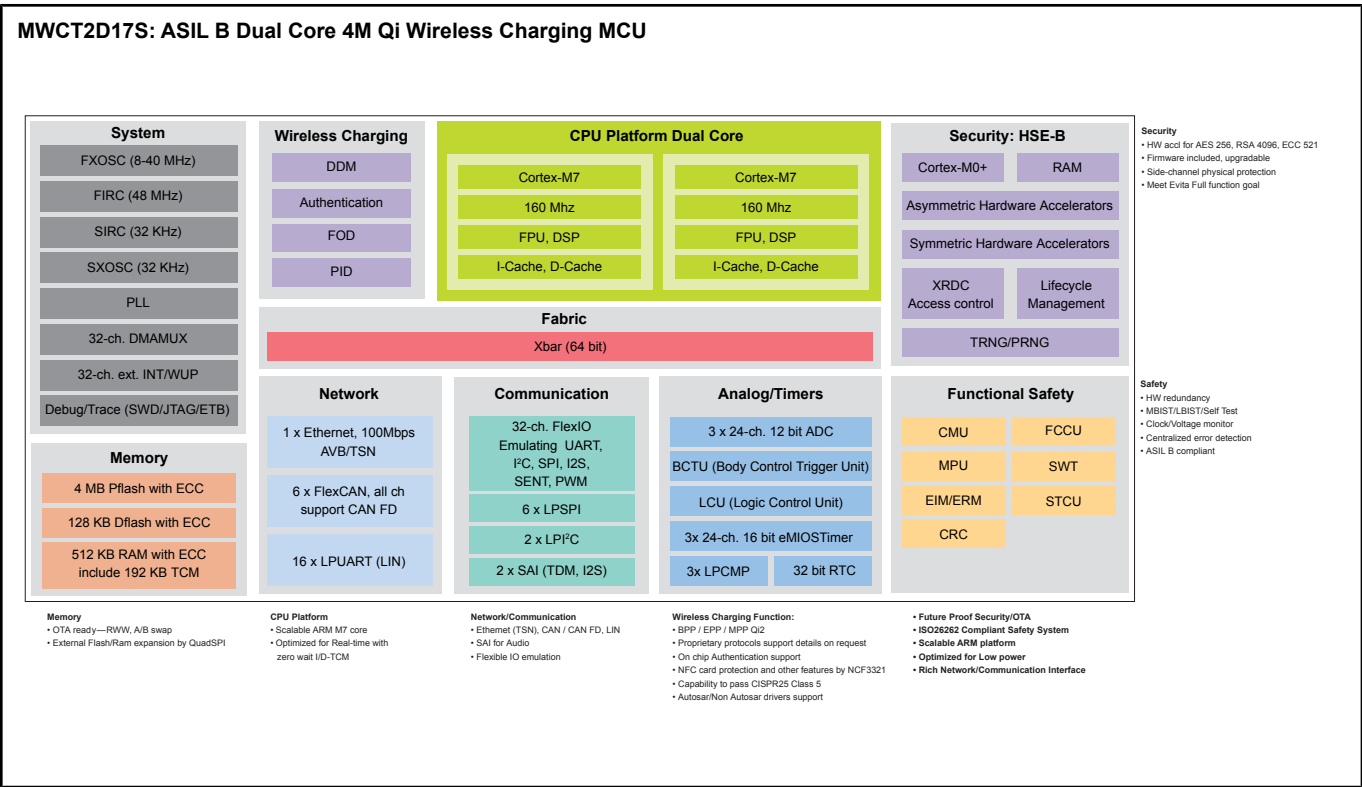# MWCT2xxxS Microcontroller for Wireless charging Transmitter ICs
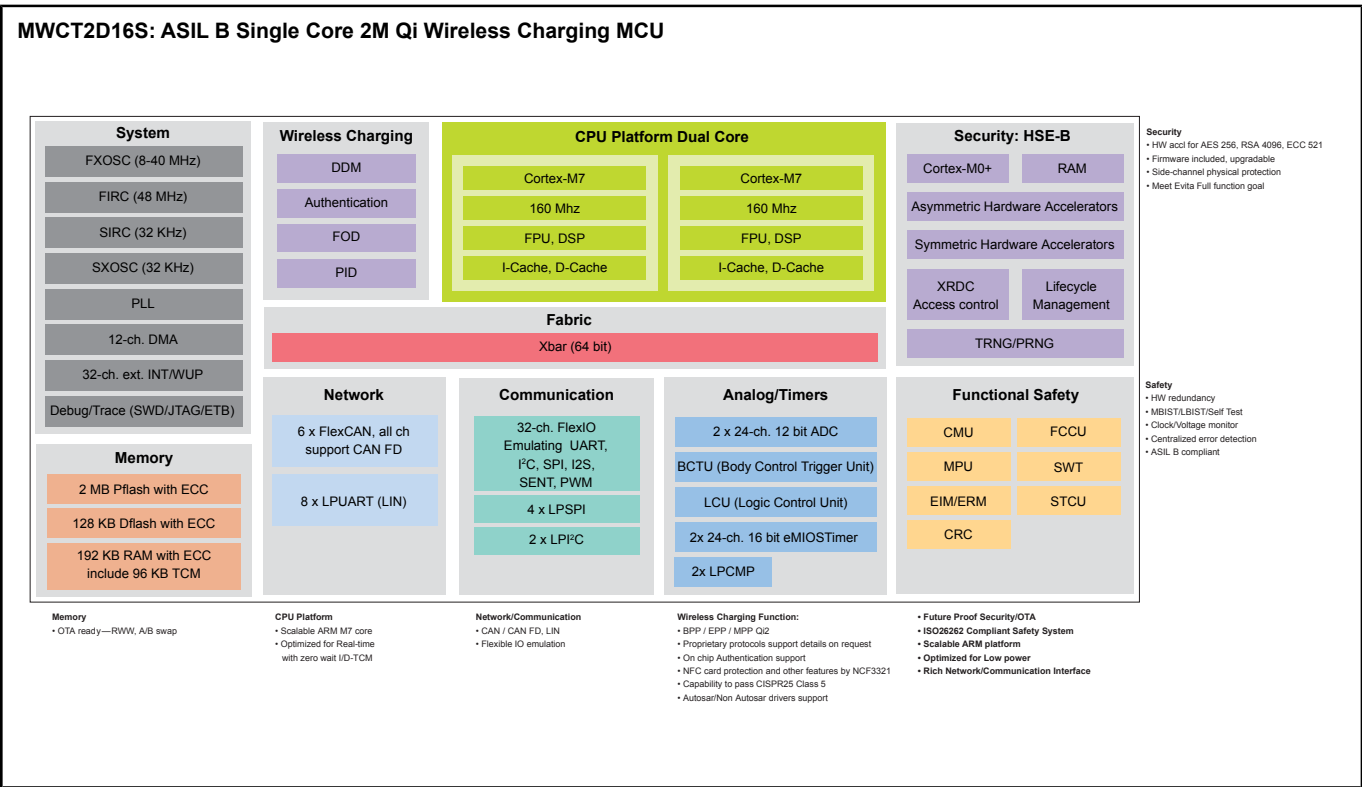
MWCT2xxxS

Last Updated: Jun 26, 2025

The NXP MWCT2xxxS multi-coil wireless charging transmitter ICs provide complete controller functionality with AUTOSAR® SW to implement a wireless charging transmitter solution in an automotive environment. With integrated security element and dual core is perfect solution for QI 2.x application

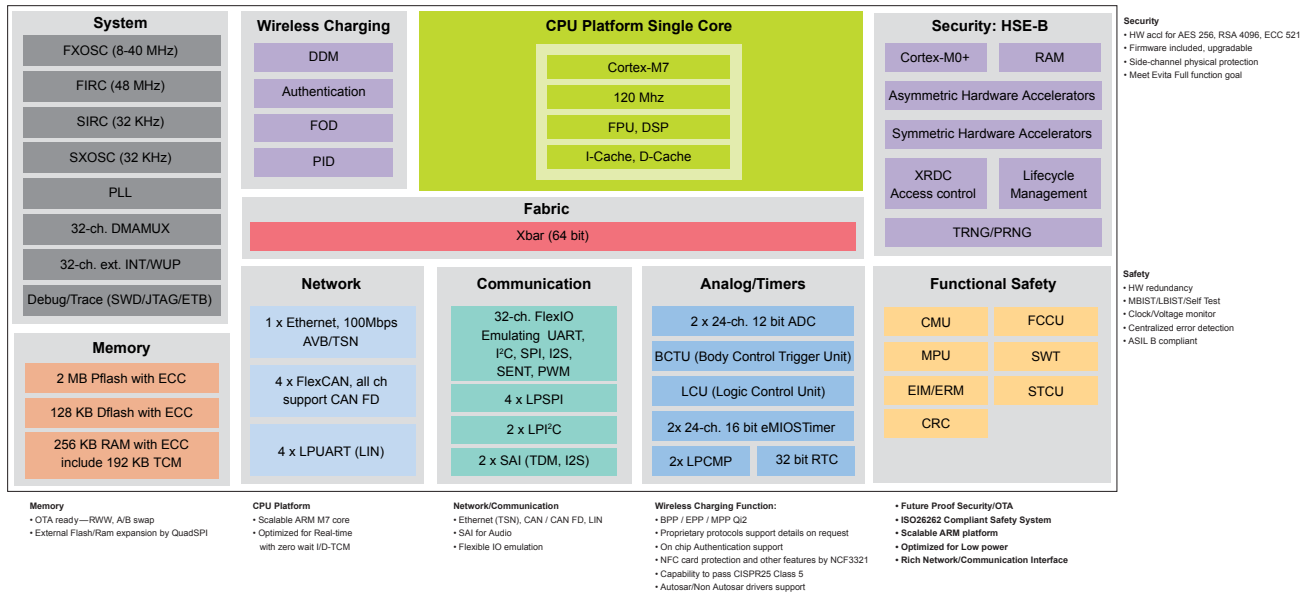# MWCT2D17S: ASIL B Dual Core 4M Qi Wireless Charging MCU Block Diagram

MWCT2D17S: ASIL B Dual Core 4M Qi Wireless Charging MCU

System
- FXOSC (8-40 MHz)
- FIRC (48 MHz)
- SIRC (32 KHz)
- SXOSC (32 KHz)
- PLL
- 32-ch. DMAMUX
- 32-ch. ext. INT/WUP
- Debug/Trace (SWD/JTAG/ETB)

Memory
- 4 MB Pflash with ECC
- 128 KB Dflash with ECC
- 512 KB RAM with ECC include 192 KB TCM

Wireless Charging
- DDM
- Authentication
- FOD
- PID

CPU Platform Dual Core
Cortex-M7	Cortex-M7
160 Mhz	160 Mhz
FPU, DSP	FPU, DSP
I-Cache, D-Cache	I-Cache, D-Cache

Fabric
Xbar (64 bit)

Network
- 1 x Ethernet, 100Mbps AVB/TSN
- 6 x FlexCAN, all ch support CAN FD
- 16 x LPUART (LIN)

Communication
- 32-ch. FlexIO Emulating UART, I²C, SPI, I2S, SENT, PWM
- 6 x LPSPI
- 2 x LPI²C
- 2 x SAI (TDM, I2S)

Analog/Timers
- 3 x 24-ch. 12 bit ADC
- BCTU (Body Control Trigger Unit)
- LCU (Logic Control Unit)
- 3x 24-ch. 16 bit eMIOSTimer
- 3x LPCMP
- 32 bit RTC

Security: HSE-B
Cortex-M0+	RAM
Asymmetric Hardware Accelerators	
Symmetric Hardware Accelerators	
XRDC Access control	Lifecycle Management
TRNG/PRNG	

Functional Safety
CMU	FCCU
MPU	SWT
EIM/ERM	STCU
CRC	

Security
- HW accl for AES 256, RSA 4096, ECC 521
- Firmware included, upgradable
- Side-channel physical protection
- Meet Evita Full function goal

Safety
- HW redundancy
- MBIST/LBIST/Self Test
- Clock/Voltage monitor
- Centralized error detection
- ASIL B compliant

Memory
- OTA ready—RWW, A/B swap
- External Flash/Ram expansion by QuadSPI

CPU Platform
- Scalable ARM M7 core
- Optimized for Real-time with zero wait I/D-TCM

Network/Communication
- Ethernet (TSN), CAN / CAN FD, LIN
- SAI for Audio
- Flexible IO emulation

Wireless Charging Function:
- BPP / EPP / MPP Qi2
- Proprietary protocols support details on request
- On chip Authentication support
- NFC card protection and other features by NCF3321
- Capability to pass CISPR25 Class 5
- Autosar/Non Autosar drivers support

- **Future Proof Security/OTA**
- **ISO26262 Compliant Safety System**
- **Scalable ARM platform**
- **Optimized for Low power**
- **Rich Network/Communication Interface**

MWCT2D16S: ASIL B Single Core 2M Qi Wireless Charging MCU Block Diagram

MWCT2D16S: ASIL B Single Core 2M Qi Wireless Charging MCU

System
- FXOSC (8-40 MHz)
- FIRC (48 MHz)
- SIRC (32 KHz)
- SXOSC (32 KHz)
- PLL
- 12-ch. DMA
- 32-ch. ext. INT/WUP
- Debug/Trace (SWD/JTAG/ETB)

Memory
- 2 MB Pflash with ECC
- 128 KB Dflash with ECC
- 192 KB RAM with ECC include 96 KB TCM

Wireless Charging
- DDM
- Authentication
- FOD
- PID

CPU Platform Dual Core
Cortex-M7	Cortex-M7
160 Mhz	160 Mhz
FPU, DSP	FPU, DSP
I-Cache, D-Cache	I-Cache, D-Cache

Fabric
Xbar (64 bit)

Network
- 6 x FlexCAN, all ch support CAN FD
- 8 x LPUART (LIN)

Communication
- 32-ch. FlexIO Emulating UART, I²C, SPI, I2S, SENT, PWM
- 4 x LPSPI
- 2 x LPI²C

Analog/Timers
- 2 x 24-ch. 12 bit ADC
- BCTU (Body Control Trigger Unit)
- LCU (Logic Control Unit)
- 2x 24-ch. 16 bit eMIOSTimer
- 2x LPCMP

Security: HSE-B
Cortex-M0+	RAM
Asymmetric Hardware Accelerators	
Symmetric Hardware Accelerators	
XRDC Access control	Lifecycle Management
TRNG/PRNG	

Functional Safety
CMU	FCCU
MPU	SWT
EIM/ERM	STCU
CRC	

Security
- HW accl for AES 256, RSA 4096, ECC 521
- Firmware included, upgradable
- Side-channel physical protection
- Meet Evita Full function goal

Safety
- HW redundancy
- MBIST/LBIST/Self Test
- Clock/Voltage monitor
- Centralized error detection
- ASIL B compliant

Memory
- OTA ready—RWW, A/B swap

CPU Platform
- Scalable ARM M7 core
- Optimized for Real-time with zero wait I/D-TCM

Network/Communication
- CAN / CAN FD, LIN
- Flexible IO emulation

Wireless Charging Function:
- BPP / EPP / MPP Qi2
- Proprietary protocols support details on request
- On chip Authentication support
- NFC card protection and other features by NCF3321
- Capability to pass CISPR25 Class 5
- Autosar/Non Autosar drivers support

- **Future Proof Security/OTA**
- **ISO26262 Compliant Safety System**
- **Scalable ARM platform**
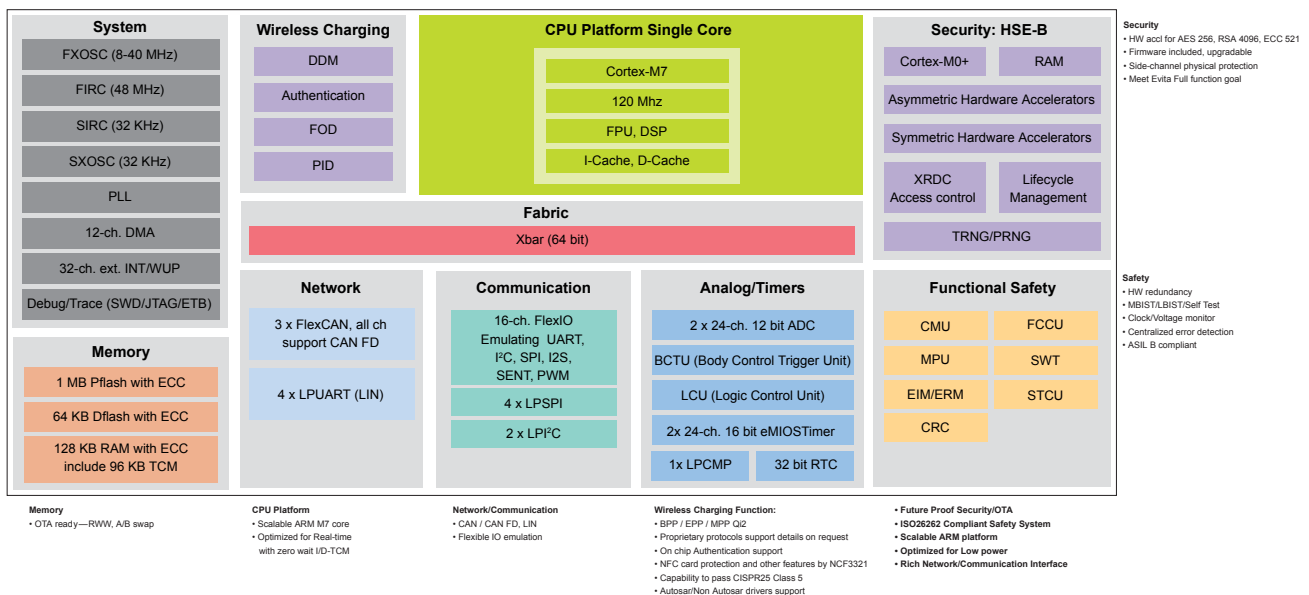- **Optimized for Low power**
- **Rich Network/Communication Interface**

MWCT2016S: ASIL B Single Core 2M Qi Wireless Charging MCU Block Diagram

MWCT2016S: ASIL B Single Core 2M Qi Wireless Charging MCU

System
- FXOSC (8-40 MHz)
- FIRC (48 MHz)
- SIRC (32 KHz)
- SXOSC (32 KHz)
- PLL
- 32-ch. DMAMUX
- 32-ch. ext. INT/WUP
- Debug/Trace (SWD/JTAG/ETB)

Memory
- 2 MB Pflash with ECC
- 128 KB Dflash with ECC
- 256 KB RAM with ECC include 192 KB TCM

Wireless Charging
- DDM
- Authentication
- FOD
- PID

CPU Platform Single Core
- Cortex-M7
- 120 Mhz
- FPU, DSP
- I-Cache, D-Cache

Fabric
- Xbar (64 bit)

Network
- 1 x Ethernet, 100Mbps AVB/TSN
- 4 x FlexCAN, all ch support CAN FD
- 4 x LPUART (LIN)

Communication
- 32-ch. FlexIO Emulating UART, I²C, SPI, I2S, SENT, PWM
- 4 x LPSPI
- 2 x LPI²C
- 2 x SAI (TDM, I2S)

Analog/Timers
- 2 x 24-ch. 12 bit ADC
- BCTU (Body Control Trigger Unit)
- LCU (Logic Control Unit)
- 2x 24-ch. 16 bit eMIOSTimer
- 2x LPCMP
- 32 bit RTC

Security: HSE-B
- Cortex-M0+
- RAM
- Asymmetric Hardware Accelerators
- Symmetric Hardware Accelerators
- XRDC Access control
- Lifecycle Management
- TRNG/PRNG

Functional Safety
- CMU
- FCCU
- MPU
- SWT
- EIM/ERM
- STCU
- CRC

Security
- HW accl for AES 256, RSA 4096, ECC 521
- Firmware included, upgradable
- Side-channel physical protection
- Meet Evita Full function goal

Safety
- HW redundancy
- MBIST/LBIST/Self Test
- Clock/Voltage monitor
- Centralized error detection
- ASIL B compliant

Memory
- OTA ready—RWW, A/B swap
- External Flash/Ram expansion by QuadSPI

CPU Platform
- Scalable ARM M7 core
- Optimized for Real-time with zero wait I/D-TCM

Network/Communication
- Ethernet (TSN), CAN / CAN FD, LIN
- SAI for Audio
- Flexible IO emulation

Wireless Charging Function:
- BPP / EPP / MPP Qi2
- Proprietary protocols support details on request
- On chip Authentication support
- NFC card protection and other features by NCF3321
- Capability to pass CISPR25 Class 5
- Autosar/Non Autosar drivers support

- **Future Proof Security/OTA**
- **ISO26262 Compliant Safety System**
- **Scalable ARM platform**
- **Optimized for Low power**
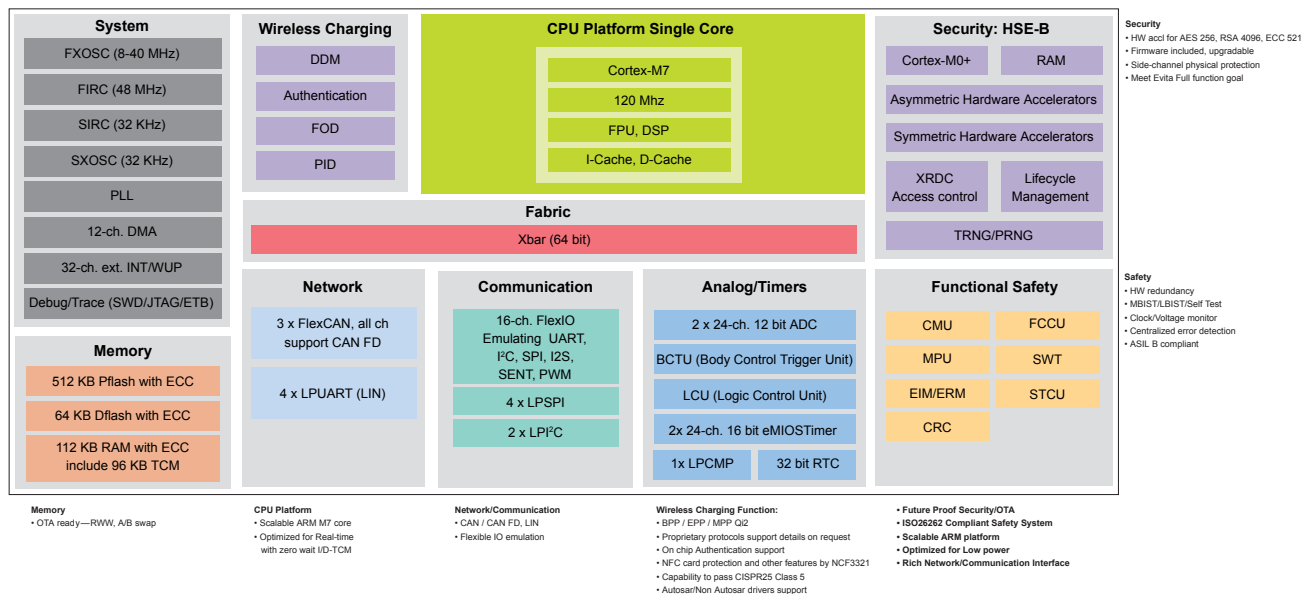- **Rich Network/Communication Interface**

MWCT2015S: ASIL B Single Core 1M Qi Wireless Charging MCU Block Diagram

MWCT2015S: ASIL B Single Core 1M Qi Wireless Charging MCU

System
- FXOSC (8-40 MHz)
- FIRC (48 MHz)
- SIRC (32 KHz)
- SXOSC (32 KHz)
- PLL
- 12-ch. DMA
- 32-ch. ext. INT/WUP
- Debug/Trace (SWD/JTAG/ETB)

Memory
- 1 MB Pflash with ECC
- 64 KB Dflash with ECC
- 128 KB RAM with ECC include 96 KB TCM

Wireless Charging
- DDM
- Authentication
- FOD
- PID

CPU Platform Single Core
- Cortex-M7
- 120 Mhz
- FPU, DSP
- I-Cache, D-Cache

Fabric
- Xbar (64 bit)

Network
- 3 x FlexCAN, all ch support CAN FD
- 4 x LPUART (LIN)

Communication
- 16-ch. FlexIO Emulating UART, I²C, SPI, I2S, SENT, PWM
- 4 x LPSPI
- 2 x LPI²C

Analog/Timers
- 2 x 24-ch. 12 bit ADC
- BCTU (Body Control Trigger Unit)
- LCU (Logic Control Unit)
- 2x 24-ch. 16 bit eMIOSTimer
- 1x LPCMP
- 32 bit RTC

Security: HSE-B
- Cortex-M0+
- RAM
- Asymmetric Hardware Accelerators
- Symmetric Hardware Accelerators
- XRDC Access control
- Lifecycle Management
- TRNG/PRNG

Functional Safety
- CMU
- FCCU
- MPU
- SWT
- EIM/ERM
- STCU
- CRC

Security
- HW accl for AES 256, RSA 4096, ECC 521
- Firmware included, upgradable
- Side-channel physical protection
- Meet Evita Full function goal

Safety
- HW redundancy
- MBIST/LBIST/Self Test
- Clock/Voltage monitor
- Centralized error detection
- ASIL B compliant

Memory
- OTA ready—RWW, A/B swap

CPU Platform
- Scalable ARM M7 core
- Optimized for Real-time with zero wait I/D-TCM

Network/Communication
- CAN / CAN FD, LIN
- Flexible IO emulation

Wireless Charging Function:
- BPP / EPP / MPP Qi2
- Proprietary protocols support details on request
- On chip Authentication support
- NFC card protection and other features by NCF3321
- Capability to pass CISPR25 Class 5
- Autosar/Non Autosar drivers support

- **Future Proof Security/OTA**
- **ISO26262 Compliant Safety System**
- **Scalable ARM platform**
- **Optimized for Low power**
- **Rich Network/Communication Interface**

MWCT2014S: ASIL B Single Core 512KB Qi Wireless Charging MCU Block Diagram

MWCT2014S: ASIL B Single Core 512KB Qi Wireless Charging MCU

System
- FXOSC (8-40 MHz)
- FIRC (48 MHz)
- SIRC (32 KHz)
- SXOSC (32 KHz)
- PLL
- 12-ch. DMA
- 32-ch. ext. INT/WUP
- Debug/Trace (SWD/JTAG/ETB)

Memory
- 512 KB Pflash with ECC
- 64 KB Dflash with ECC
- 112 KB RAM with ECC include 96 KB TCM

Wireless Charging
- DDM
- Authentication
- FOD
- PID

CPU Platform Single Core
- Cortex-M7
- 120 Mhz
- FPU, DSP
- I-Cache, D-Cache

Fabric
- Xbar (64 bit)

Network
- 3 x FlexCAN, all ch support CAN FD
- 4 x LPUART (LIN)

Communication
- 16-ch. FlexIO Emulating UART, I²C, SPI, I2S, SENT, PWM
- 4 x LPSPI
- 2 x LPI²C

Analog/Timers
- 2 x 24-ch. 12 bit ADC
- BCTU (Body Control Trigger Unit)
- LCU (Logic Control Unit)
- 2x 24-ch. 16 bit eMIOSTimer
- 1x LPCMP
- 32 bit RTC

Security: HSE-B
- Cortex-M0+
- RAM
- Asymmetric Hardware Accelerators
- Symmetric Hardware Accelerators
- XRDC Access control
- Lifecycle Management
- TRNG/PRNG

Functional Safety
- CMU
- FCCU
- MPU
- SWT
- EIM/ERM
- STCU
- CRC

Security
- HW accl for AES 256, RSA 4096, ECC 521
- Firmware included, upgradable
- Side-channel physical protection
- Meet Evita Full function goal

Safety
- HW redundancy
- MBIST/LBIST/Self Test
- Clock/Voltage monitor
- Centralized error detection
- ASIL B compliant

Memory
- OTA ready—RWW, A/B swap

CPU Platform
- Scalable ARM M7 core
- Optimized for Real-time with zero wait I/D-TCM

Network/Communication
- CAN / CAN FD, LIN
- Flexible IO emulation

Wireless Charging Function:
- BPP / EPP / MPP Qi2
- Proprietary protocols support details on request
- On chip Authentication support
- NFC card protection and other features by NCF3321
- Capability to pass CISPR25 Class 5
- Autosar/Non Autosar drivers support

- **Future Proof Security/OTA**
- **ISO26262 Compliant Safety System**
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View additional information for MWCT2xxxS Microcontroller for Wireless charging Transmitter ICs.

Note: The information on this document is subject to change without notice.