80C51 8-Bit Microcontroller Family

P80C52SBPN

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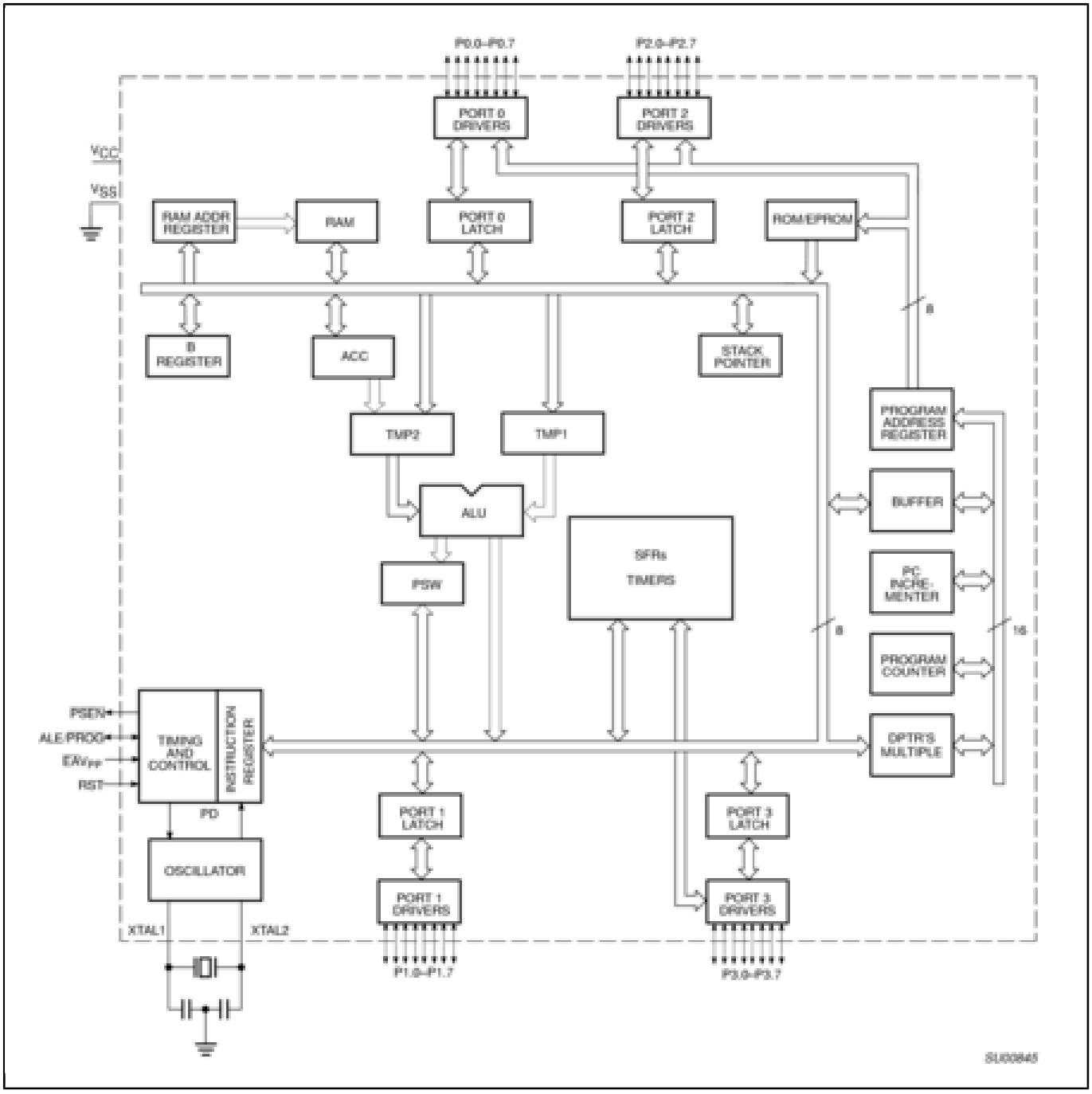
The Philips 80C51/87C51/80C52/87C52 is a high-performance static 80C51 design fabricated with Philips high-density CMOS technology with operation from 2.7 V to 5.5 V.

The 8xC51 and 8xC52 contain a 128 bytes RAM and 256 bytes RAM respectively, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction-idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

Block diagram: P80C31SBAA, P80C31SBPN, P80C31SFAA, P80C32SBAA, P80C32SBPN, P80C32UBAA, P80C32UFAA, P87C51SBAA, P87C51SBPN, P87C52SBAA, P87C52SBPN, P87C52SFAA, P87C52UBAA, P87C52UBPN Block Diagram



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