Low-Power Level Translating I²C-Bus/SMBus Repeater

PCA9509P

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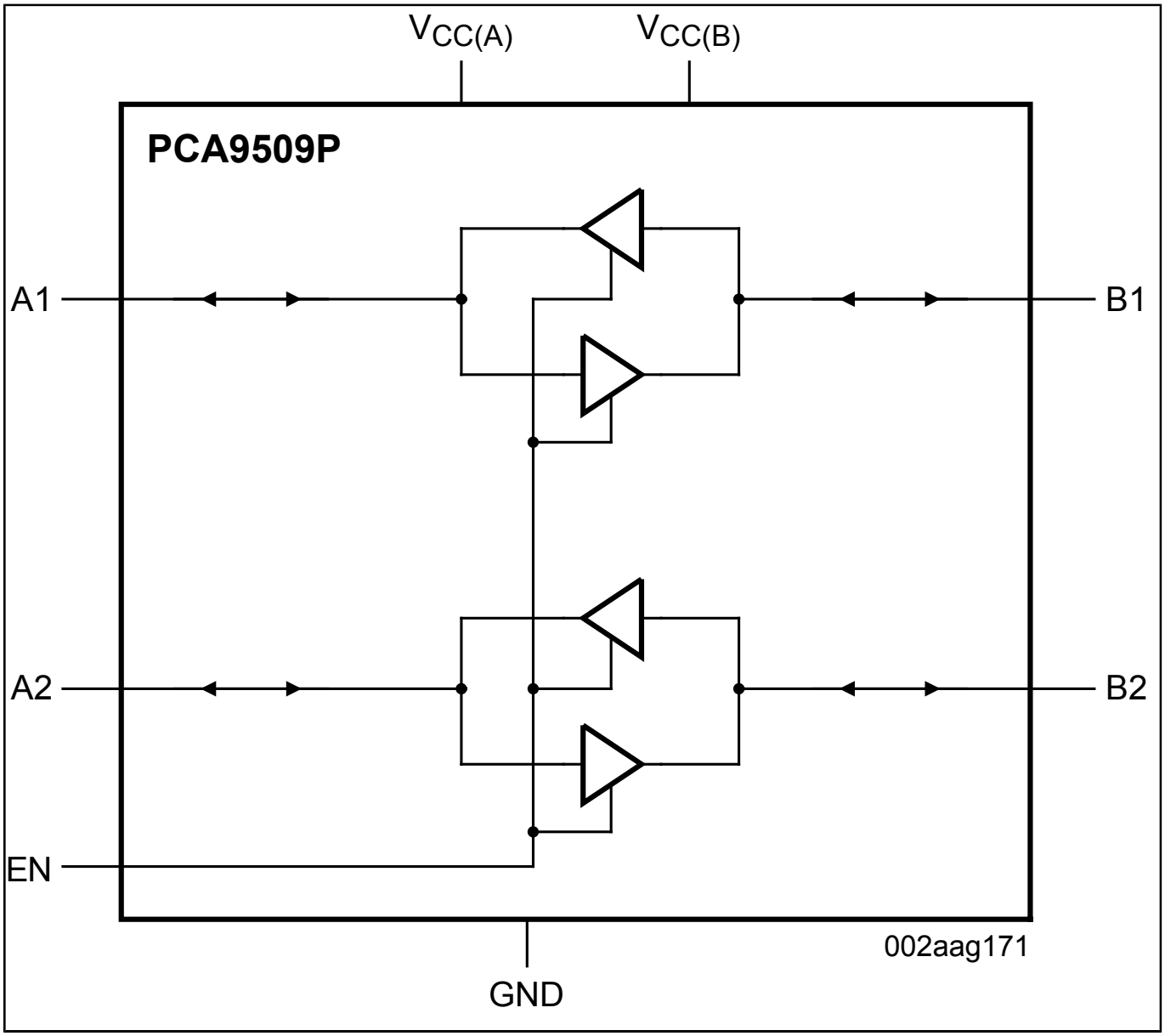
The PCA9509P is a level translating I²C-bus/SMBus repeater with two voltage supplies that enables processor low voltage 2-wire serial bus to interface with standard I²C-bus or SMBus I/O. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling the I²C-bus or SMBus maximum capacitance of 400 pF on the higher voltage side. Port A allows a voltage range from 0.8 V to 1.5 V and is overvoltage tolerant. Port B allows a voltage range from 2.3 V to 5.5 V and is overvoltage tolerant. Both port A and port B SDA and SCL pins are high-impedance when the PCA9509P is unpowered.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses an offset LOW which prevents bus lock-up and allows the bidirectional nature of the device. The output pull-down on the port A internal buffer LOW is set for approximately 0.2 VCC(A), while the input threshold of the internal buffer is set about 0.1 VCC(A) lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables port B to connect to any other I²C-bus devices or buffer.

The PCA9509P drivers are not enabled unless VCC(A) is above 0.7 V and VCC(B) is above 1.7 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

The PCA9509P is the same as the PCA9509A but without the port A internal current source to allow high value pull-up resistors to reduce current consumption in portable applications.

PCA9509P Block Diagram Block Diagram



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