Hot Swappable I²C-Bus and SMBus Bus Buffer

PCA9510A

Last Updated: Dec 23, 2025

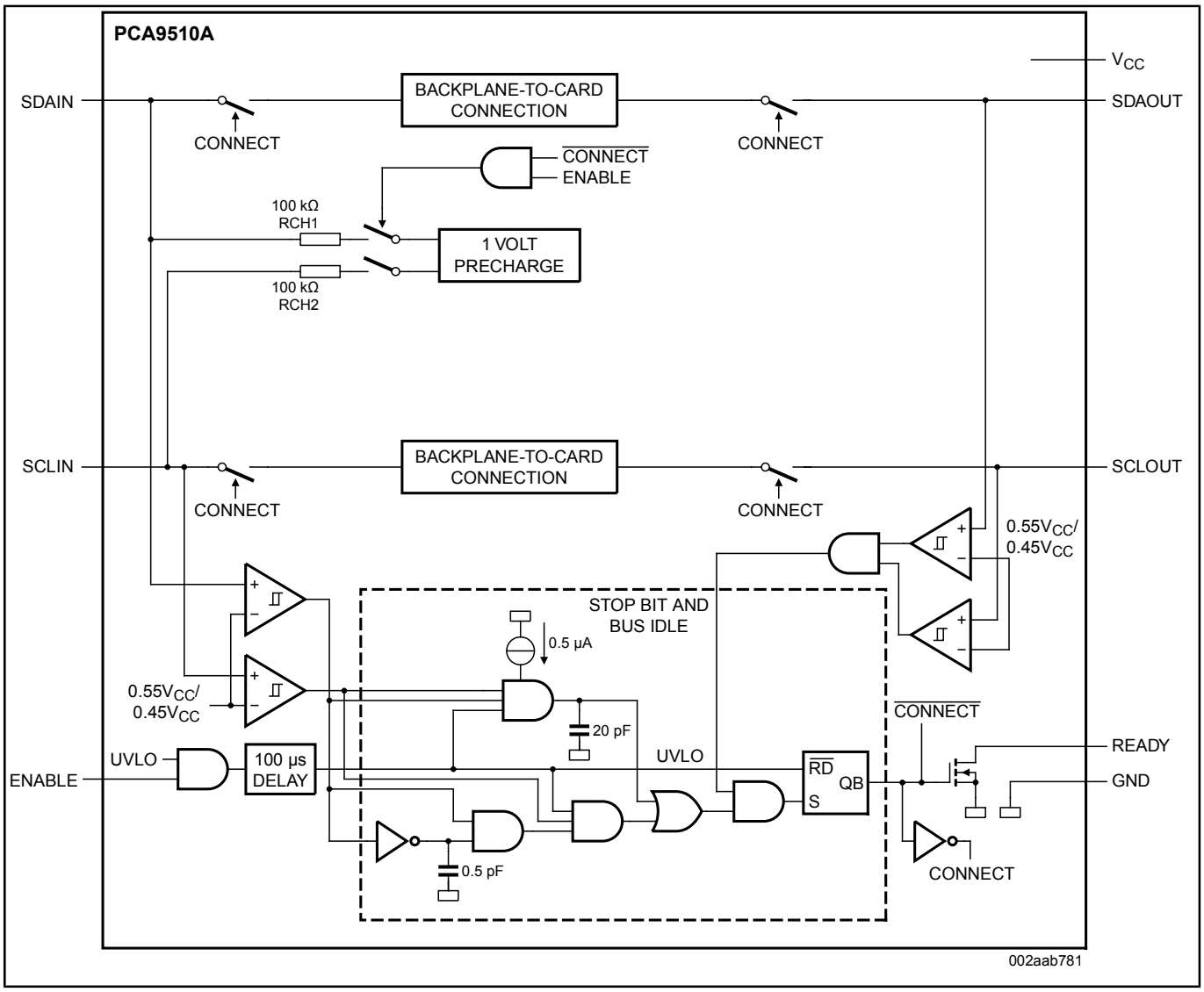
The PCA9510A is a hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9510A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9510A has no rise time accelerator circuitry to prevent interference when there are multiple devices in the same system. The PCA9510A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a Low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

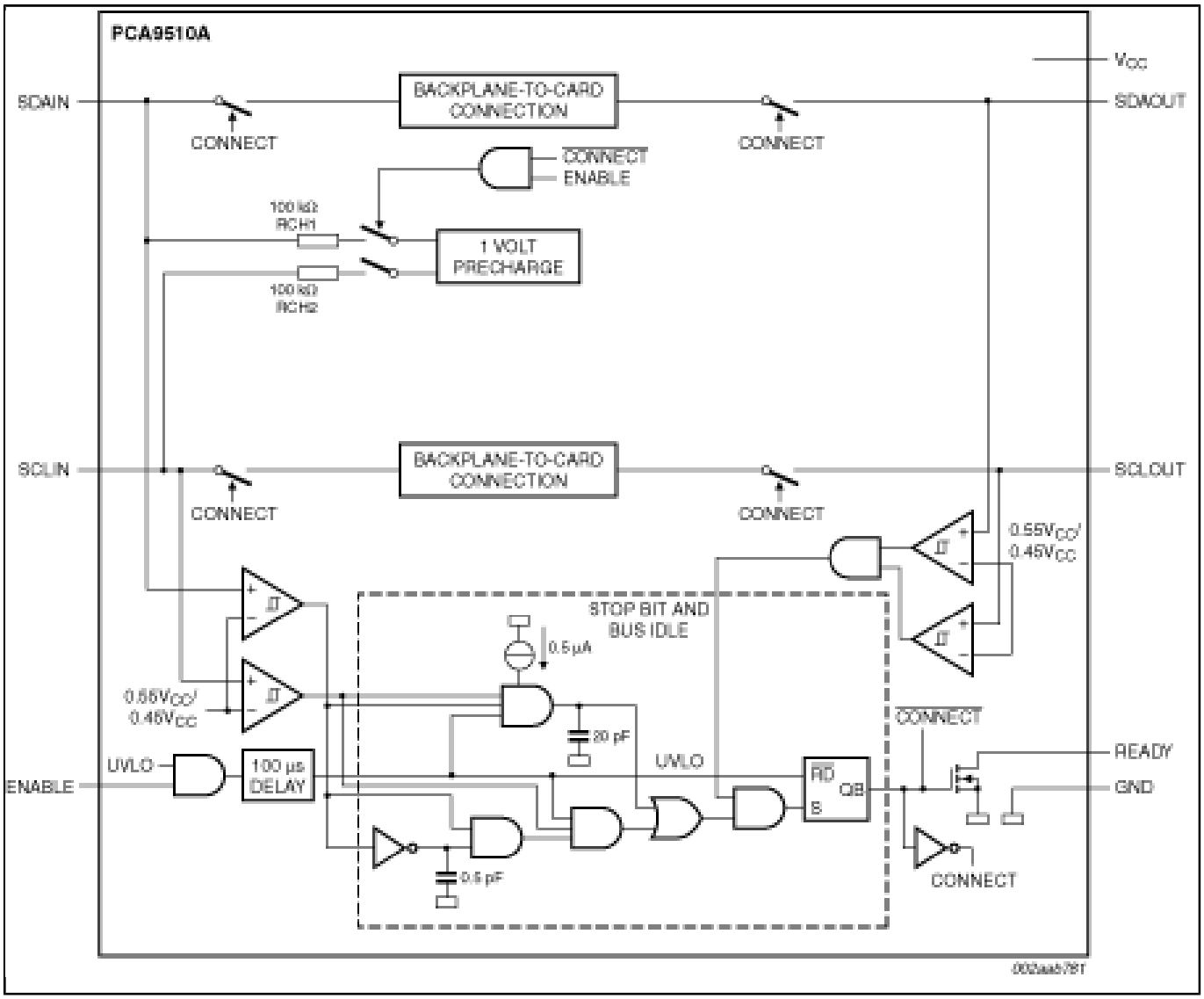
During insertion, the PCA9510A SDAIN and SCLIN pins (inputs only) are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

Remark: The dynamic offset design of the PCA9510A/11A/12A/13A/14A I/O drivers allow them to be connected to another PCA9510A/11A/12A/13A/14A device in series or in parallel and to the A side of the PCA9517. The PCA9510A/11A/12A/13A/14A cannotconnect to the static offset I/Os used on the PCA9515/15A/16/16A/18 or PCA9517 B side or P82B96 Sx/y side.

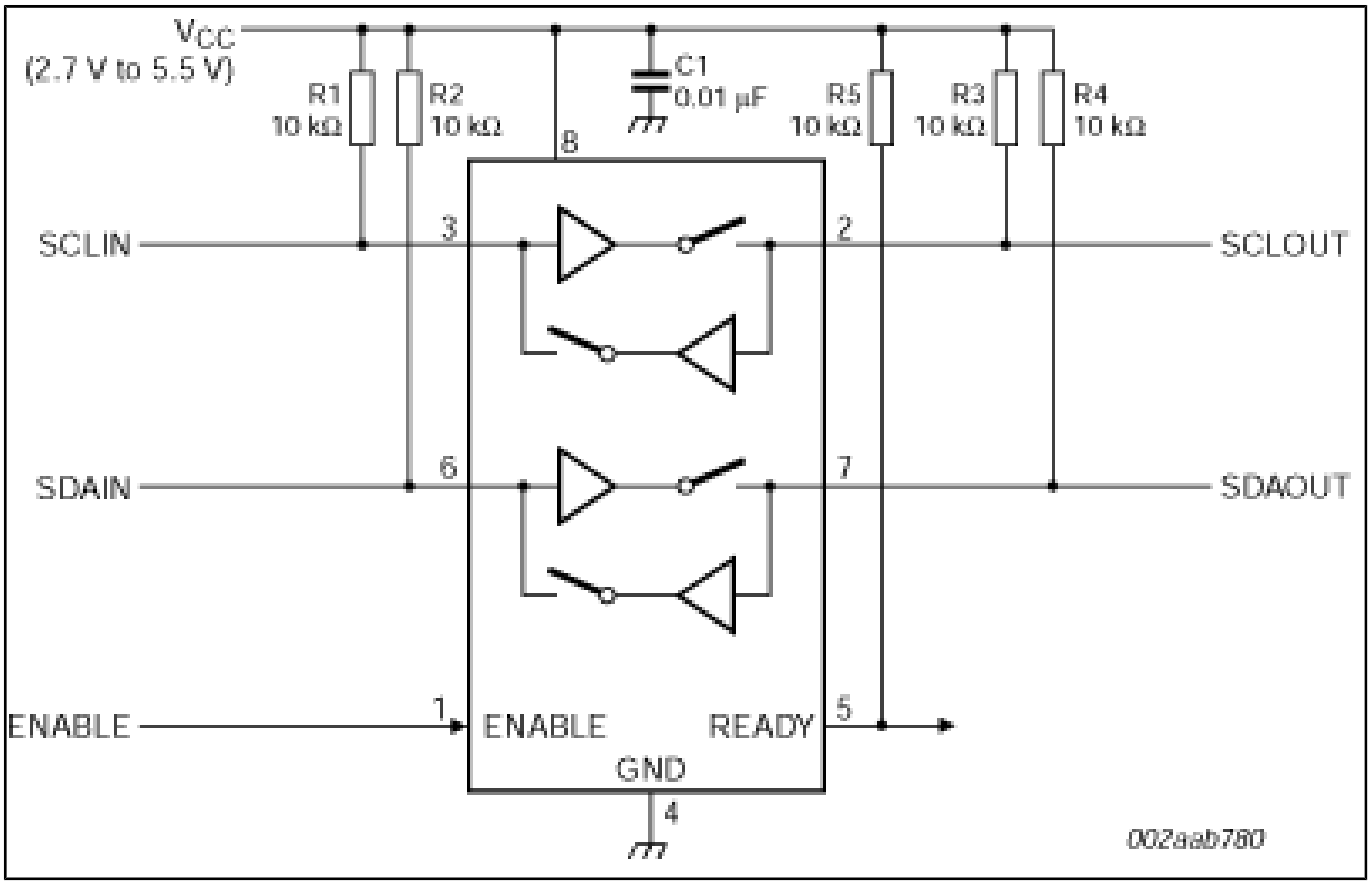
PCA9510A Block Diagram Block Diagram



Block diagram: PCA9510AD, PCA9510ADP Block Diagram



Block diagram: PCA9510AD, PCA9510ADP Block Diagram



View additional information for Hot Swappable I²C-Bus and SMBus Bus Buffer.

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