Hot Swappable I²C-Bus and SMBus Bus Buffer

PCA9511A

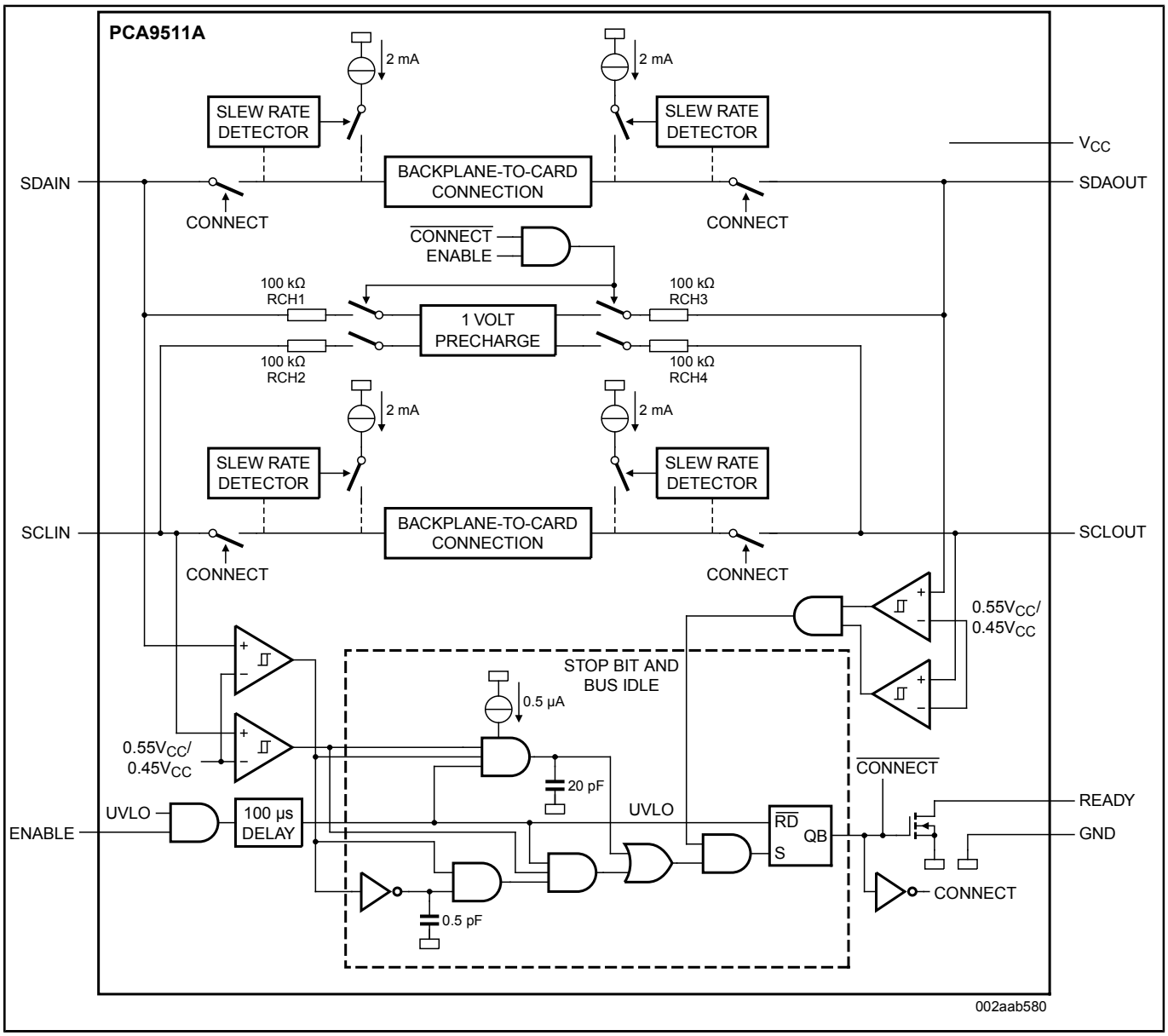
Last Updated: Jun 14, 2022

The PCA9511A is a hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

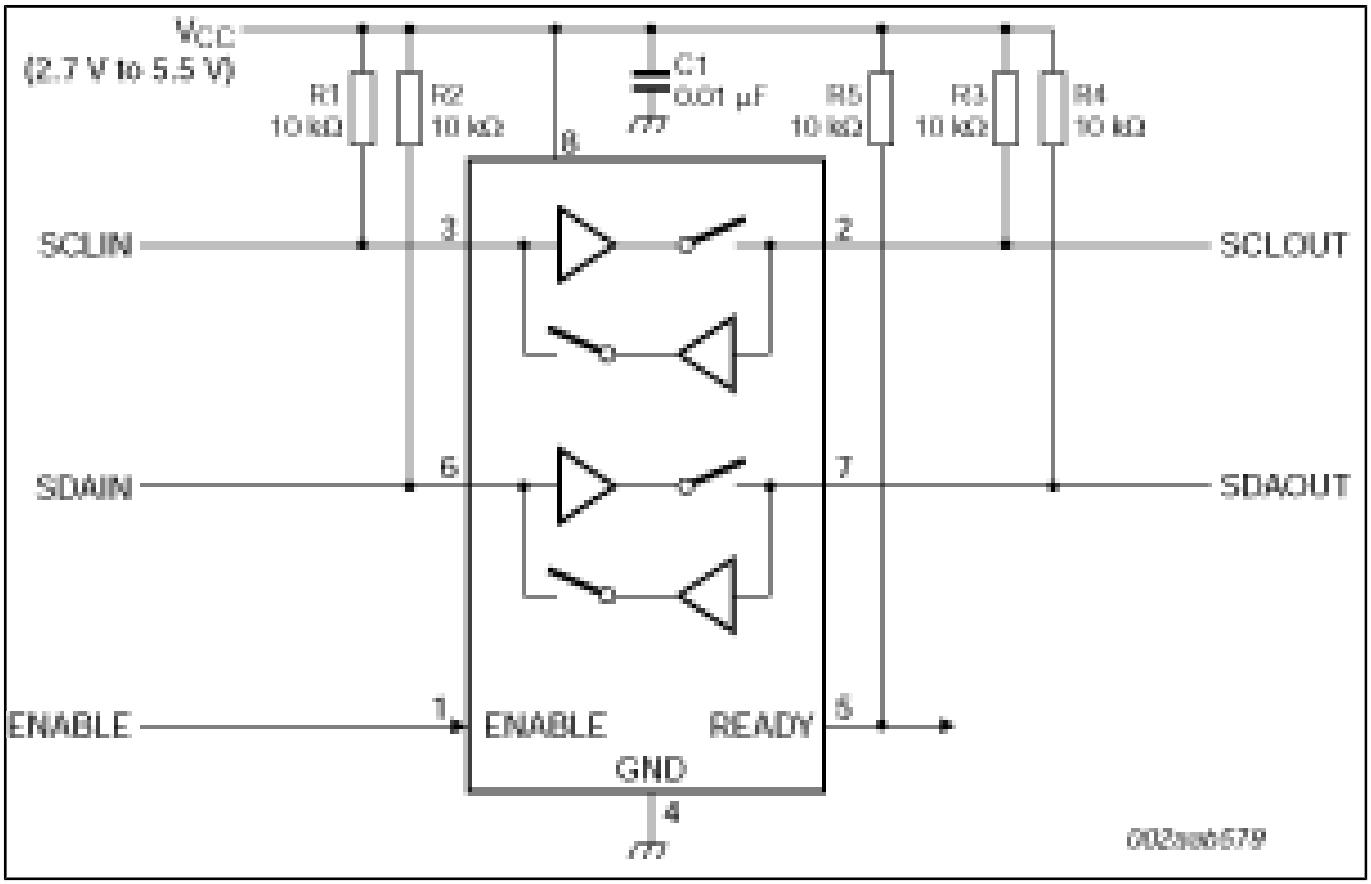
The PCA9511A rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9511A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

During insertion, the PCA9511A SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

PCA9511A Block Diagram Block Diagram



Block diagram: PCA9511AD, PCA9511ADP, PCA9513AD, PCA9513ADP, PCA9514AD, PCA9514ADP Block Diagram



View additional information for Hot Swappable I²C-Bus and SMBus Bus Buffer.

Note: The information on this document is subject to change without notice.