Level-Shifting Hot Swappable I²C-Bus and SMBus Bus Buffer

PCA9512A_PCA9512B

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The PCA9512A/B is a hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corruption of the data and clock buses and includes two dedicated supply voltage pins to provide level shifting between 3.3 V and 5 V systems while maintaining a better noise margin for each voltage level. Either pin may be powered with supply voltages ranging from 2.7 V to 5.5 V with no constraints on which supply voltage is higher. Control circuitry prevents the backplane from being connected to the card until a stop bit or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9512A/B provides bidirectional buffering, keeping the backplane and card capacitances isolated.

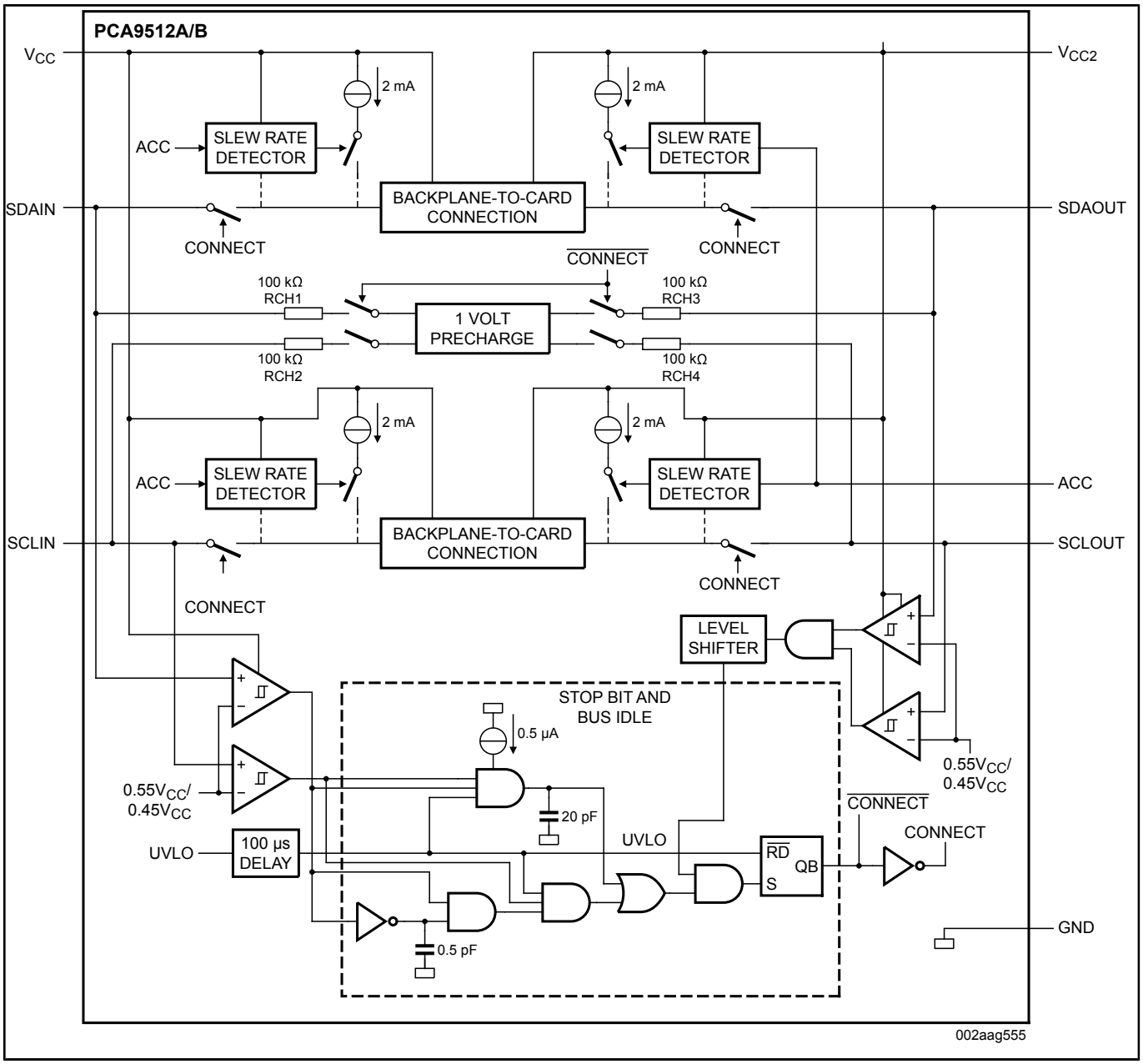
Both the PCA9512A and PCA9512B use identical silicon (PCN201012007F dated 13 Dec 2010), so the PCA9512B will be discontinued in the near future and is not recommended for new designs.

The PCA9512A/B rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9512A/B incorporates a digital input pin that enables and disables the rise time accelerators on all four SDAn and SCLn pins.

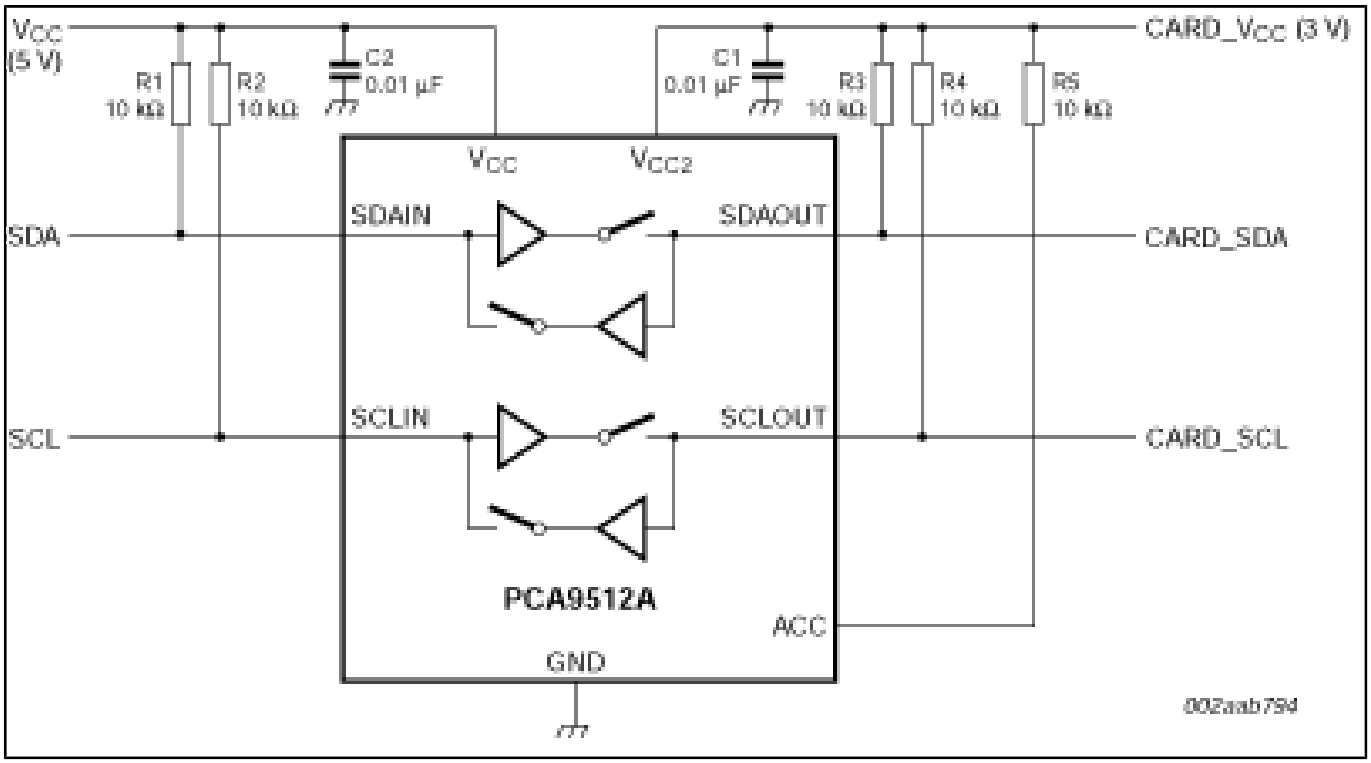
During insertion, the PCA9512A/B SDAn and SCLn pins are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

The incremental offset design of the PCA9510A/11A/12A/12B/13A/14A I/O drivers allows them to be connected to another PCA9510A/11A/12A/12B/13A/14A device in series or in parallel and to the I²C compliant side of static offset bus buffers, but not to the static offset side of those bus buffers.

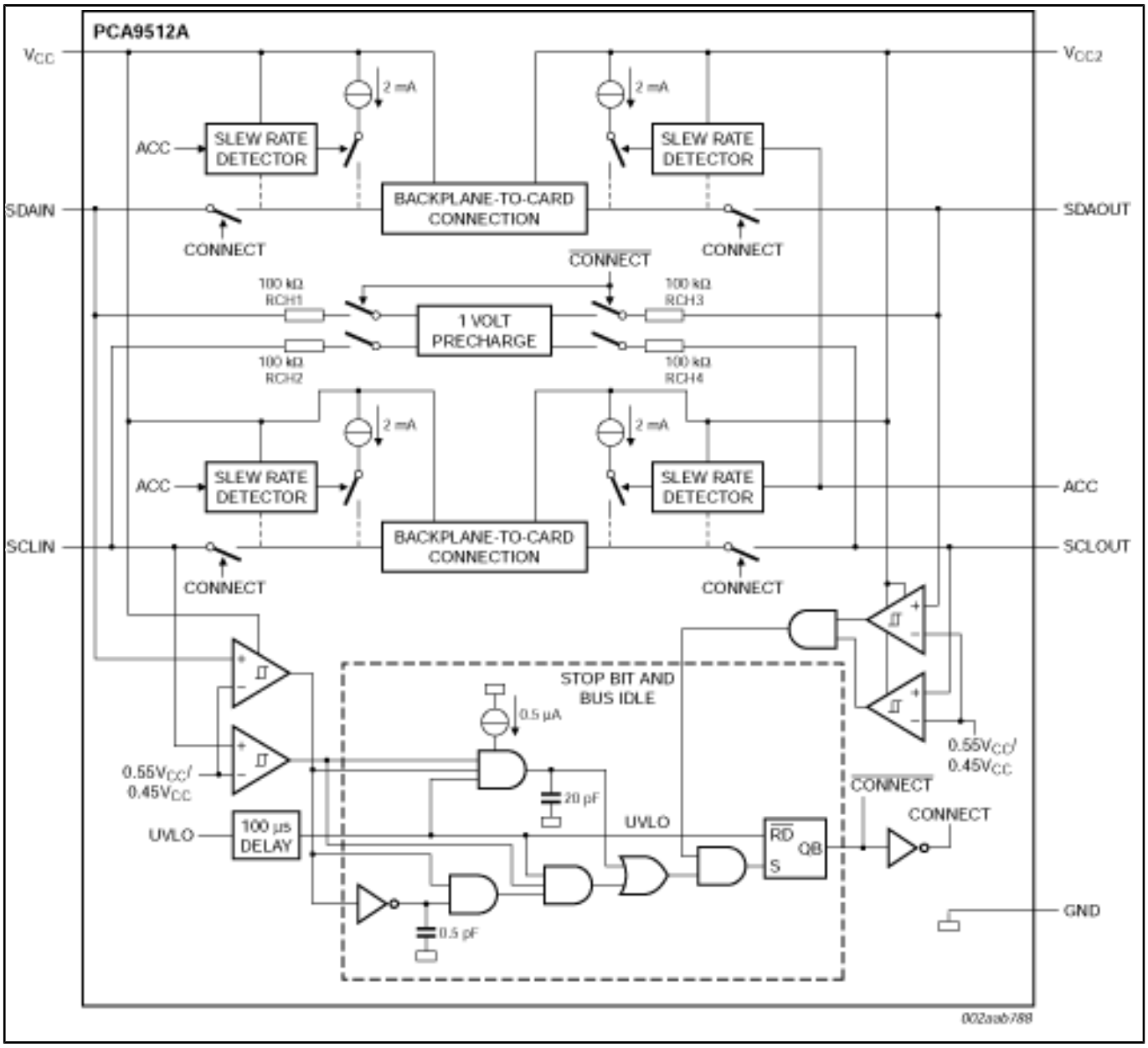
PCA9512A-PCA9512B Block Diagram Block Diagram



Block diagram: PCA9512AD, PCA9512ADP Block Diagram



Block diagram: PCA9512AD, PCA9512ADP Block Diagram



View additional information for Level-Shifting Hot Swappable I²C-Bus and SMBus Bus Buffer.

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