Level Translating I²C-Bus Repeater

PCA9517A

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The PCA9517A is a CMOS integrated circuit that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) I²C-bus or SMBus applications. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF. Using the PCA9517A enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the PCA9517A is unpowered.

The 2.7 V to 5.5 V bus port B drivers behave much like the drivers on the PCA9515A device, while the adjustable voltage bus port A drivers drive more current and eliminate the static offset voltage. This results in a LOW on the port B translating into a nearly 0 V LOW on the port A which accommodates smaller voltage swings of lower voltage logic.

The static offset design of the port B PCA9517A I/O drivers prevent them from being connected to another device that has rise time accelerator including the PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515A, PCA9516A, PCA9517A (port B), or PCA9518. Port A of two or more PCA9517As can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9517As can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

The PCA9517A drivers are not enabled unless VCC(A) is above 0.8 V and VCC(B) is above 2.5 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the port B internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on port A drives a hard LOW and the input level is set at 0.3VCC(A) to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V.

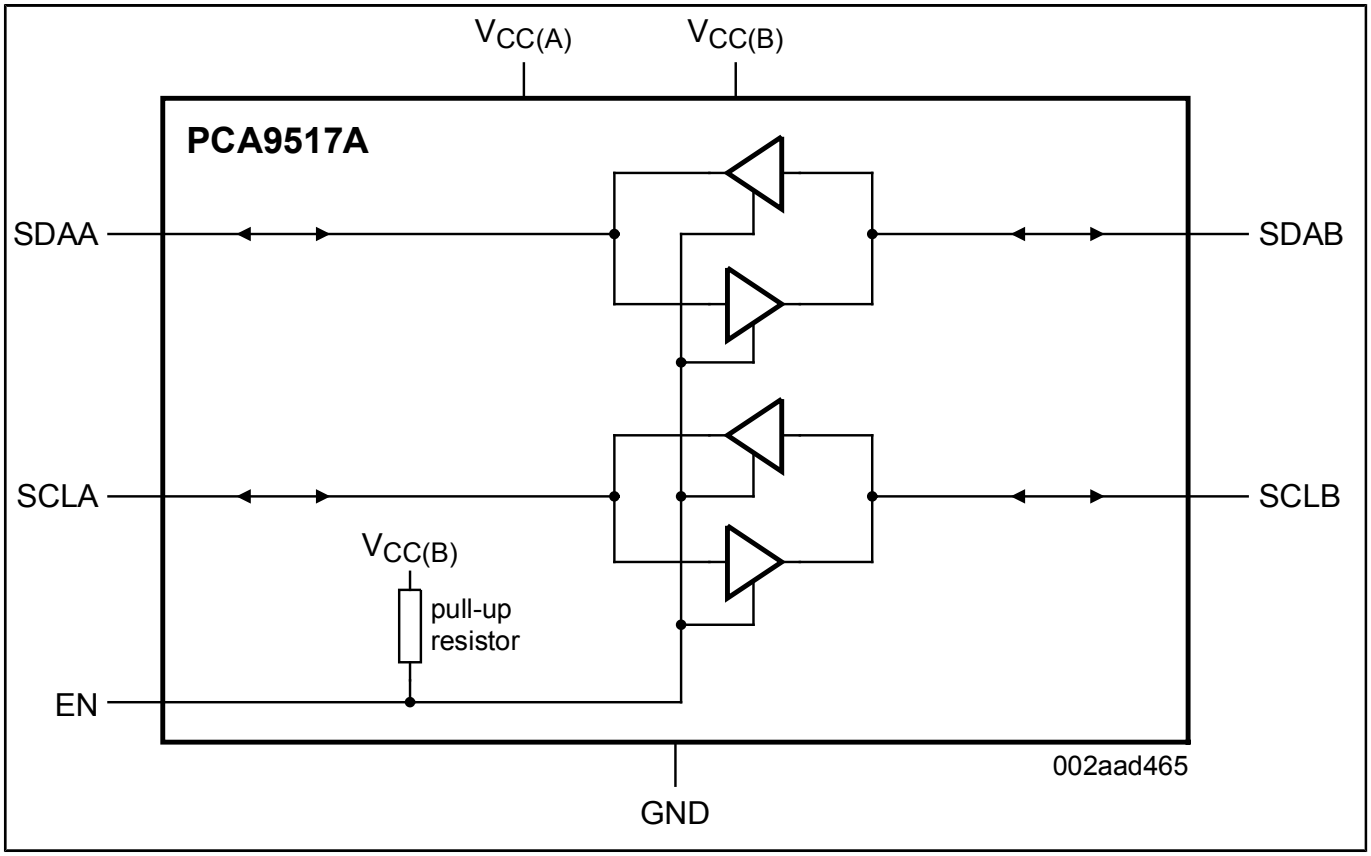
Table 1. PCA9517 and PCA9517A comparison

Parameter		
PCA9517[1]		
PCA9517A[2]		
electrostatic discharge, HBM	> 2 kV	> 5.5 kV

[1] PCA9517 will be discontinued in several years, so move to the PCA9517A for all new designs and system updates.

[2] The PCA9517A is an improved hot swap and ESD version of the PCA9517, but otherwise operates identically and should be used for all new designs and system updates.

PCA9517A Block Diagram



View additional information for Level Translating I²C-Bus Repeater.

Note: The information on this document is subject to change without notice.