Three-Channel Bidirectional Bus Extender for HDMI, I²C-Bus and SMBus

PCA9527DP

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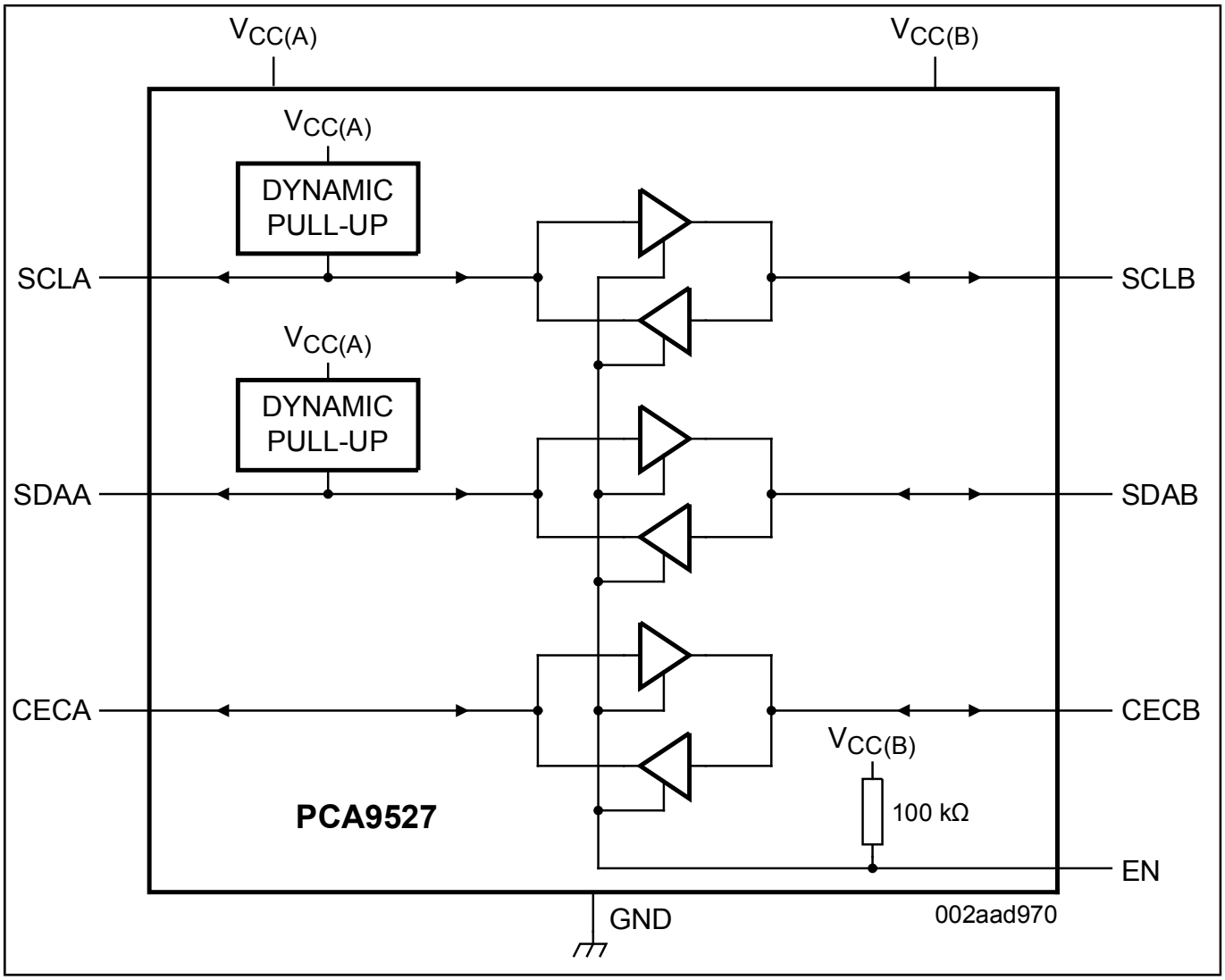
The PCA9527 is a 3-channel bidirectional open-drain bus buffer for Display Data Control (DDC) clock, data and Consumer Electronic Control (CEC) for HDMI application. The device has two power supply pins to allow voltage level shift from 2.7 V to 5 V, and a rise time accelerator on port A of each DDC clock and data for driving longer cable (up to 18 meters or 1400 pF reliably without violating the bus rise time). The 5 V tolerant CEC channel is internally connected to VCC(B) and has no rise time accelerator. The CEC channel can be used as an interrupt or reset.

While retaining all the operating modes and features of the I²C-bus system during the level shift, it also permits extension of the I²C-bus by providing bidirectional buffering for data (SDA), clock (SCL), and CEC. Using the PCA9527 enables the system designer to isolate bus capacitance to meet HDMI DDC version 1.3 distance specification. The SDAx and SCLx pins are overvoltage tolerant and are high-impedance when the PCA9527 is unpowered. The port B drivers (SDAB, SCLB, CECB) with static level offset behave much like the drivers on the PCA9515 device, while the SDAA and SCLA drivers integrate the rise time accelerator, sink more current and eliminate the static offset voltage. The CECA driver has the same current and static offset voltage features as the SDAA and SCLA, but it does not have the rise time accelerator and is powered and referenced to VCC(B). This results in a LOW on the port B translating into a nearly 0 V LOW on port A, providing zero offset. The static level offset design of the port B I/O drivers prevent them from being connected to another device that has rise time accelerator including the PCA9507 (port B), PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515, PCA9516A, PCA9517 (port B), or PCA9518A. Port A of two or more PCA9527s can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9527s can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider. Rise time accelerators on the SDAA and SCLA pins are turned on when input threshold is above 0.3VCC(A). The PCA9527 SDA and SCL drivers are not enabled

unless VCC(A) and VCC(B) are above 2.7 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle. The output pull-down on the port B internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring.

PCA9527 Block Diagram Block Diagram



View additional information for Three-Channel Bidirectional Bus Extender for HDMI, I²C-Bus and SMBus.

Note: The information on this document is subject to change without notice.

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