



Two-Channel I²C-Bus Multiplexer and Interrupt Logic

PCA9542A

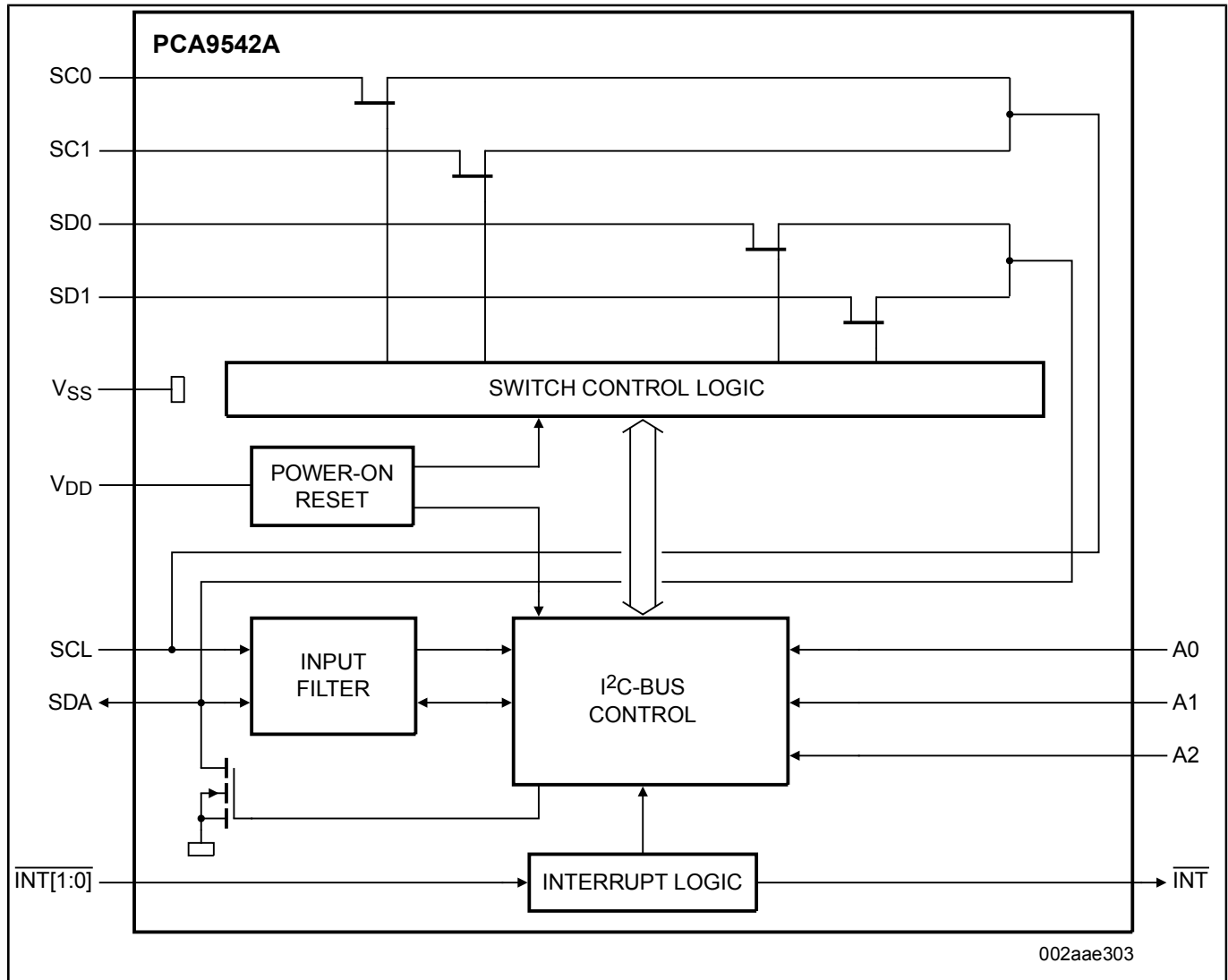
Last Updated: Sep 13, 2024

The PCA9542A is a 1-of-2 bidirectional translating multiplexer, controlled via the I²C-bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Two interrupt inputs, INT0 and INT1, one for each of the SCx/SDx downstream pairs, are provided. One interrupt output, INT, which acts as an AND of the two interrupt inputs, is provided.

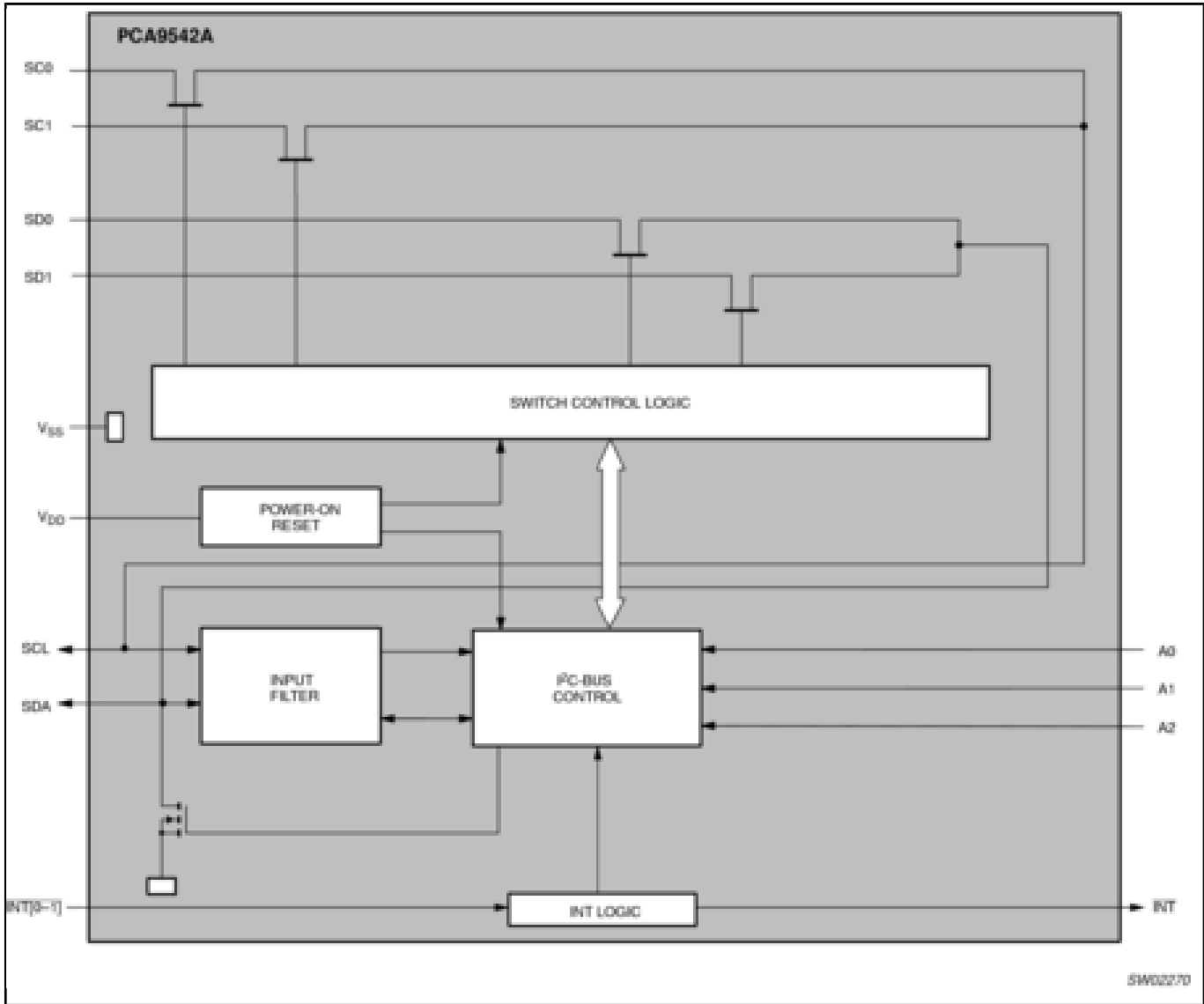
A power-on reset function puts the registers in their default state and initializes the I²C-bus state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the VDD pin can be used to limit the maximum high voltage which will be passed by the PCA9542A. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

PCA9542A Block Diagram



PCA9542AD, PCA9542APW Block Diagram



View additional information for [Two-Channel I²C-Bus Multiplexer and Interrupt Logic](#).

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.