



# Two-Channel I<sup>2</sup>C-Bus Switch with Interrupt Logic and Reset

## PCA9543A\_43B

Last Updated: Dec 23, 2025

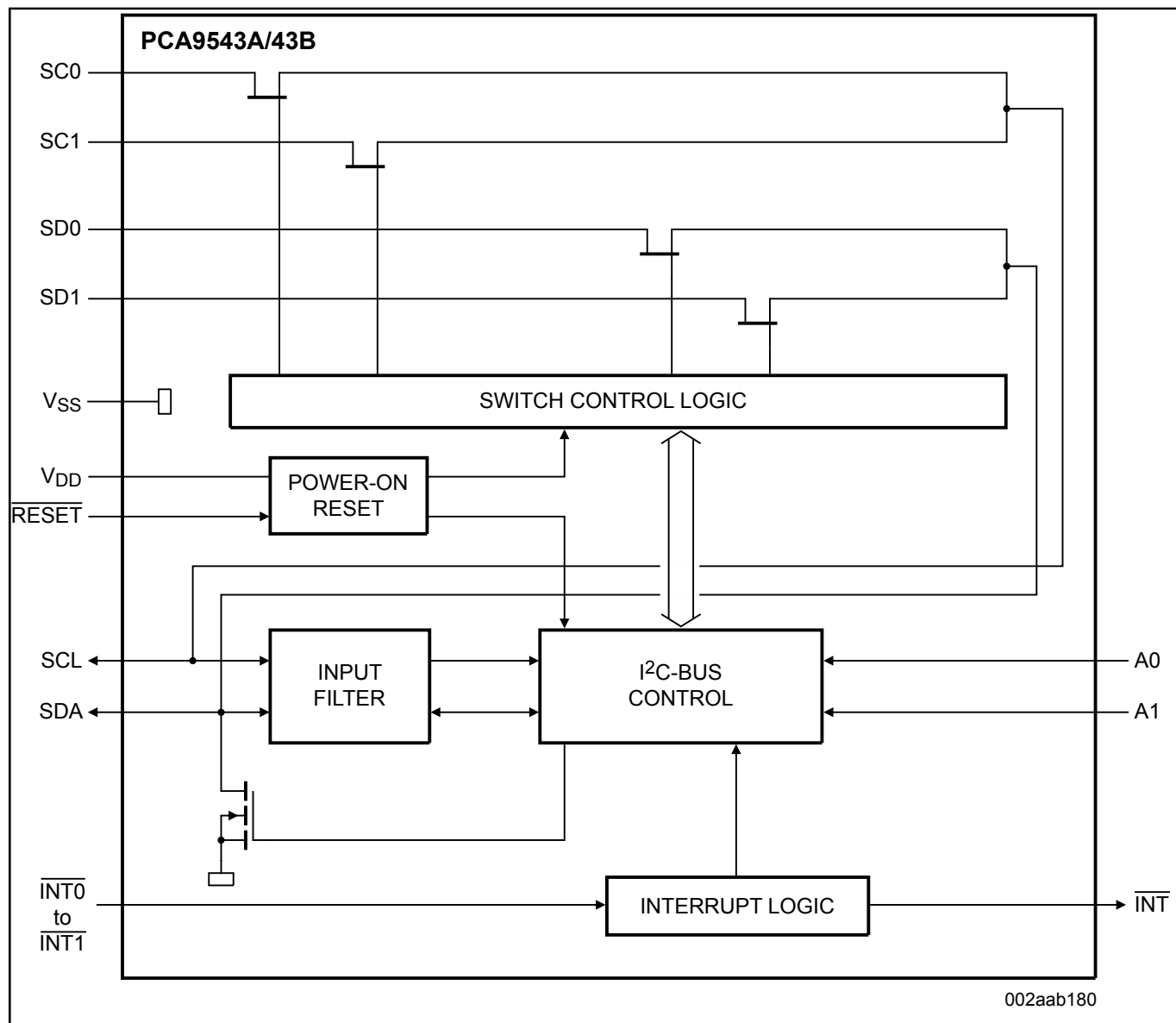
The PCA9543A/43B is a bidirectional translating switch, controlled by the I<sup>2</sup>C-bus. The SCL/SDA upstream pair fans out to two downstream pairs, or channels. Any individual SCx/SDx channels or combination of channels can be selected, determined by the contents of the programmable control register. Two interrupt inputs, INT0 and INT1, one for each of the downstream pairs, are provided. One interrupt output, INT, which acts as an AND of the two interrupt inputs, is provided.

An active LOW reset input allows the PCA9543X to recover from a situation where one of the downstream I<sup>2</sup>C-buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I<sup>2</sup>C-bus state machine and causes all the channels to be deselected, as does the internal power-on reset function.

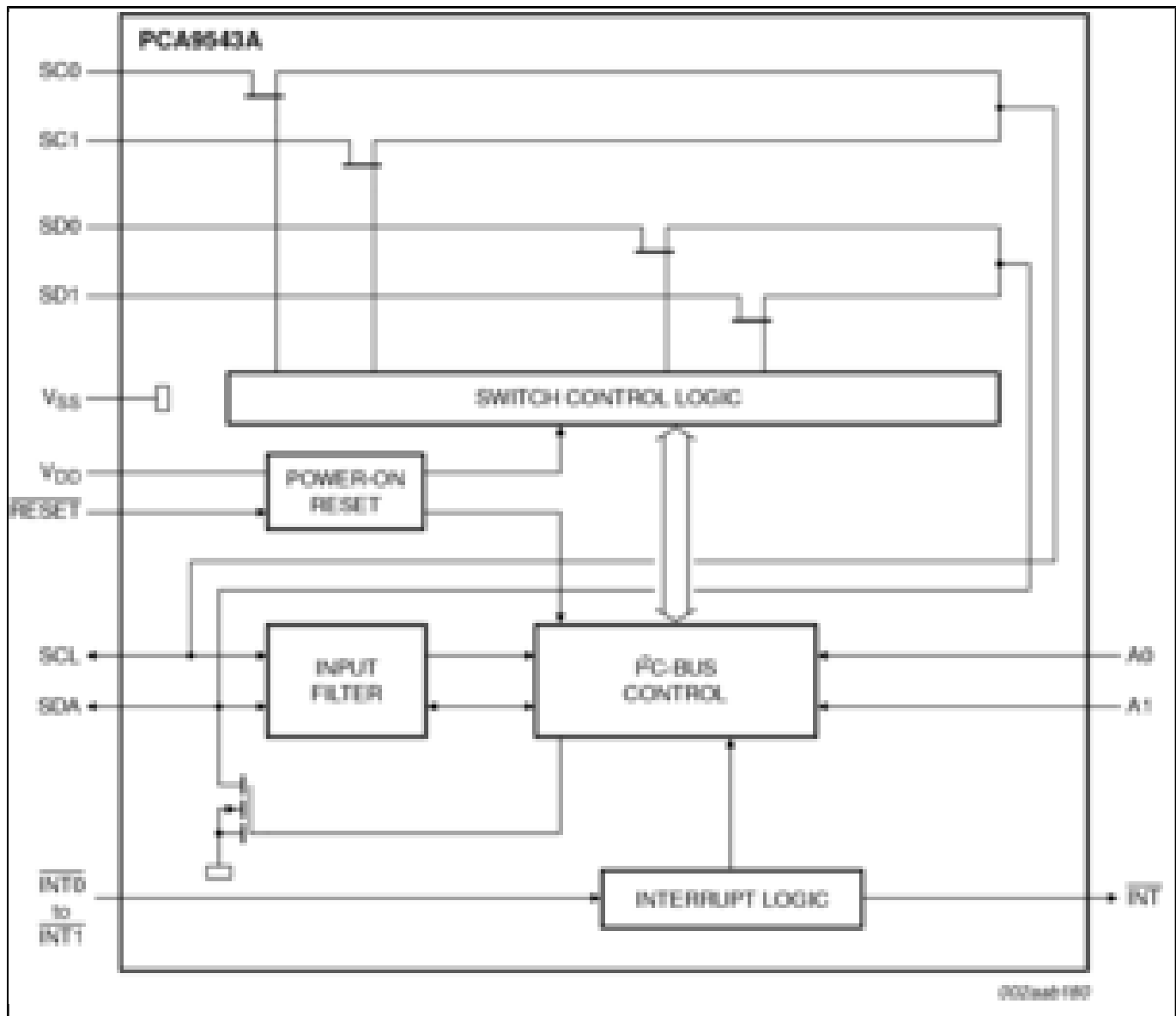
The pass gates of the switches are constructed such that the VDD pin can be used to limit the maximum high voltage which will be passed by the PCA9543X. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

The PCA9543A and PCA9543B are identical except for the fixed portion of the target address.

**PCA9543A\_43B Block Diagram Block Diagram**



**PCA9543AD, PCA9543APW, PCA9543BPW, PCA9543CPW Block Diagram Block Diagram**



View additional information for [Two-Channel I2C-Bus Switch with Interrupt Logic and Reset](#).

**Note:** The information on this document is subject to change without notice.

**www.nxp.com**

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2026 NXP B.V.