16-Bit I²C-Bus and SMBus, Level Translating, Low Voltage GPIO with Reset and Interrupt

PCA9575

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The PCA9575 is a CMOS device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion in low voltage processor and handheld battery powered mobile applications and was developed to enhance the NXP family of I2C-bus I/O expanders. The improvements include lower supply current, lower operating voltage of 1.1 V to 3.6 V, separate supply rails to allow voltage level translation anywhere between 1.1 V and 3.6 V, 400 kHz clock frequency, and smaller packaging. Any of the 16 I/O ports can be configured as an input or output independent of each other and default on start-up to inputs.

I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum; for example in battery powered mobile applications and clamshell devices for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. PCA9575 has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/Os is required. The core of PCA9575 can operate at a voltage as low as 1.1 V while each I/O bank can operate in the range 1.1 V to 3.6 V. Bus hold with programmable on-chip pull-up or pull-down feature for I/Os is also provided.

The output stage consists of two banks each of 8-bit configuration registers, input registers, interrupt mask registers, output registers, bus-hold and pull-up/pull-down registers and polarity inversion registers. These registers allow the system controller to program and configure 16 GPIOs through the I2C-bus.

The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read registers can be inverted with the Polarity Inversion register (active HIGH or active LOW operation). Either a bus-hold function or pull-up/pull-down feature can be selected by programming corresponding registers. The bus-hold provides a valid logic level when the I/O bus is not actively driven. When bus-hold feature is not selected, the I/O ports can be configured to have pull-up or pull-down by programming the pull-up/pull-down configuration register.

An open-drain interrupt output pin (INT) allows monitoring of the input pins and is asserted each time a change occurs on an input port unless that port is masked (default = masked). A 'GPIO All Call' command allows programming multiple PCA9575s at the same time even if they have different individual I2C-bus addresses. This allows optimal code programming when more than one device needs to be programmed with the same instruction or if all outputs need to be turned on or off at the same time. The internal Power-On Reset (POR) or hardware reset pin (RESET) initializes the two banks of 8 I/Os as inputs, sets the registers to their default values and initializes the device state machine. The I/O banks are held in its default state when the logic supply (VDD) is off.

The PCA9575 is available in 24-pin TSSOP, 28-pin TSSOP and HWQFN24 packages, and is specified over the -40 C to +85 C industrial temperature range.

The 28-pin package provides four address select pins, allowing up to 16 PCA9575 devices to be connected with 16 different addresses on the same I2C-bus.

PCA9575 Block Diagram

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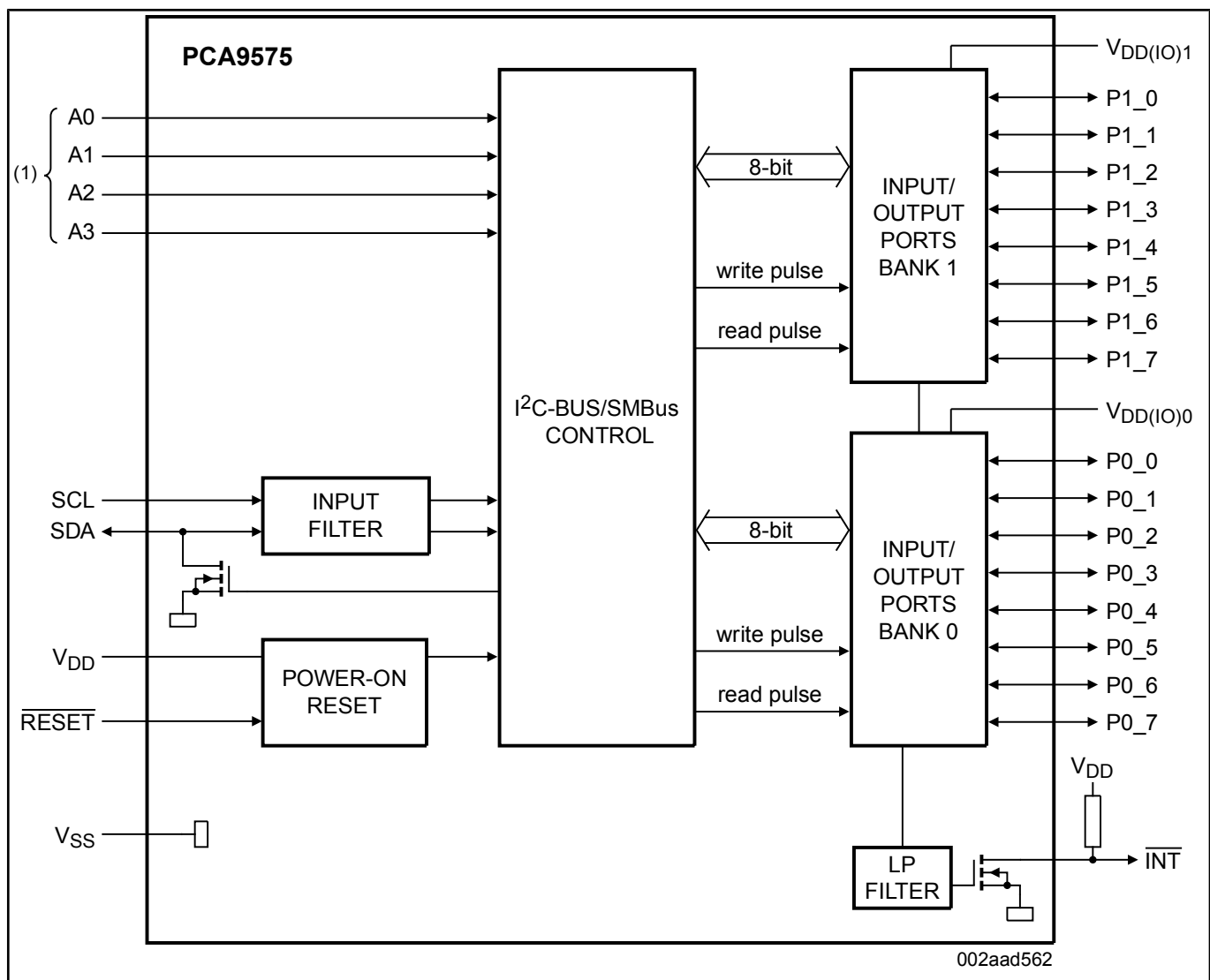
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