Dual Bidirectional Bus Buffer

PCA9600

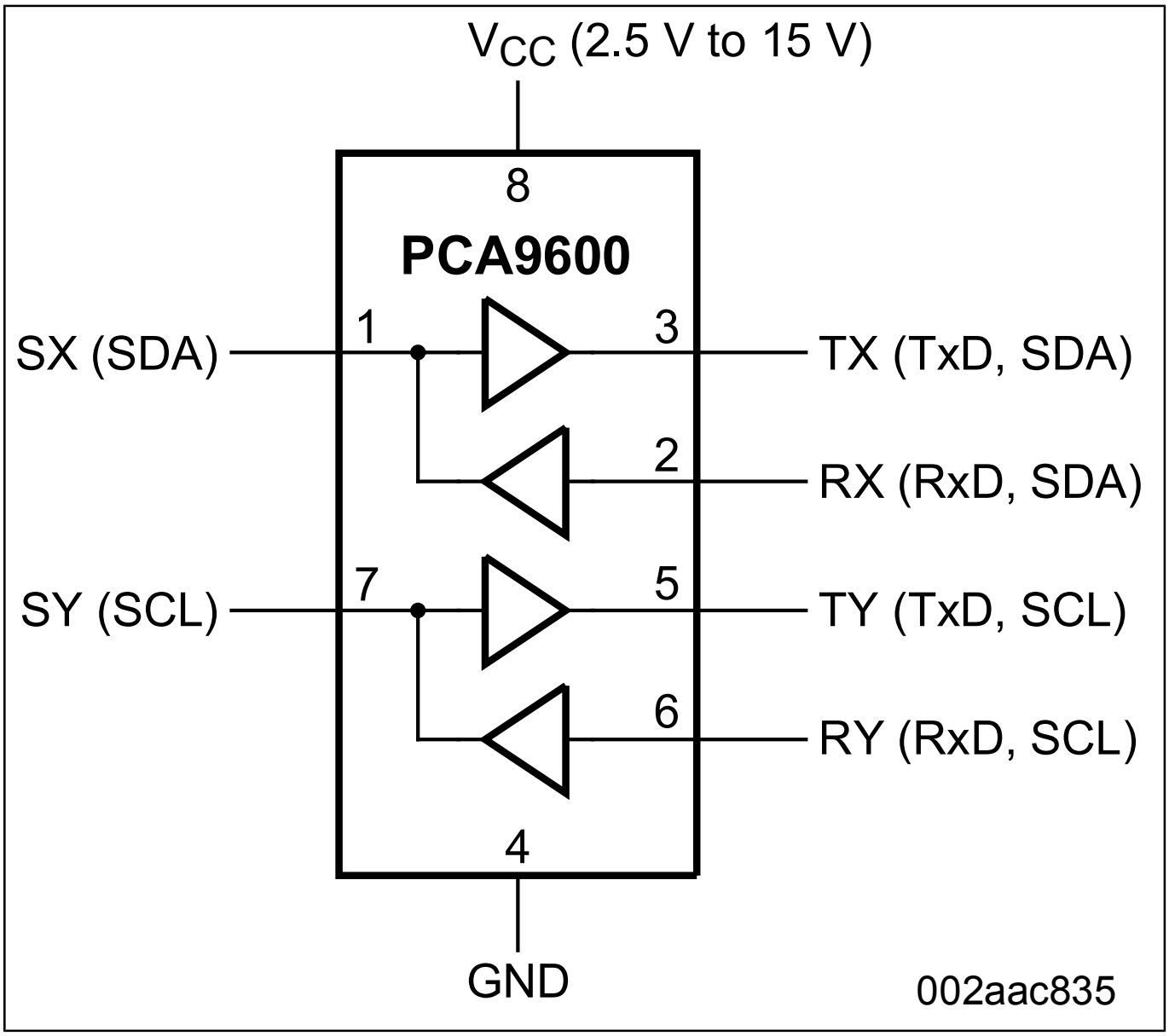
Last Updated: Dec 23, 2025

The PCA9600 is designed to isolate I²C-bus capacitance, allowing long buses to be driven in point-to-point or multipoint applications of up to 4000 pF. The PCA9600 is a higher-speed version of the P82B96. It creates a non-latching, bidirectional, logic interface between a normal I²C-bus and a range of other higher capacitance or different voltage bus configurations. It can operate at speeds up to at least 1 MHz, and the high drive side is compatible with the Fast-mode Plus (Fm+) specifications.

The PCA9600 features temperature-stabilized logic voltage levels at its SX/SY interface making it suitable for interfacing with buses that have non I²C-bus-compliant logic levels such as SMBus, PMBus, or with microprocessors that use those same TTL logic levels.

The separation of the bidirectional I²C-bus signals into unidirectional TX and RX signals enables the SDA and SCL signals to be transmitted via balanced transmission lines (twisted pairs), or with galvanic isolation using opto or magnetic coupling. The TX and RX signals may be connected together to provide a normal bidirectional signal.

PCA9600 Block Diagram



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Note: The information on this document is subject to change without notice.