



Low Power HDMI/DVI Level Shifter with Active DDC Buffer, Supporting 3.4 Gbit/s Operation

PTN3363BS

Last Updated: Dec 24, 2025

PTN3363 is a low power, high-speed level shifter device which converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals, up to 3.4 Gbit/s per lane to support 36-bit deep color mode, 4K x 2K video format or 3D video data transport. Each of these lanes provides a level-shifting differential active buffer, with built-in Equalization, to translate from low-swing AC-coupled differential signaling on the source side, to TMDS-type DC-coupled differential current-mode signaling terminated into 50 Ω to 3.3 V on the sink side. Additionally, the PTN3363 provides a single-ended active buffer for voltage translation of the HPD signal from 5 V on the sink side to 3.3 V on the source side and provides a channel with active buffering and level shifting of the DDC channel (consisting of a clock and a data line) between 3.3 V source-side and 5 V sink-side. The DDC channel is implemented using active I²C-bus buffer technology providing redriving and level shifting as well as disablement (isolation between source and sink) of the clock and data lines.

The low-swing AC-coupled differential input signals to the PTN3363 typically come from a display source with multi-mode I/O, which supports multiple display standards, for example, DisplayPort, HDMI and DVI. While the input differential signals are configured to carry DVI or HDMI coded data, they do not comply with the electrical requirements of the DVI v1.0 or HDMI v1.4b specification. By using PTN3363, chip set vendors are able to implement such reconfigurable I/Os on multi-mode display source devices, allowing the support of multiple display standards while keeping the number of chip set I/O pins low.

The PTN3363 main high-speed differential lanes feature low-swing self-biasing differential inputs which are compliant to the electrical specifications of DisplayPort Standard v1.2a and/or PCI Express Standard v1.1, and open-drain current-steering differential outputs compliant to DVI v1.0 and HDMI v1.4b electrical specifications. The I²C-bus channel actively buffers as well as level-translates the DDC signals. The PTN3363 supports standby mode in order to minimize current consumption when Hot Plug Detect signal HPD_SINK is LOW.

PTN3363 is powered from a single 3.3 V power supply consuming a small amount of power (72 mW typical) and is offered in a 32-terminal HVQFN32 package.

The diagram illustrates the internal architecture of the PTN3363 chip, which is a high-speed digital-to-analog converter (DAC) for HDMI. The chip is organized into several functional blocks:

- Input/Output Pairs:** Four differential input/output pairs are shown, labeled IN_D1+/IN_D1-, IN_D2+/IN_D2-, IN_D3+/IN_D3-, and IN_D4+/IN_D4-. Each pair is connected to an internal EQ (Equalization) block, which is then connected to an output driver (transistors) and a current source (enable).
- HPD Level Shifter:** The HPD_SOURCE (0 V to 3.3 V) input is connected to an HPD level shifter, which outputs to the HPD_SINK (0 V to 5 V) pin. A 200 kΩ resistor is connected between the HPD_SINK and ground.
- SYSTEM CONTROL:** This block receives HIZ_EN and DDC_EN (0 V to 3.3 V) inputs and controls the chip's operation.
- I2C-BUS SLAVE ROM:** This block receives SCL_SOURCE and SDA_SOURCE inputs and outputs to the SCL_SINK and SDA_SINK pins.
- DDC BUFFER AND LEVEL SHIFTER:** This block receives SCL_SINK and SDA_SINK inputs and outputs to the SCL_SOURCE and SDA_SOURCE pins.

The chip is labeled PTN3363 and has a part number 002aah236. The diagram also shows various internal components like resistors (Rterm), capacitors, and transistors.

View additional information for [Low Power HDMI/DVI Level Shifter with Active DDC Buffer, Supporting 3.4 Gbit/s Operation](#).

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2026 NXP B.V.