RapidRF Smart LDMOS Front-End Designs

RAPIDRFSL-FRONTEND

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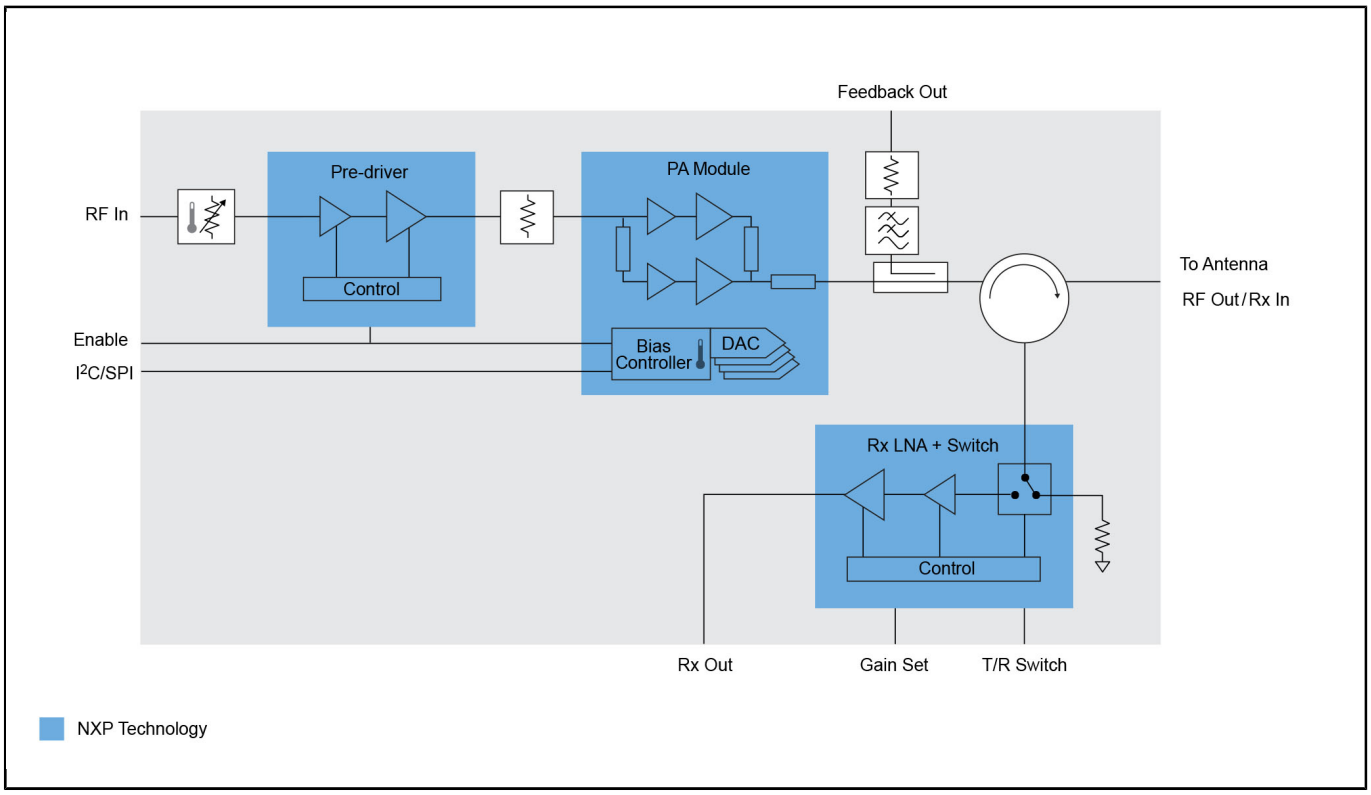
NXP’s RapidRF Smart LDMOS front-end designs provide further integration with a highly efficient RF power amplifier, linear pre-driver, Rx LNA with T/R switch, and a circulator all in a compact footprint—and now includes the bias controller and temperature sensor within the power amplifier package. These designs incorporate a coupler for DPD feedback and are to be used with digital pre-distortion.

RapidRF reference boards are ideal for 5G radio units requiring 2.5 to 8 Watts (34-39 dBm) average transmit power at the antenna. A common PCB layout used for multiple frequency bands simplifies both design and manufacturing for faster time-to-market.

RapidRF Smart LDMOS Front-End Block Diagram Block Diagram



View additional information for RapidRF Smart LDMOS Front-End Designs.

Note: The information on this document is subject to change without notice.