



S32K3 Microcontrollers for General-Purpose

S32K3

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The S32K3 MCUs of 32-bit AEC-Q100 qualified MCUs combine a scalable family of Arm® Cortex®-M7-based microcontrollers in single, dual, and lockstep core configurations, supporting up to ASIL D functional safety automotive and industrial applications.

S32K3 MCUs feature hardware security engine (HSE) with NXP firmware, support for firmware over-the-air (FOTA) updates and free ISO 26262 compliant Real-Time Drivers (RTD) for AUTOSAR® and non-AUTOSAR.

S32K3 MCUs are available in the new NXP MaxQFP package, which reduces the package footprint by up to 55% when compared to the standard QFP package.

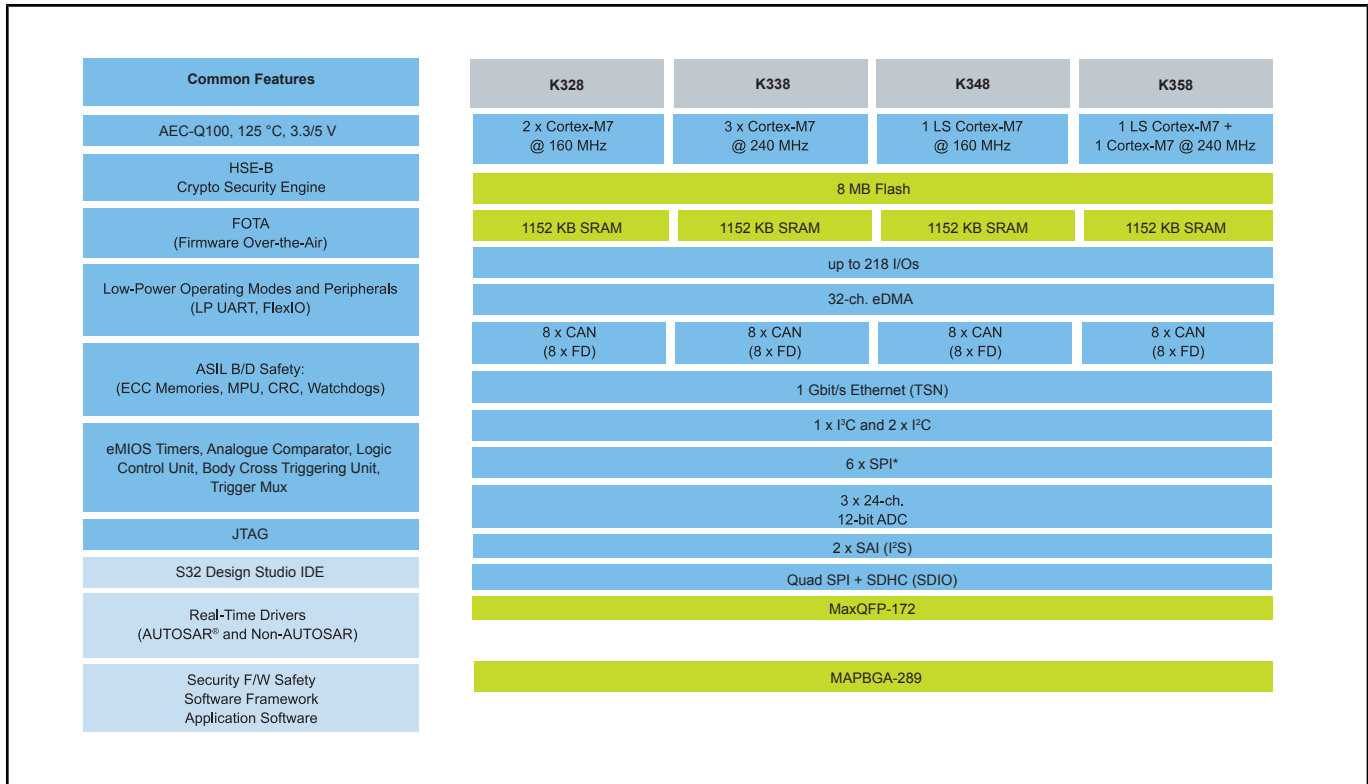
S32K3 Family Features Part 1 Block Diagram

Common Features	K311	K312	K314
AEC-Q100, 125 °C, 3.3/5 V	1 x Arm® Cortex®-M7 @120 MHz		1x Cortex-M7 @160 MHz
HSE-B Crypto Security Engine	1 MB Flash	2 MB Flash	4 MB Flash
FOTA (Firmware Over-the-Air)	128 K SRAM	192 K SRAM	512 K SRAM
Low-Power Operating Modes and Peripherals (LP UART, FlexIO)	up to 84 I/Os	up to 143 I/Os	up to 218 I/Os
ASIL B/D Safety: (ECC Memories, MPU, CRC, Watchdogs)	16-ch. eDMA		32-ch. eDMA
eMIOS Timers, Analogue Comparator, Logic Control Unit, Body Cross Triggering Unit, Trigger Mux	3 x CAN (3 x FD)	6 x CAN (6 x FD)	
JTAG	1 x I ² C and 2 x I ² C		100 Mbit/s Ethernet (TSN)
S32 Design Studio IDE	1 x I ² C and 2 x I ² C		2 x I ² C
Real-Time Drivers (AUTOSAR® and Non-AUTOSAR)	4 x SPI*		6 x SPI*
Security F/W Safety Software Framework Application Software	2 x 24-ch. 12-bit ADC		3 x 24-ch. 12-bit ADC
			2 x SAI (I ² S)
			Quad SPI
	LQFP-48	MaxQFP-172	
	MaxQFP-100		
			MAPBGA-257

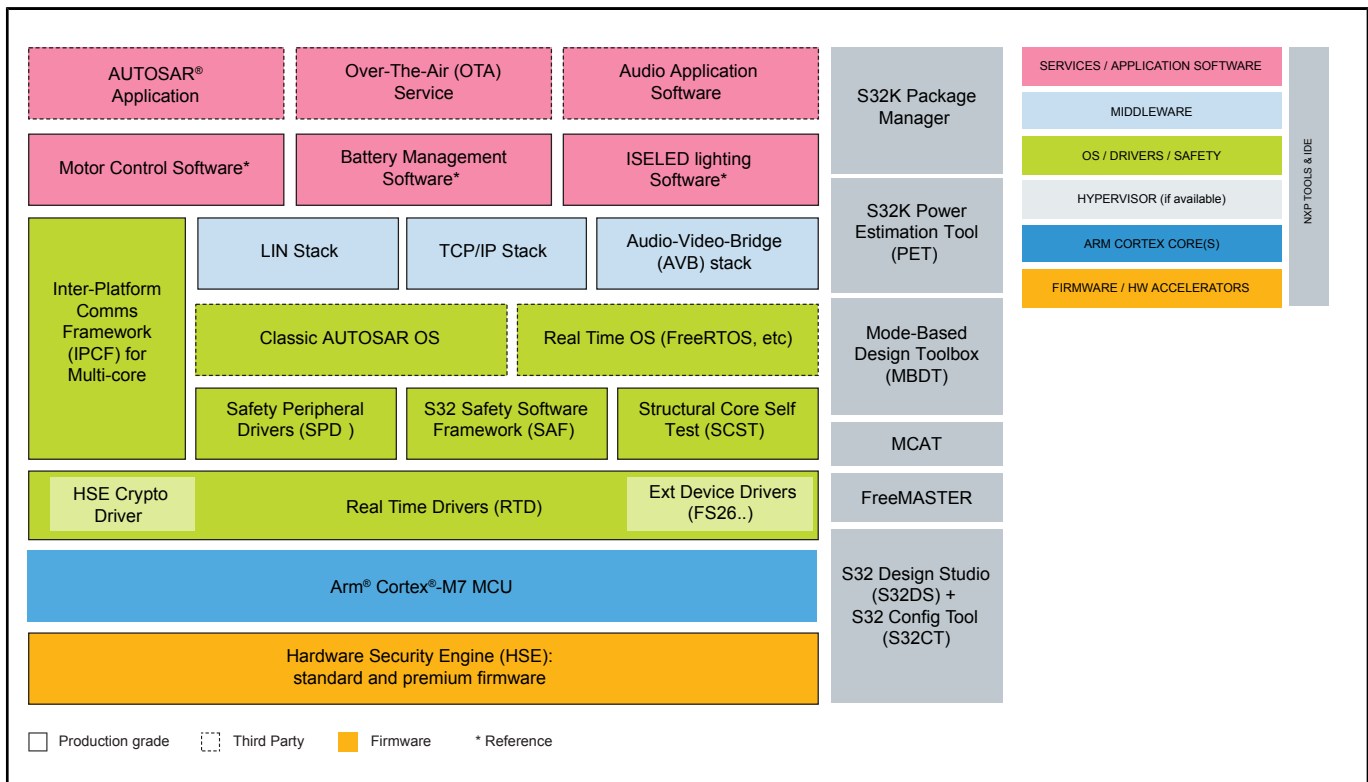
S32K3 Family Features Part 2 Block Diagram

Common Features	K322	K324	K341	K342	K344
AEC-Q100, 125 °C, 3.3/5 V	2 x Cortex-M7 @160 MHz		1 Lockstep Cortex-M7 @ 160 MHz		
HSE-B Crypto Security Engine	2 MB Flash	4 MB Flash	1 MB Flash	2 MB Flash	4 MB Flash
FOTA (Firmware Over-the-Air)	256 k SRAM	512 k SRAM	256 k SRAM	256 k SRAM	512 k SRAM
Low-Power Operating Modes and Peripherals (LP UART, FlexIO)	up to 143 I/Os	up to 218 I/Os	up to 143 I/Os	up to 143 I/Os	up to 218 I/Os
ASIL B/D Safety: (ECC Memories, MPU, CRC, Watchdogs)	32-ch. eDMA				
eMIOS Timers, Analogue Comparator, Logic Control Unit, Body Cross Triggering Unit, Trigger Mux	4 x CAN (4 x FD)	6 x CAN (6 x FD)	4 x CAN (4 x FD)	4 x CAN (4 x FD)	6 x CAN (6 x FD)
JTAG	100 Mbit/s Ethernet (TSN)				
S32 Design Studio IDE	1 x I ² C and 2 x I ² C	2 x I ² C	1 x I ² C and 2 x I ² C	1 x I ² C and 2 x I ² C	2 x I ² C
Real-Time Drivers (AUTOSAR® and Non-AUTOSAR)	4 x SPI*	6 x SPI*	4 x SPI*	4 x SPI*	6 x SPI*
Security F/W Safety Software Framework Application Software	2 x 24-ch. 12-bit ADC	3 x 24-ch. 12-bit ADC	2 x 24-ch. 12-bit ADC	2 x 24-ch. 12-bit ADC	3 x 24-ch. 12-bit ADC
	2 x SAI (I ² S)				
	Quad SPI				
	MaxQFP-172				
	MaxQFP-100		MaxQFP-100	MaxQFP-100	
		MAPBGA-257			MAPBGA-257

S32K3 Family Features Part 3 Block Diagram



S32K3 Software Ecosystem Block Diagram



View additional information for [S32K3 Microcontrollers for General-Purpose](#).

Note: The information on this document is subject to change without notice.

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