



S32K3 Microcontrollers for Automotive General Purpose

S32K3

Last Updated: Dec 19, 2025

The S32K3 Family of 32-bit microcontrollers (MCUs) offers Arm® Cortex®-M7-based MCUs in single, dual and lockstep core configurations. S32K3 Family offers scalability in number of cores, memory and peripherals, ensuring high-performance and functional safety compliant with ISO 26262 up to ASIL D.

S32K3 Family provides a comprehensive end-to-end solution for development and production. S32K3 MCUs feature a hardware security engine (HSE) with NXP firmware, enable firmware over-the-air (FOTA) updates and include ISO 26262 compliant Real-Time Drivers (RTD) suitable for both AUTOSAR® and non-AUTOSAR applications.

Through compatibility with the NXP S32 Automotive Platform, S32K3 Family enables seamless software reuse and flexibility across applications in body, zone control and electrification.

S32K3 MCUs are available in various package types, including MAPBGA, LQFP and HDQFP, providing flexibility in integration and design. Also, the NXP HDQFP package reduces the package footprint by up to 55 % compared to a standard QFP package.

S32K3 Family Features Part 1 Block Diagram

Common Features	K310	K311	K312	K314
AEC-Q100, 125 °C, 3.3/5 V	1 x Arm® Cortex®-M7 @ 120 MHz			1 x Arm® Cortex®-M7 @ 160 MHz
HSE-B Crypto Security Engine	512 KB Flash	1 MB Flash	2 MB Flash	4 MB Flash
FOTA (Firmware Over-the-Air)	112 KB SRAM (incl. 96 KB TCM)	128 KB SRAM (incl. 96 KB TCM)	192 KB SRAM (incl. 96 KB TCM)	512 KB SRAM (incl. 96 KB TCM)
Low-Power Operating Modes and Peripherals (LPUART, FlexIO)	38/83 I/Os	38/83 I/Os	83/145 I/Os	142/218 I/Os
ASIL B/D Safety: (ECC Memories, MPU, CRC, Watchdogs)	12-ch eDMA			32-ch eDMA
	3 x CAN (FD)		6 x CAN (FD)	
eMIOS Timers Logic Control Unit Body Cross Triggering Unit Trigger Mux	2 x I ² C, 4 x UART(LIN)		2 x I ² C, 8 x UART(LIN)	2 x I ² C, 16 x UART(LIN)
	4 x SPI			6 x SPI
Debug/Trace (SWD/JTAG/ETB)	2 x 24ch 12-bit ADC			3 x 24ch 12-bit ADC
S32 Design Studio IDE S32 Configuration Tool	Analog Comparator		2 x Analog Comparator	3 x Analog Comparator
Real-Time Drivers (AUTOSAR® and Non-AUTOSAR)				2 x SAI (I ² S)
Security F/W Safety Software Framework Communication Stacks Application Software	LQFP-48			Quad SPI (4-bit data)
	HDQFP-100			
				HDQFP-172
Model-Based Design Toolbox				MAPBGA-257

S32K3 Family Features Part 2 Block Diagram

Common Features	K322	K324	K341	K342	K344
AEC-Q100, 125 °C, 3.3/5 V	2 x Arm® Cortex®-M7 @ 160 MHz		1 x LockStep Arm® Cortex®-M7 @ 160 MHz		
HSE-B Crypto Security Engine	2 MB Flash	4 MB Flash	1 MB Flash	2 MB Flash	4 MB Flash
FOTA (Firmware Over-the-Air)	256 KB SRAM (incl. 192 KB TCM)	512 KB SRAM (incl. 192 KB TCM)	256 KB SRAM (incl. 192 KB TCM)	256 KB SRAM (incl. 192 KB TCM)	512 KB SRAM (incl. 192 KB TCM)
Low-Power Operating Modes and Peripherals (LPUART, FlexIO)	80/142 I/Os	142/218 I/Os	80/142 I/Os	80/142 I/Os	142/218 I/Os
	32-ch eDMA				
ASIL B/D Safety: (ECC Memories, MPU, CRC, Watchdogs)	4 x CAN (FD)	6 x CAN (FD)	4 x CAN (FD)	4 x CAN (FD)	6 x CAN (FD)
	100 Mbit/s Ethernet (TSN)				
eMIOS Timers Logic Control Unit Body Cross Triggering Unit Trigger Mux	4 x UART(LIN)	16 x UART(LIN)	4 x UART(LIN)		16 x UART(LIN)
	2 x I ² C				
Debug/Trace (SWD/JTAG/ETB)	4 x SPI	6 x SPI	4 x SPI		6 x SPI
	2 x 24-ch 12-bit ADC	3 x 24-ch 12-bit ADC	2 x 24-ch 12-bit ADC		3 x 24-ch 12-bit ADC
S32 Design Studio IDE S32 Configuration Tool	2 x Analog Comparator	3 x Analog Comparator	2 x Analog Comparator		3 x Analog Comparator
Real-Time Drivers (AUTOSAR® and Non-AUTOSAR)	2 x SAI (I ² S)				
	Quad SPI (4-bit data)				
Security F/W Safety Software Framework Communication Stacks Application Software	HDQFP-100		HDQFP-100		
	HDQFP-172				
Model-Based Design Toolbox	MAPBGA-257		MAPBGA-257		

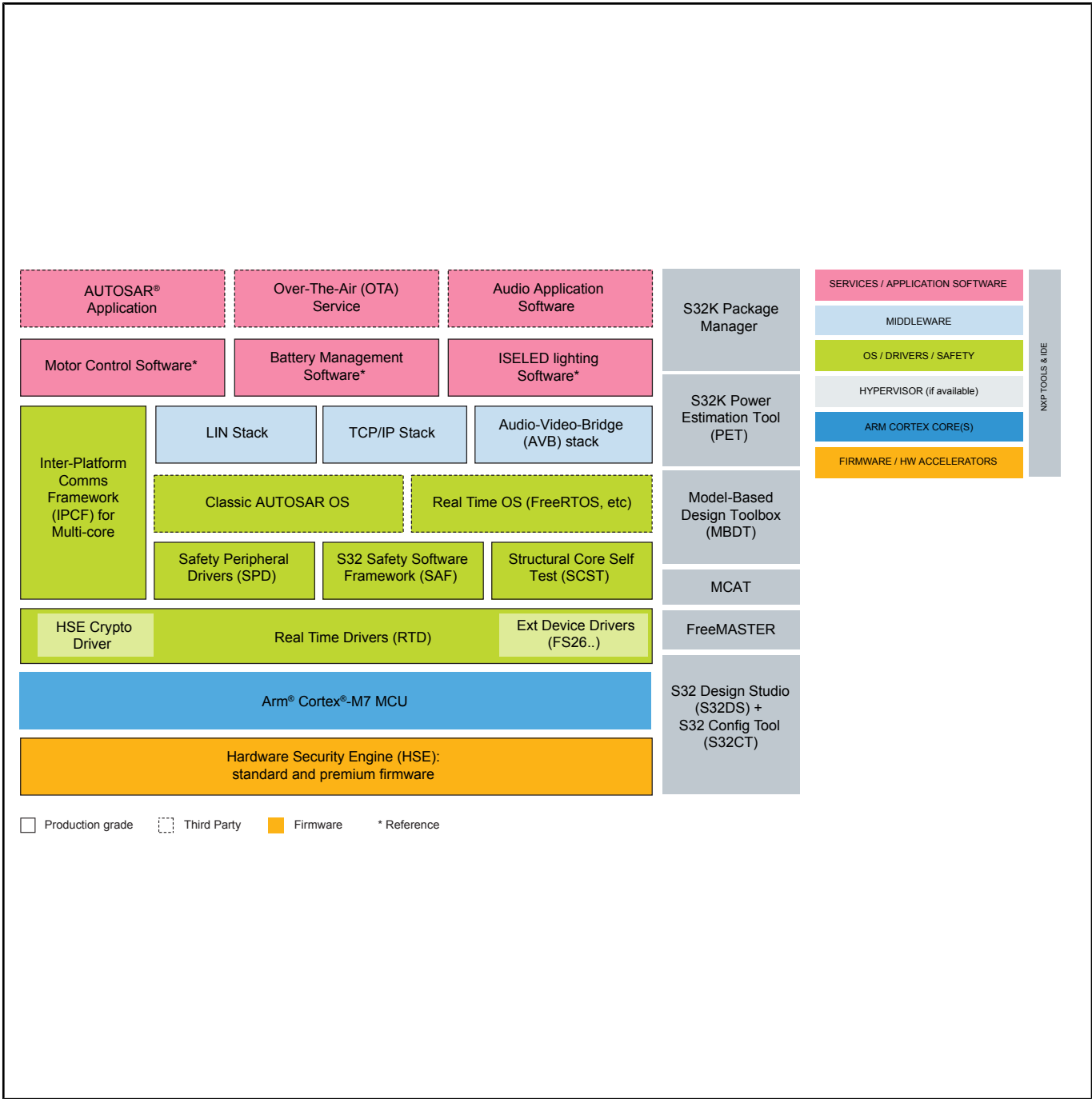
S32K3 Family Features Part 3 Block Diagram

Common Features	K364	K366	K374	K376	K394	K396
AEC-Q100, 125 °C, 3.3/5 V	1 x LockStep + 1 Arm® Cortex®-M7 @ 320 MHz		1 x LockStep + 2 x Split-Lock Arm® Cortex®-M7 @ 320 MHz			
HSE_B Crypto Security Engine	2 x motor control coprocessor (2x 16ch)			2 x motor control coprocessor (2x 32ch)		
FOTA (Firmware Over-the-Air)	4 MB Flash	6 MB Flash	4 MB Flash	6 MB Flash	4 MB Flash	6 MB Flash
Low-Power Operating Modes and Peripherals (LPUART, FlexIO)	704 KB SRAM (incl. 192 KB TCM)		800 KB SRAM (incl. 288 KB TCM)			
	127/ 209+8LVDS I/Os					
ASIL D Safety: (ECC Memories, MPU, CRC, Watchdogs)	64-ch eDMA with 32ch LockStep					
	6 x CAN (FD)					
eMIOS Timers Logic Control Unit Body Cross Triggering Unit Trigger Mux	100 Mbit/s Ethernet (AVB/TSN)					
	ZipWire					
	6 x SPI, 4x UART(LIN), 2 x I ² C					
Debug/Trace (SWD/JTAG/ETB)	2x 12-ch eFlexPWM with NanoEdge (8-ch each high-resolution PWM)					
S32 Design Studio IDE S32 Configuration Tool	2 x sigma-delta ADC with programmable DSP		4 x sigma-delta ADC with programmable DSP			
Real-Time Drivers (AUTOSAR® and Non-AUTOSAR)	4 x 12-bit SAR-ADC (48 inputs)		7 x 12-bit SAR-ADC (69 inputs)			
Security F/W Safety Software Framework Communication Stacks Application Software	2x Sine Wave Generator, 2 x Analog Comparator					
	Quad SPI (8-bit data width, SDR and DDR mode)					
	LQFP-EP-176					
ASIL-D SW Resolver, IPCF, MBDT	MAPBGA-289					

S32K3 Family Features Part 4 Block Diagram

Common Features	K328	K338	K348	K358	K388	K389*
AEC-Q100, 125 °C, 3.3/5 V	2 x Arm® Cortex®-M7 @ 240 MHz	3 x Arm® Cortex®-M7 @ 240 MHz	1 x LockStep Arm® Cortex®-M7 @ 240 MHz	1 x LockStep + 1 Arm® Cortex®-M7 @ 240 MHz	1 x LockStep + 3 or 2 x LockStep + 1 Arm® Cortex®-M7 @ 320 MHz	1 x LockStep + 3 or 2 x LockStep + 1 Arm® Cortex®-M7 @ 320 MHz
HSE-B Crypto Security Engine	8 MB Flash					12 MB Flash
FOTA (Firmware Over-the-Air)	1152 KB SRAM (incl. 192 TCM)	1152 KB SRAM (incl. 384 TCM)	1152 KB SRAM (incl. 192 TCM)	1152 KB SRAM (incl. 384 TCM)		2304 KB SRAM (incl. 384 TCM)
Low-Power Operating Modes and Peripherals (LPUART, FlexIO)	137/235 I/Os				202 I/Os	321 I/Os
ASIL B/D Safety: (ECC Memories, MPU, CRC, Watchdogs)	32-ch eDMA					
	8 x CAN (FD)					12 x CAN (FD)
eMIOS Timers Analog Comparator Logic Control Unit Body Cross Triggering Unit Trigger Mux	1 Gbit/s Ethernet (TSN)				2x 1 Gbit/s Ethernet (TSN)	
	2 x I ² C, 16 x UART(LIN)					
Debug/Trace (SWD/JTAG/ETB)	6 x SPI					
	3 x 24-ch 12-bit ADC					
S32 Design Studio IDE S32 Configuration Tool	2 x SAI (I ² S)					
Real-Time Drivers (AUTOSAR® and Non-AUTOSAR)	Quad SPI (8-bit data width, SDR and DDR mode)				Quad SPI (4-bit data)	
	uSDHC (SDIO)					
Security F/W Safety Software Framework Communication Stacks Application Software	HDQFP-EP-172					
	MAPBGA-289					
Model-Based Design Toolbox	*S32K389 feature set is under evaluation and subject to change.					MAPBGA-437

S32K3 Software Ecosystem Block Diagram



View additional information for [S32K3 Microcontrollers for Automotive General Purpose](#).

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.