Software Defined Radio Processor for V2X Communication

SAF5100

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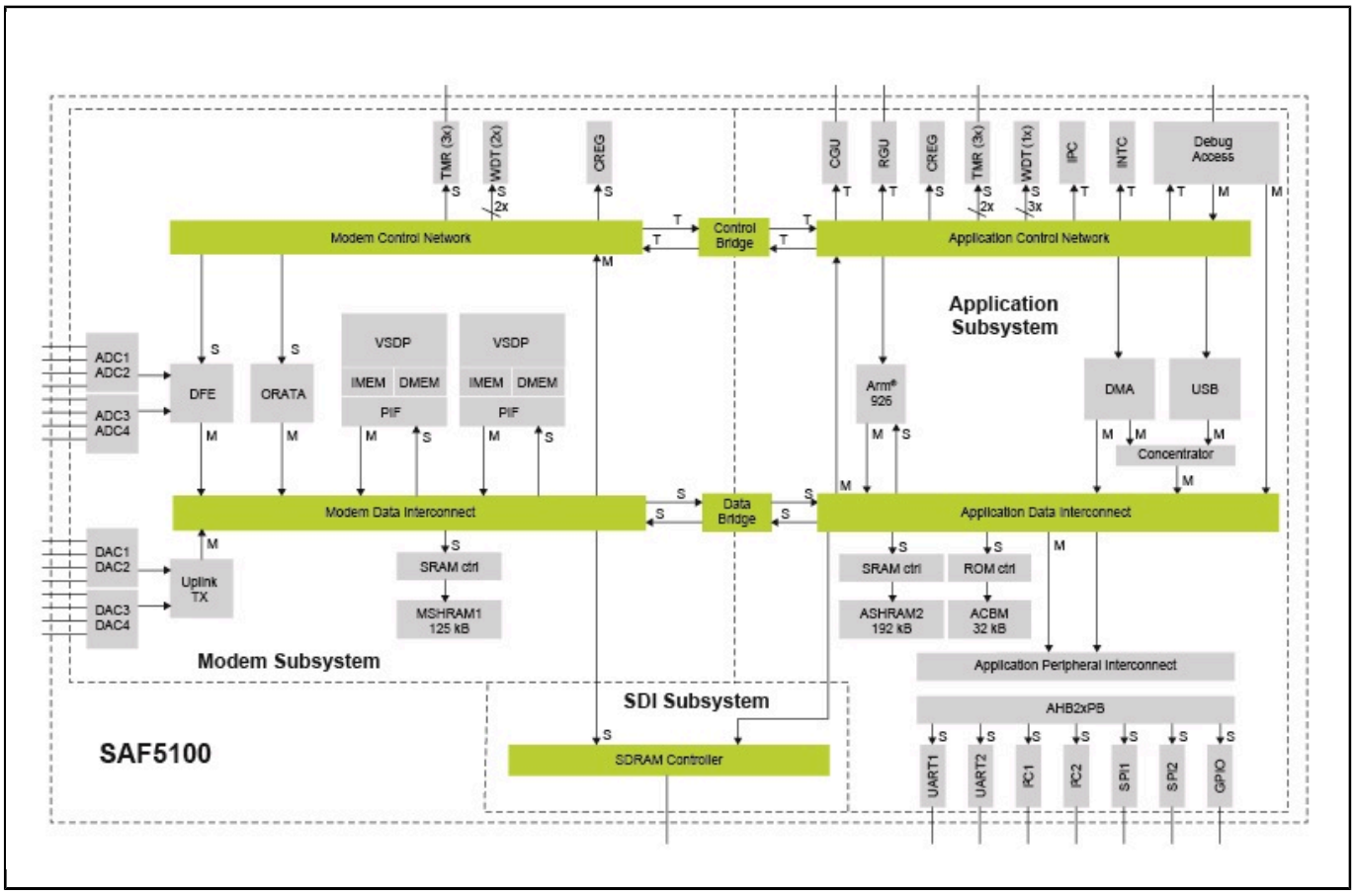
The SAF5100 is available in a Ball Grid Array (BGA) package occupying small Printed-Circuit Board (PCB) real estate and is suitable for multi-layer PCBs.

The SAF5100 this baseband processor includes Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) for interfacing with an external transceiver. Digital components included are:

- Digital Signal Processors (DSP) for advanced radio (de)modulation
- Hardware Accelerators (HWA) for IEEE 802.11p WiFi standard PHYsical layer (PHY) reception
- A microcontroller core for IEEE 1609.4 Medium Access Control (MAC)/Logical Link Control (LLC) processing
- Several standard interfaces such as Universal Serial Bus (USB) and SPI are included for connecting to an external host

The SAF5100 is available with an executable of a firmware comprising PHY/MAC (IEEE 802.11p and ETSI EN 302 663) and LLC (IEEE 1609.4 and ETSI EN 302 663) to be loaded into the RAM of the SAF5100.

Software Defined Radio Processor for V2X Communication Block Diagram Block Diagram



View additional information for Software Defined Radio Processor for V2X Communication.

Note: The information on this document is subject to change without notice.