



5 V, 3.3 V and 2.5 V dual UART, 5 Mbit/s (max.), with 64-byte FIFOs and 68 mode uP interfac

SC68C752B

Archived

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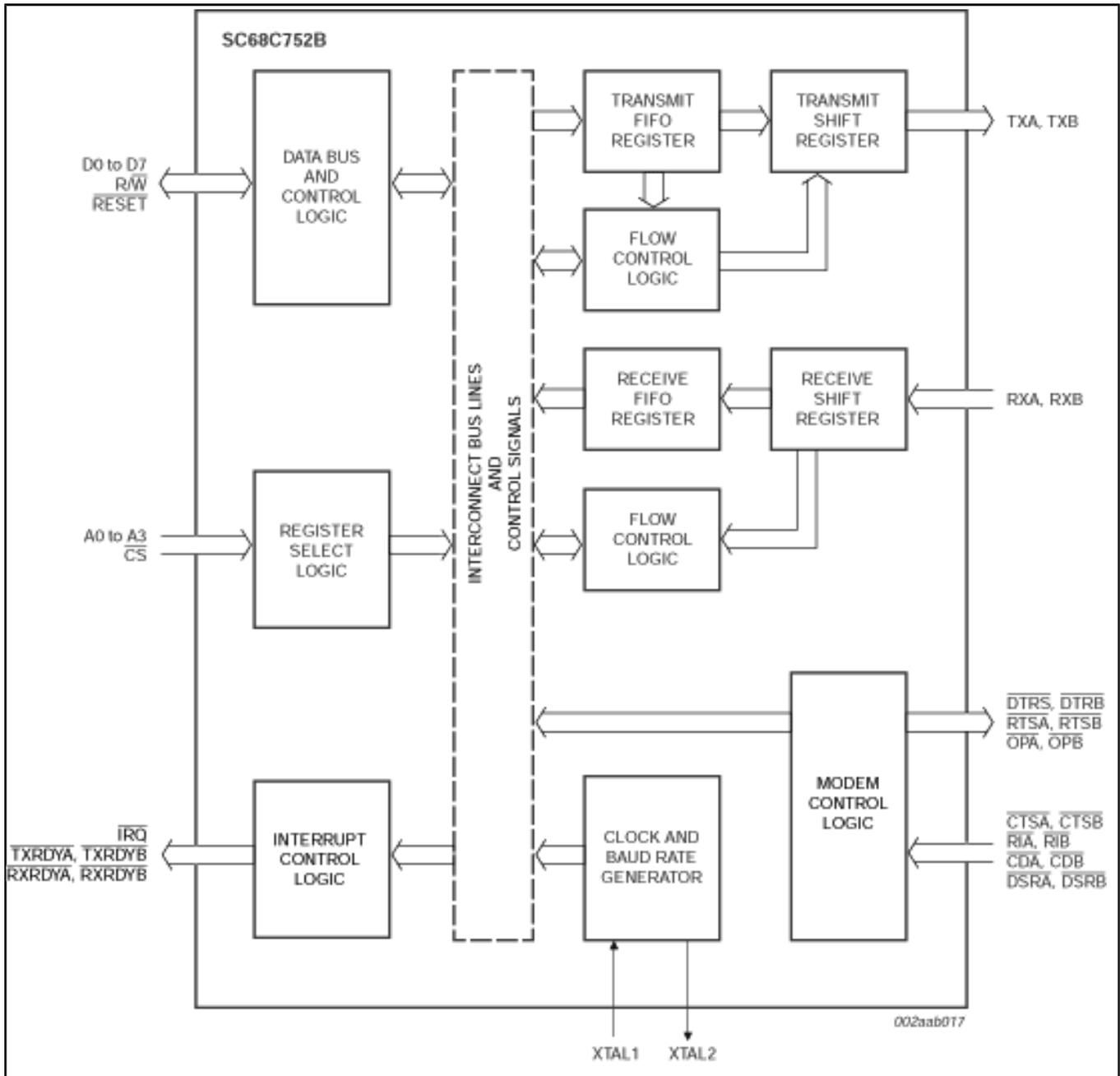
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The SC68C752B is a dual Universal Asynchronous Receiver/Transmitter (UART) with 64-byte FIFOs, automatic hardware/software flow control and data rates up to 5 Mbit/s. The SC68C752B offers enhanced features. It has a Transmission Control Register (TCR) that stores receiver FIFO threshold levels to start/stop transmission during hardware and software flow control. With the FIFO Rdy register, the software gets the status of TXRDYn/RXRDYn for all four ports in one access. On-chip status registers provide the user with error indications, operational status and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The UART transmits data, sent to it over the peripheral 8-bit bus, on the TXn signal and receives characters on the RXn signal. Characters can be programmed to be 5 bits, 6 bits, 7 bits or 8 bits. The UART has a 64-byte receive FIFO and transmit FIFO and can be programmed to interrupt at different trigger levels. The UART generates its own desired baud rate based upon a programmable divisor and its input clock. It can transmit even, odd or no parity and 1, 1.5 or 2 stop bits. The receiver can detect break, idle or framing errors, FIFO overflow and parity errors. The transmitter can detect FIFO underflow. The UART also contains a software interface for modem control operations and has software flow control and hardware flow control capabilities.

The SC68C752B is available in LQFP48 and HVQFN32 packages.

SC68C752BIB48, SC68C752BIBS Block Diagram



View additional information for [5 V](#), [3.3 V](#) and [2.5 V](#) dual UART, 5 Mbit/s (max.), with 64-byte FIFOs and 68 mode uP interfac.

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