3.3 V or 5.0 V Universal Asynchronous Receiver/Transmitter (UART)

SC28L91

アーカイブス

このページには、製造中止（生産終了）となった製品の情報が記載されています。本ページに記載されている仕様および情報は、過去の参考情報です。

Last Updated: Jul 24, 2023

The SC28L91 is a new member of the IMPACT family of Serial Communications Controllers. It is a single channel UART operating at 3.3 V and 5.0 V VCC, 8 or 16 byte FIFOs and is quite compatible with software of the SC28L92 and previous UARTs offered by Philips. It is a new part that is similar to our previous one channel part but is vastly improved. The improvements being: 16 character receiver, 16 character transmit FIFOs, watch dog timer for the receiver, mode register 0 is added, extended baud rate, over all faster bus and data speeds, programmable receiver and transmitter interrupts and versatile I/O structure. (The previous one channel part, SCC2691, is NOT being discontinued.)

Pin programming will allow the device to operate with either the Motorola or Intel bus interface. Bit 3 of the MR0 register allows the device to operate in an 8-byte FIFO mode if strict compliance with an 8-byte FIFO structure is required.

The Philips Semiconductors SC28L91 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter channel in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system with modem and DMA interface.

The operating mode and data format of the channel can be programmed independently. Additionally, the receiver and transmitter can select its operating speed as one of 28 fixed baud rates; a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

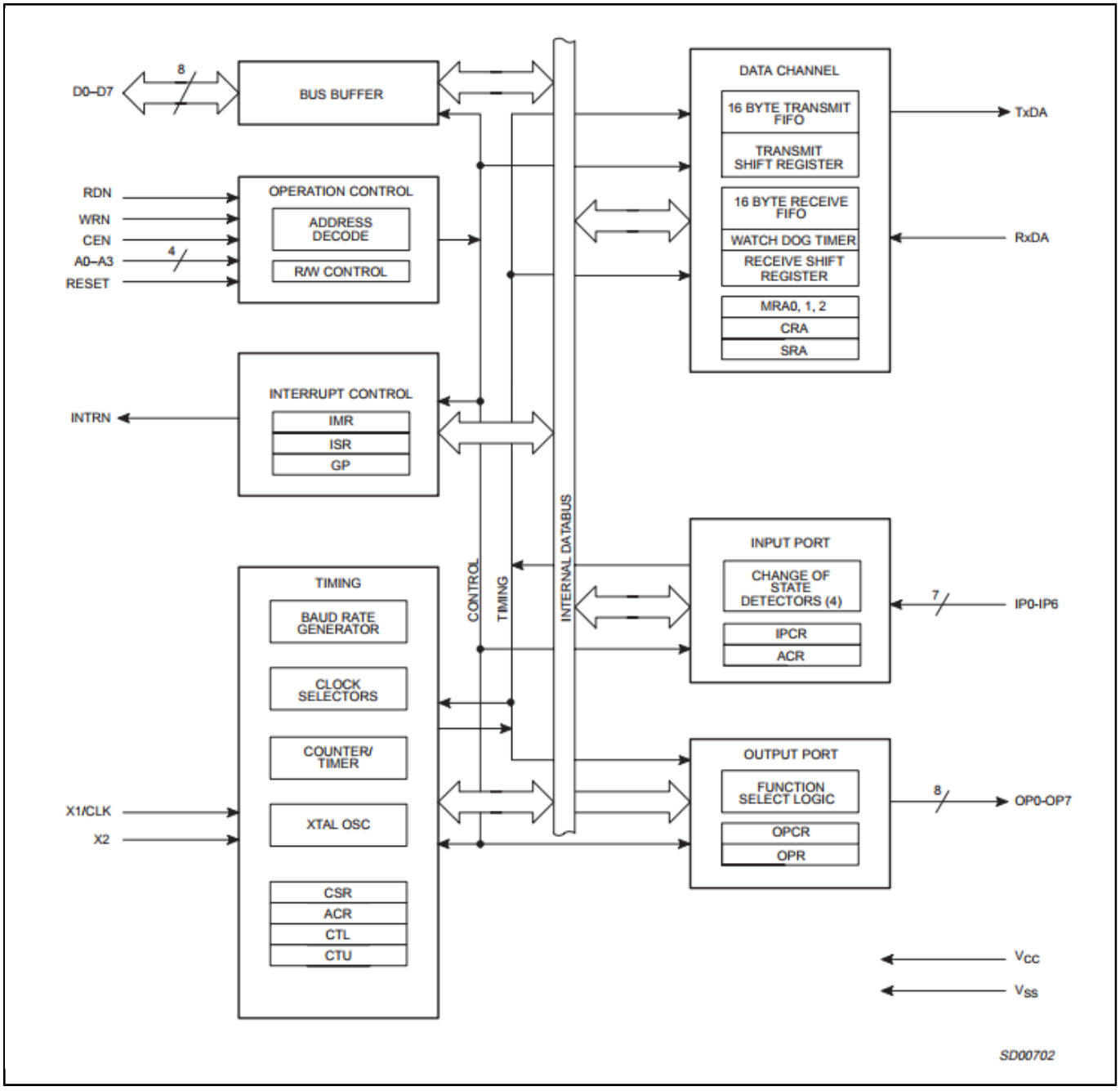
The receiver and transmitter is buffered by 8 or 16 character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven

systems. In addition, a flow control capability is provided via RTS/CTS signaling to disable a remote transmitter when the receiver buffer is full.

DMA interface is and other general purpose signals are provided on the SC28L91 via a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general-purpose ports or can be assigned specific functions (such as clock inputs or status/ interrupt outputs, FIFO conditions) under program control.

The SC28L91 is available in two package versions: a 44-pin PLCC and 44-pin plastic quad flat pack (PQFP).

SC28L91 Block Diagram Block Diagram



View additional information for 3.3 V or 5.0 V Universal Asynchronous Receiver/Transmitter (UART).

Note: The information on this document is subject to change without notice.

---

www.nxp.com