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Exploring Options for DDR Memory Interleaving

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Objective

Discover benefits of interleaving and all the available options for programming interleaving on the DDR controller for devices with single and dual memory controllers.

- Chip select interleaving
- Memory controller interleaving
- Difference between cache line, page, bank and super bank interleaving
- How to program the memory mapped registers for each type of interleaving

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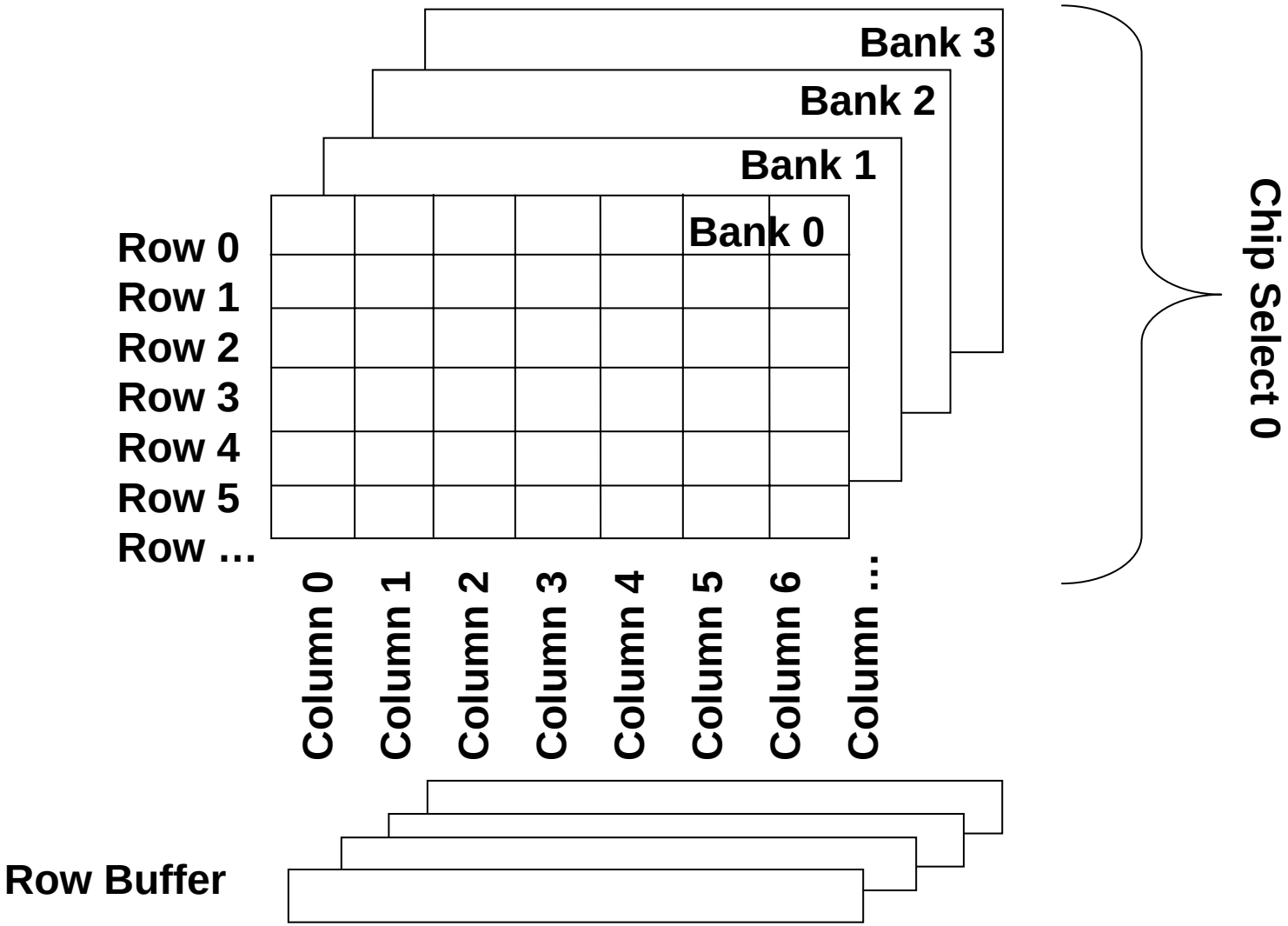
Agenda

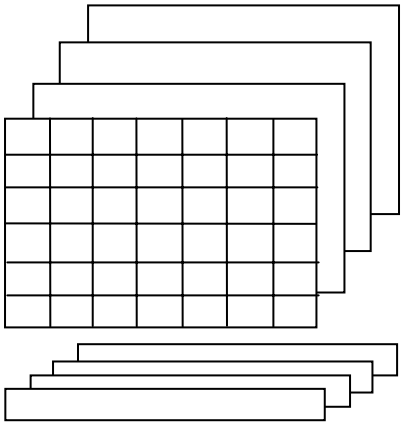
1. DDR memory space organization overview
2. Review components of an address issued to DDR SDRAM
3. Discuss interleaving with a single memory controller
   - Chip Select (Bank) Interleaving
4. Discuss interleaving with dual memory controllers
   - Chip Select (Bank) Interleaving
   - Memory Controller Interleaving
     - Cache line interleaving
     - Page interleaving
     - Bank interleaving
     - Super-bank interleaving

Memory Space Organization

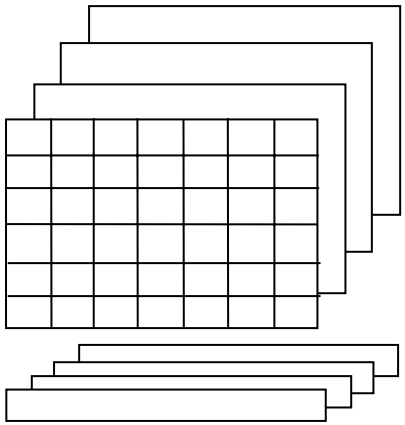


Memory Space Organization

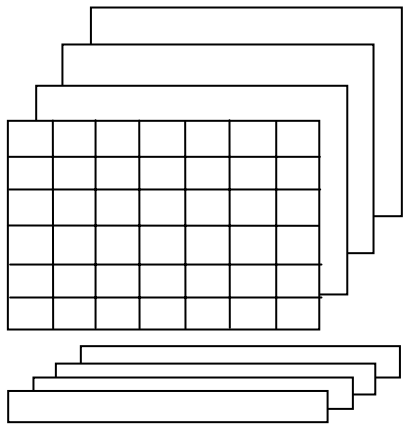
Chip Select 0



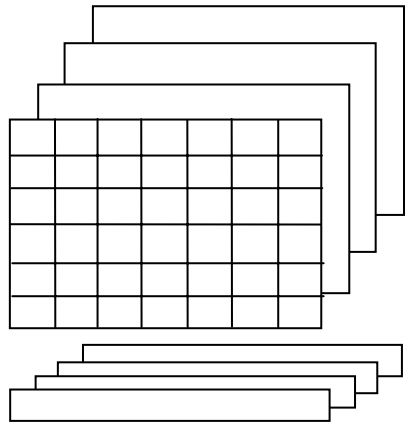
Chip Select 1



Chip Select 2



Chip Select 3



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Components of an Address

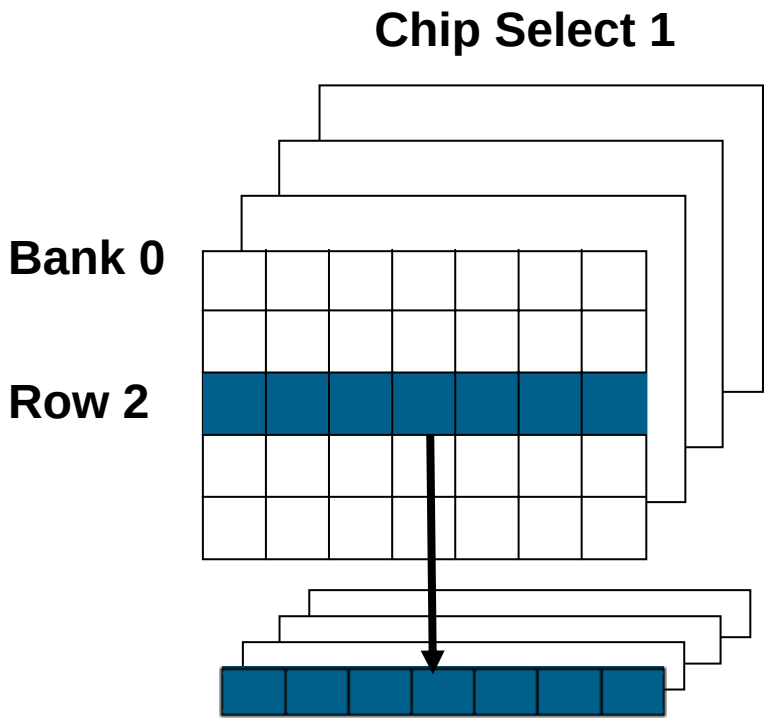
- Byte offset (O)—Always 3 bits
- Column select (C)—Varies depending on device size and memory type
- Bank select (B)—2 or 3 bits, depending on device size (4 or 8 sub-banks)
- Row select (R)—Varies depending on device size
- Chip select (S)—1 or 2 bits, depending on number chip selects used (1-4)

For example, a device with 32-bit address space, one memory controller, 4 chip selects, 14 rows, 10 columns and 4 sub-banks would use the bit allocations shown in the figure below.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
-	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	B	B	C	C	C	C	C	C	C	C	C	C	O	O	O

Stage One of a DRAM Read/Write Operation

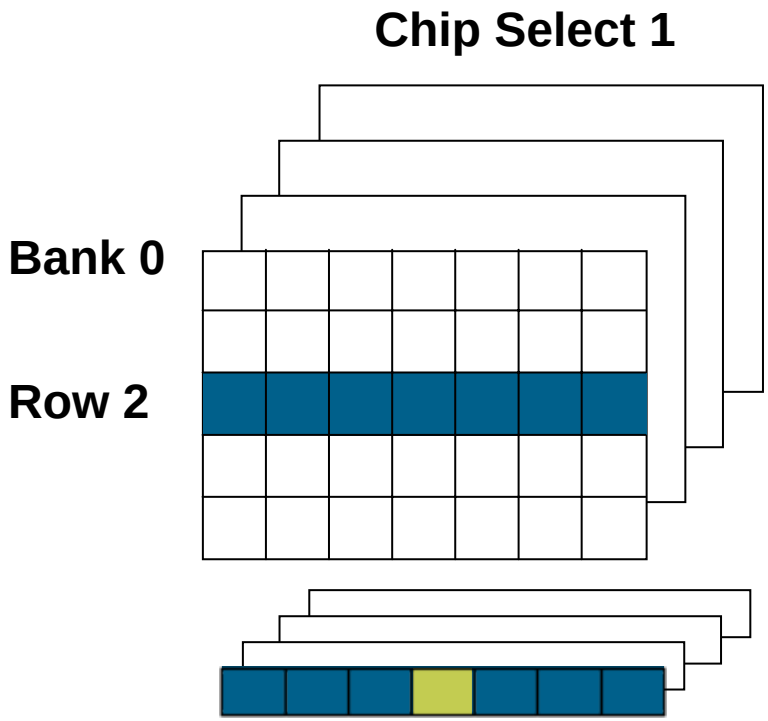
1. **Active Command** – Chip Select (S bits), Bank (B bits) and Row (R bits) of address are used to open a page of memory into a buffer so that a *read* or *write* can occur (one page is usually 1K)



Stage Two of a DRAM Read/Write Operation

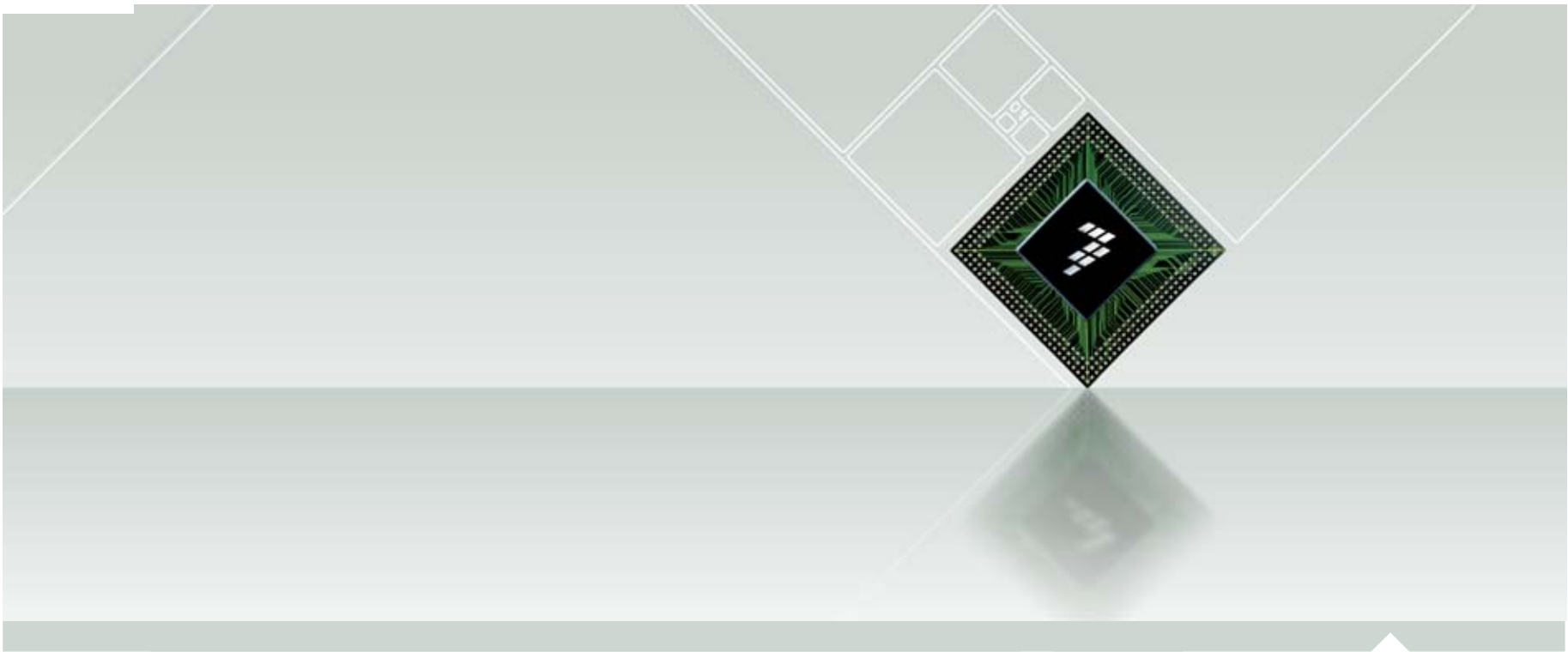
2. **Read/Write** – Columns (C bits) are used during the *read/write* command to point to the specific address within an open page for the read/write operation

   Pages remain open in the buffer until a different page needs to be opened to access a different address.



Overview of Interleaving

- Interleaving re-arranges the address bits such that the probability of hitting an open page is more likely
- Pages remain open in the buffer until a different page needs to be opened to access a different address. Reducing the number of times pages are opened and closed increases performance
- Instead of writing software that can predict which pages are open at certain times to increase *read/write* address hits, hardware can help do this.



Interleaving with a Single Memory Controller

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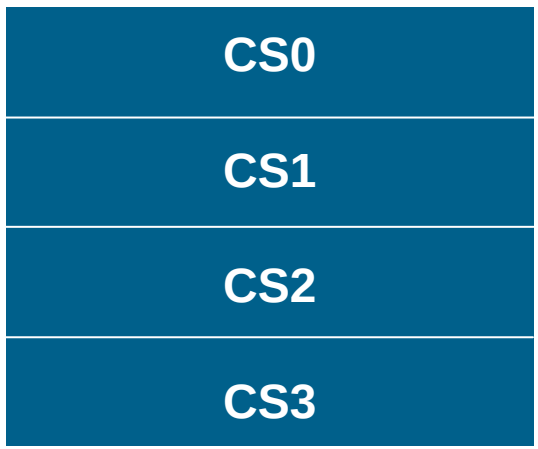
Chip Select Interleaving

- For devices that have a single memory controller, Chip Select Interleaving is the only type of interleaving available.
- The memory controller can be programmed to enable up to four chip selects.
- Chip Select Interleaving controls how these four chip selects are interleaved within the memory controller.



Components of an Address with Interleaving

Without Interleaving:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
-	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	B	B	C	C	C	C	C	C	C	C	C	C	O	O	O

With Chip Select Interleaving:

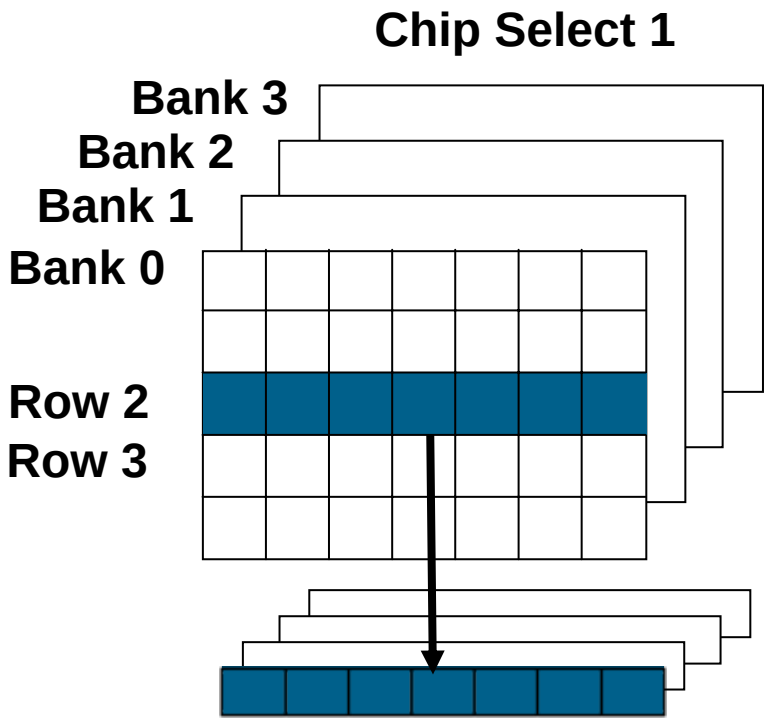
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	S	S	B	B	C	C	C	C	C	C	C	C	C	C	O	O	O

When chip select interleaving is enabled, the memory controller automatically changes the arrangements of address components by moving the chip select bits to the left of the sub-bank bits.

Open and Closing Pages

Any change to an address that only affects the Chip Select (S) bits or Bank (B) bits does not require the page to be closed and re-opened.

Any change to the Row (R) bits causes the open page to be closed and a new one to be opened.



Benefit of Interleaving

Chip Select Interleaving creates a larger continuous memory space of open pages to operate within which improves performance.

Without Interleaving:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
-	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	B	B	C	C	C	C	C	C	C	C	C	C	O	O	O

Address space = 0x0000_XXXX **2^16 = 64 Kbit**

With Chip Select Interleaving:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	S	S	B	B	C	C	C	C	C	C	C	C	C	C	O	O	O

Address space = 0x0000X_XXXX **2^18 = 256 Kbit**

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Transaction Flow with Interleaving

- Reducing the number of times a page has to be closed and opened actually reduces the number of active commands that have to be sent.
- This allows the DDR controller to use the *read/write* stage of a transaction more often.

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Chip Select Interleaving Programming Constraints

- The size of each chip select participating in chip select interleaving must be equal.
- The start and end address of the combined size of all the chip selects participating in interleaving must be entered in the lowest numbered CSn_BNDS register.
- LAW must be set up to target interleaved memory.
- The type of chip select interleaving must be indicated in the *DDR_SDRAM_CFG[BA_INTLV_CTL]* register.

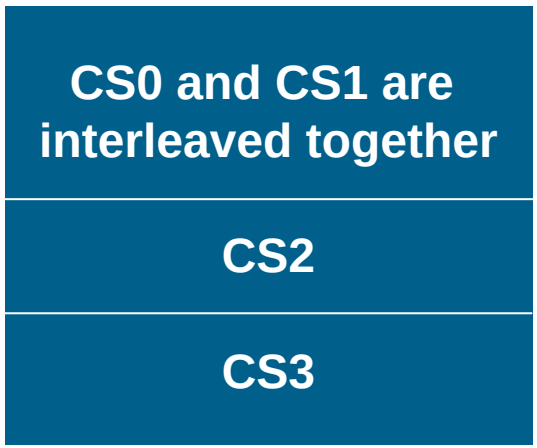
Chip Select Interleaving Options

There are four options within Chip Select Interleaving:

1. External memory chip selects 0 and 1 are interleaved
2. External memory chip selects 2 and 3 are interleaved
3. External memory chip selects 0 and 1 are interleaved together and chip selects 2 and 3 are interleaved together
4. External memory chip selects 0 through 3 are all interleaved together

Interleaving Chip Selects 0 and 1

DDR_SDRAM_CFG[BA_INTLV_CTL] = 1000000



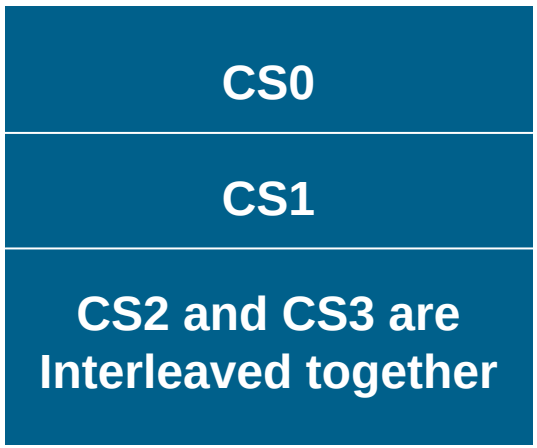
Interleaving Chip Selects 0 and 1

Table 1. Register Setting for Interleaving Banks 0 and 1

Register	Field	Bit Setting	Notes
DDR_SDRAM_CFG	[BA_INTLV_CTL]	1000000	External memory banks 0 and 1 are interleaved
CS0_CONFIG	[CS_0_EN]	1	Chip Select 0 is active and assumes the state set in CS0_BNDS
	All Other Fields Used	User Defined	All other fields in CS0_CONFIG are used
CS1_CONFIG	[ODT_RD_CFG]	User Defined	All fields in CS0_CONFIG override all fields in CS1_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_WR_CFG]	User Defined	
CS2_CONFIG	All Fields Used	User Defined	All fields in CS2_CONFIG are used if the third chip select is enabled
CS3_CONFIG	All Fields Used	User Defined	All fields in CS3_CONFIG are used if the fourth chip select is enabled
CS0_BNDS	All Fields Used	User Defined	All fields in CS0_BNDS override all fields in CS1_BNDS. The start and end address in CS0_BNDS must be set to the combined interleaved memory space.
CS1_BNDS	All Fields Unused	—	
CS2_BNDS	All Fields Used	User Defined	All fields in CS2_BNDS are used if the third chip select is enabled in CS2_CONFIG
CS3_BNDS	All Fields Used	User Defined	All fields in CS3_BNDS are used if the fourth chip select is enabled in CS3_CONFIG

Interleaving Chip Selects 2 and 3

DDR_SDRAM_CFG[BA_INTLV_CTL] = 0100000



Interleaving Chip Selects 2 and 3

Table 2. Register Setting for Interleaving Banks 2 and 3

Register	Field	Bit Setting	Notes
DDR_SDRAM_CFG	[BA_INTLV_CTL]	0100000	External memory banks 2 and 3 are interleaved
CS0_CONFIG	All Fields Used	User Defined	All fields in CS0_CONFIG are used if the first chip select is enabled
CS1_CONFIG	All Fields Used	User Defined	All fields in CS1_CONFIG are used if the second chip select is enabled
CS2_CONFIG	[CS_2_EN]	1	Chip Select 2 is active and assumes the state set in CS2_BNDS
	All Other Fields Used	User Defined	All other fields in CS2_CONFIG are used
CS3_CONFIG	[CS_3_EN]	Don't care	All fields in CS2_CONFIG override all fields in CS3_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_RD_CFG]	User Defined	
	[ODT_WR_CFG]	User Defined	
CS0_BNDS	All Fields Used	User Defined	All fields in CS0_BNDS are used if the first chip select is enabled in CS0_CONFIG
CS1_BNDS	All Fields Used	User Defined	All fields in CS1_BNDS are used if the second chip select is enabled in CS1_CONFIG
CS2_BNDS	All Fields Used	User Defined	All fields in CS2_BNDS override all fields in CS3_BNDS. The start and end address in CS2_BNDS must be set to the combined interleaved memory space.
CS3_BNDS	All Fields Unused	—	

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Interleaving CS 0 and 1 Together and CS 2 and 3 Together

DDR_SDRAM_CFG[BA_INTLV_CTL] = 1100000

CS0 and CS1 are Interleaved together

CS2 and CS3 are Interleaved together

Interleaving CS 0 and 1 Together and CS 2 and 3 Together

Table 3. Register Setting for Interleaving Banks 0 and 1 as well as Banks 2 and 3

Register	Field	Bit Setting	Notes
DDR_SDRAM_CFG	[BA_INTLV_CTL]	1100000	External memory banks 0 and 1 are interleaved together and banks 2 and 3 are interleaved together
CS0_CONFIG	[CS_0_EN]	1	Chip Select 0 is active and assumes the state set in CS0_BNDS
	All Other Fields Used	User Defined	All other fields in CS0_CONFIG are used
CS1_CONFIG	[ODT_RD_CFG]	User Defined	All fields in CS0_CONFIG override all fields in CS1_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_WR_CFG]	User Defined	
CS2_CONFIG	[CS_2_EN]	1	Chip Select 2 is active and assumes the state set in CS2_BNDS
	All Other Fields Used	User Defined	All other fields in CS2_CONFIG are used
CS3_CONFIG	[ODT_RD_CFG]	User Defined	All fields in CS2_CONFIG override all fields in CS3_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_WR_CFG]	User Defined	
CS0_BNDS	All Fields Used	User Defined	All fields in CS0_BNDS override all fields in CS1_BNDS. The start and end address in CS0_BNDS must be set to the combined interleaved memory space shared between CS0 and CS1.
CS1_BNDS	All Fields Unused	—	
CS2_BNDS	All Fields Used	User Defined	All fields in CS2_BNDS override all fields in CS3_BNDS. The start and end address in CS2_BNDS must be set to the combined interleaved memory space shared between CS2 and CS3.
CS3_BNDS	All Fields Unused	—	

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Interleaving Chip Select 0 through 3

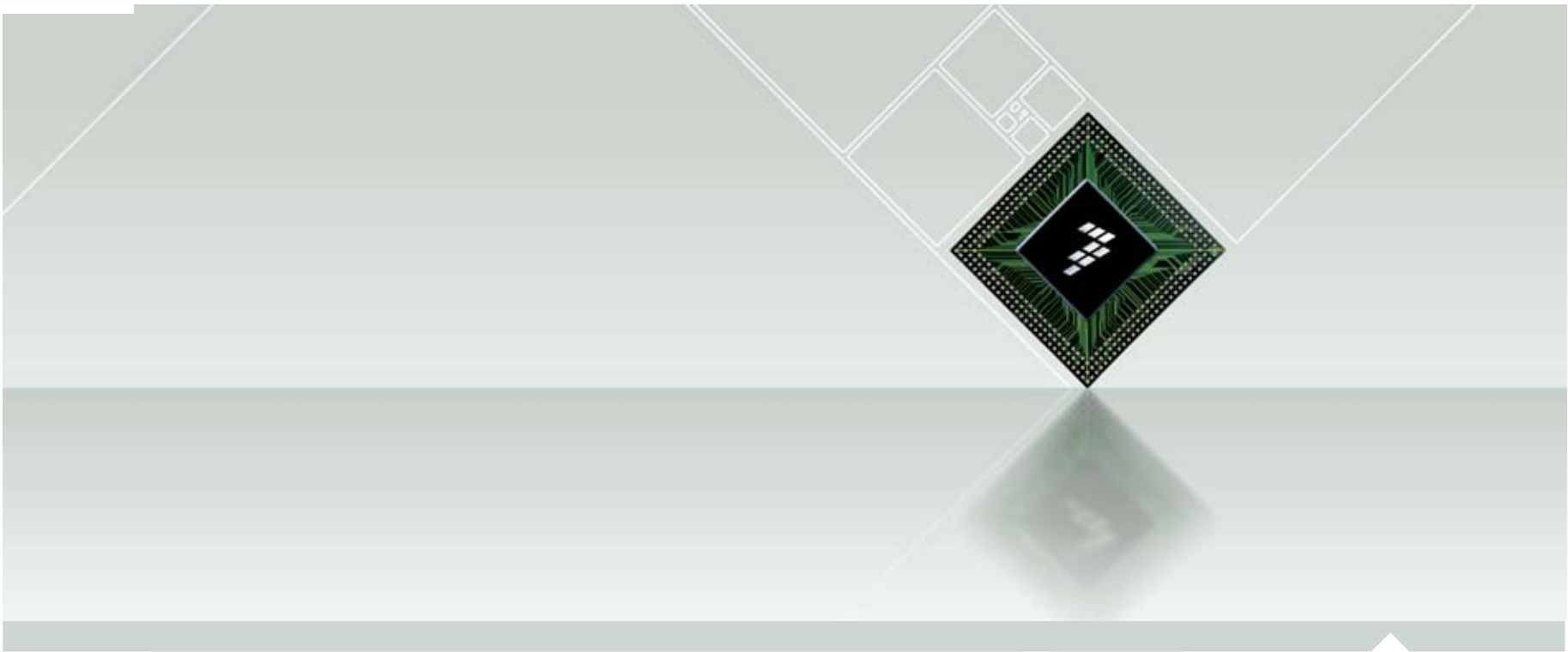
DDR_SDRAM_CFG[BA_INTLV_CTL] = xx00100

CS0 through CS3 are Interleaved together

Interleaving Chip Select 0 through 3

Table 4. Register Setting for Interleaving Banks 0 through 3

Register	Field	Bit Setting	Notes
DDR_SDRAM_CFG	[BA_INTLV_CTL]	xx00100	External memory banks 0 through 3 are all interleaved together
CS0_CONFIG	[CS_0_EN]	1	Chip Select 0 is active and assumes the state set in CS0_BNDS
	All Other Fields Used	User Defined	All other fields in CS0_CONFIG are used
CS1_CONFIG	[ODT_RD_CFG]	User Defined	All fields in CS0_CONFIG override all fields in CS1_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_WR_CFG]	User Defined	
CS2_CONFIG	[ODT_RD_CFG]	User Defined	All fields in CS0_CONFIG override all fields in CS2_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_WR_CFG]	User Defined	
CS3_CONFIG	[ODT_RD_CFG]	User Defined	All fields in CS0_CONFIG override all fields in CS3_CONFIG with the exception of [ODT_RD_CFG] and [ODT_WR_CFG]
	[ODT_WR_CFG]	User Defined	
CS0_BNDS	All Fields Used	User Defined	All fields in CS0_BNDS override all fields in CS1_BNDS, CS2_BNDS and CS3_BNDS. The start and end address in CS0_BNDS must be set to the combined interleaved memory space.
CS1_BNDS	All Fields Unused	—	
CS2_BNDS	All Fields Unused	—	
CS3_BNDS	All Fields Unused	—	



Interleaving with Dual Memory Controllers

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Types of Interleaving

- Chip Select Interleaving
  - Can be enabled on either or both controllers
  - Behaves exactly like single memory controller interleaving
  - Benefits are exactly the same as a single memory controller
- Memory Controller Interleaving
  - Only available with dual memory controllers
- Chip Select and Memory Controller Interleaving combined

Components of an Address

- Byte offset (O)—Always 3 bits
- Column select (C)—Varies depending on device size and memory type
- Bank select (B)—2 or 3 bits, depending on device size (4 or 8 sub-banks)
- Row select (R)—Varies depending on device size
- Chip select (S)—1 or 2 bits, depending on number chip selects used (1-4)
- Memory Controller (M) — 1 bit, depending on number of memory controllers used

For example, a device with 36-bit address space, two memory controllers, 4 chip selects, 14 rows, 10 columns and 4 sub-banks would use the bit allocations shown in the figure below.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	M	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	B	B	C	C	C	C	C	C	C	C	C	C	O

Memory Controller Interleaving Types

- The memory controller (M) bit location in the address is programmable
  - Cache-line interleaving
  - Page interleaving
  - Bank interleaving
  - Super-bank interleaving
- Memory Controller Interleaving is combined with Chip Select interleaving if multiple chip selects are desired to participate in memory controller interleaving
  - Without chip select interleaving, only CS0 from memory controller 1 will be interleaving with CS0 from memory controller 2

Cache-line Interleaving

- Bit 29 (64 byte cache line devices)/30 (32 byte cache line devices) of the 36-bit physical address is used to select the memory controller
- Every cache-line transfer switches between each memory controller to increase bandwidth which improves performance
- Re-arranging the M bit also increases the continuous memory space by a power of 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	B	B	C	C	C	C	C	C	C	C	M	C	C	O

- With Chip Select Interleaving Enabled

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	S	S	B	B	C	C	C	C	C	C	C	C	M	C	C	O

Page Interleaving

- The bit used to select the memory controller is the bit to the left of the highest-order column bits
- Every page line transfer switches between each memory controller
- Re-arranging the M bit also increases the continuous memory space by a power of 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	B	B	M	C	C	C	C	C	C	C	C	C	C	O

- With Chip Select Interleaving Enabled

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	S	S	B	B	M	C	C	C	C	C	C	C	C	C	C	O

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Bank Interleaving

- The bit used to select the memory controller is the bit to the left of the bank select bits, which are to the left of the highest-order column bits
- Every bank transfer switches between each memory controller

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	S	S	R	R	R	R	R	R	R	R	R	R	R	R	R	R	M	B	B	C	C	C	C	C	C	C	C	C	C	O

- With Chip Select Interleaving Enabled

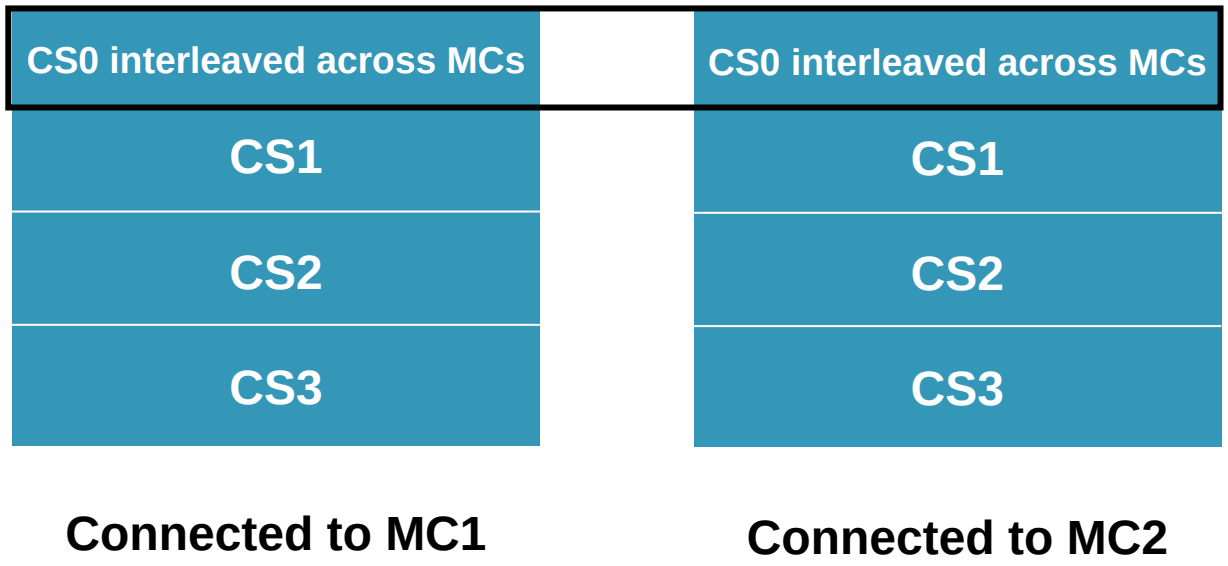
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	S	S	M	B	B	C	C	C	C	C	C	C	C	C	C	O

Super-bank Interleaving

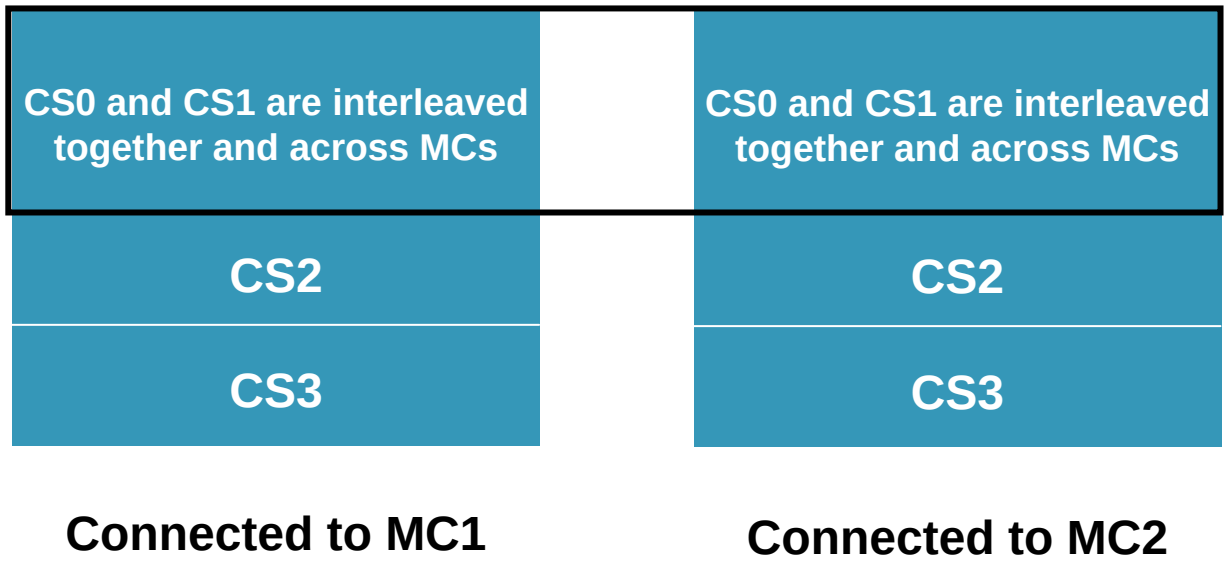
- The bit used to select the memory controller is the bit to the left of the Chip Select interleaved bits
- Chip Select Interleaving must be enabled with this mode
- Very similar to Bank interleaving with Chip Select interleaving enabled
  - Difference is which bit is used to switch between memory controllers

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33-35
-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	M	S	S	B	B	C	C	C	C	C	C	C	C	C	C	O

Memory Controller Interleaving Only



...emory Controller and Chip Select Interleaving Combinations



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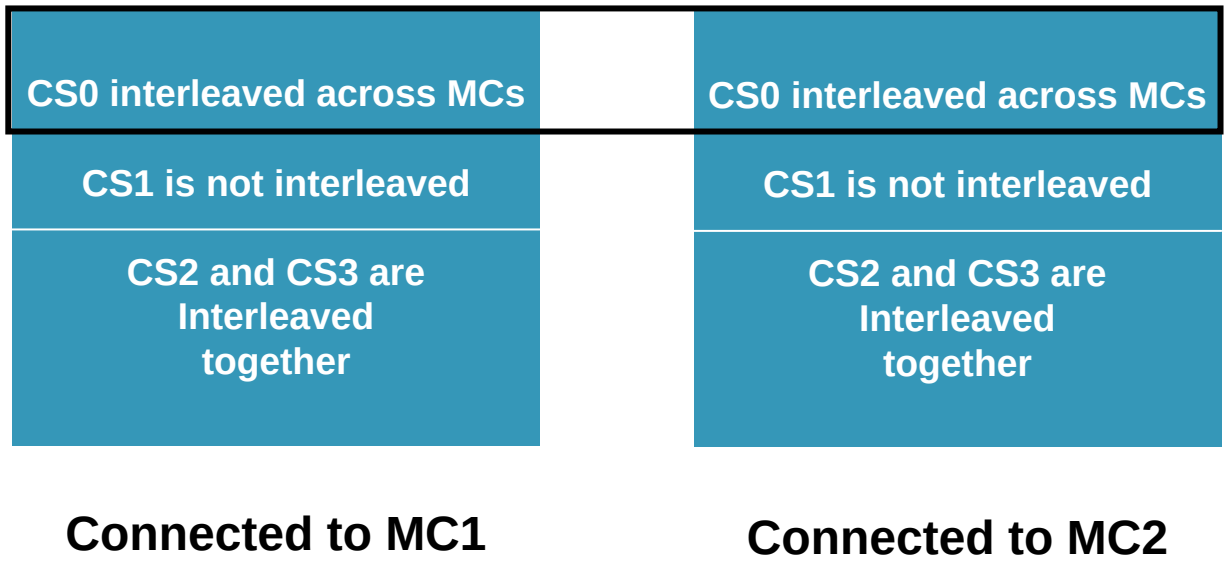

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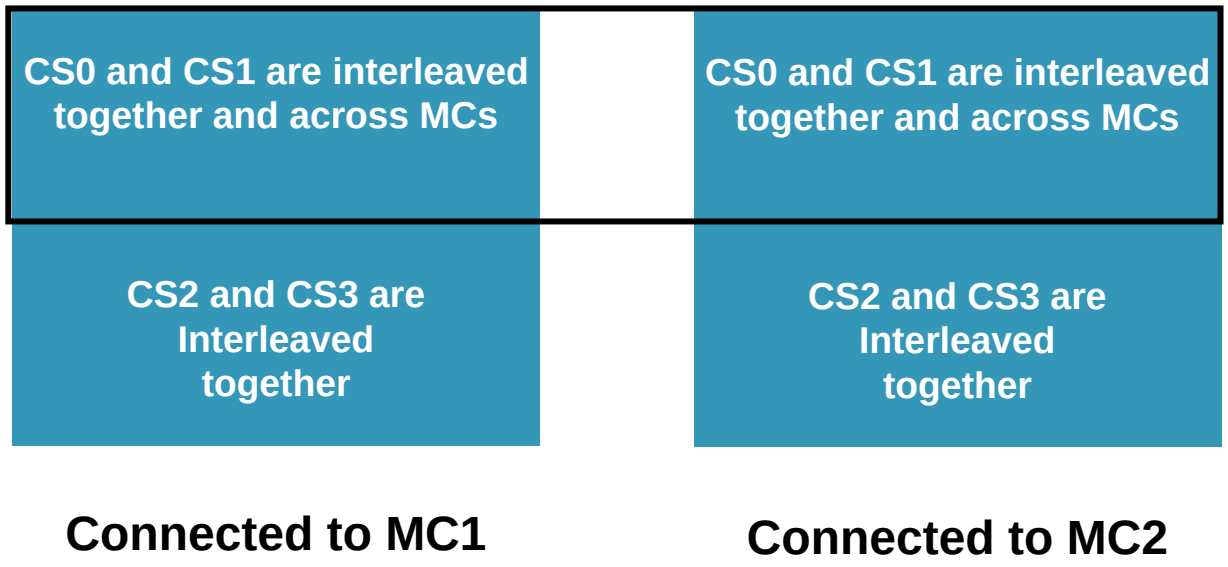

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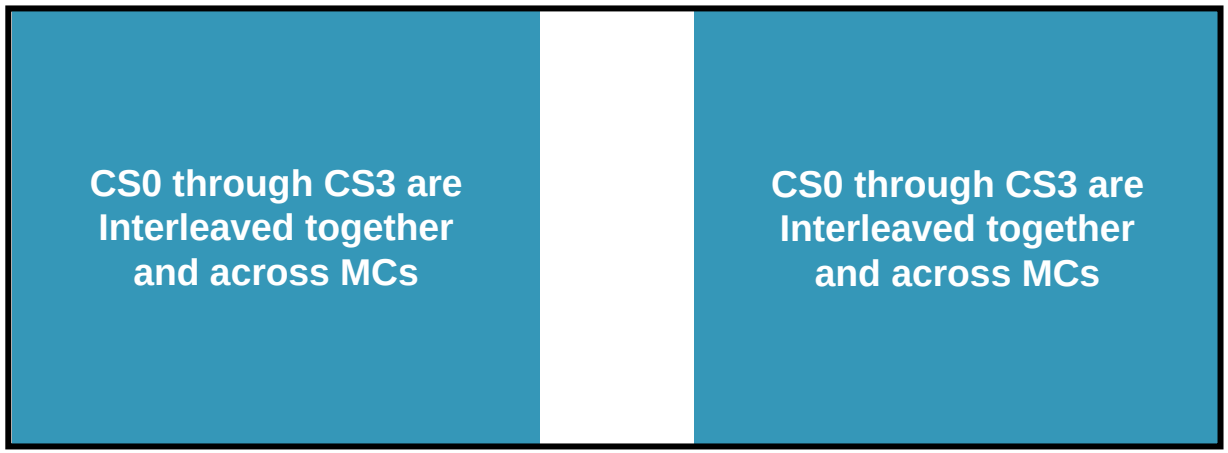

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Memory Controller Interleaving Programming Constraints

- CS0 of both memory controllers must be included in the two memory controller interleaving.
- The interleaved DDR LAW must be programmed for the memory space interleaved between the two memory controllers.
- A LAW for each memory controller must be programmed for the memory space not interleaved between the memory controllers.
- The size of chip selects participating in interleaving must be equal.
- The start and end address of combined size of all the chip selects participating in interleaving must be entered in the *CS0_BNDS* register of both memory controllers.

...ory Controller Interleaving Programming Constraints (cont.)

- The combined memory space participating in the two memory controller interleaving must be continuous.
- When chip selects other than CS0 are to be interleaved, the chip selects must be combined by setting the correct type of chip select interleaving in the *DDR_SDRAM_CFG[BA_INTLV_CTL]* register.
- Finally the memory controller interleaving must be enabled and its type selected in the *CS0_CONFIG* register of both memory controllers.

Selecting the Type of Interleaving

Determining which type of interleaving will provide the best performance is achieved by examining the specific application under the available interleaving types and letting the performance results point to the best type.

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Resources

- **AN3939** “DDR Interleaving for PowerQUICC and QorIQ Processors”
  - http://cache.freescale.com/files/32bit/doc/app_note/AN3939.pdf?fpsp=1&WT_TYPE=Application Notes&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation


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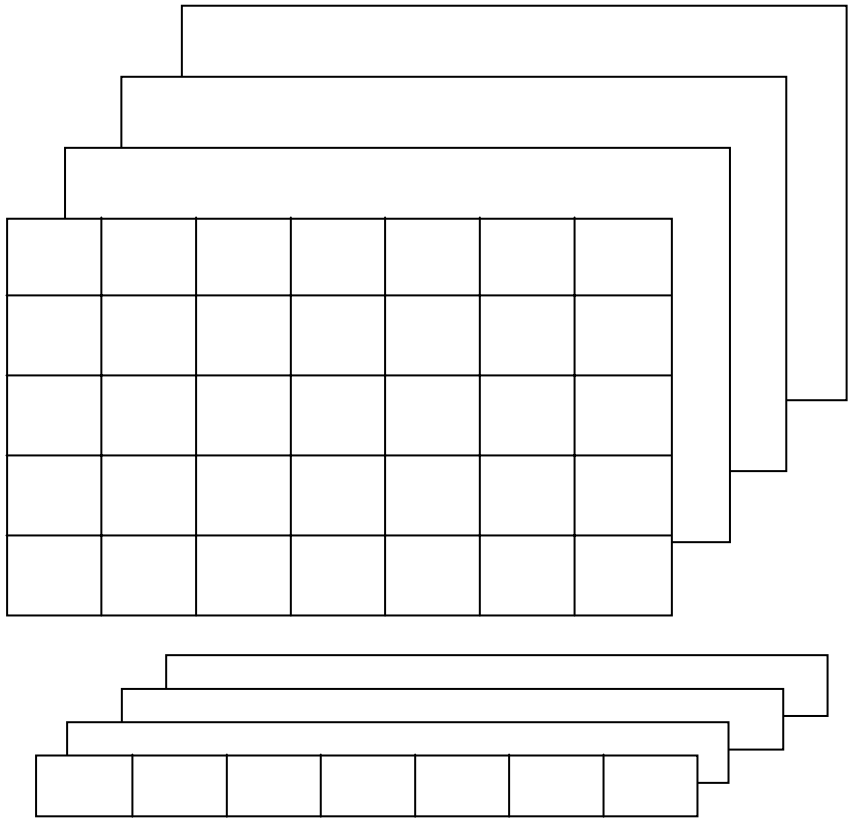
Memory Space Organization

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