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Introduction to Freescale's New RapidIO® Interface and Technology and Applicable Use Cases

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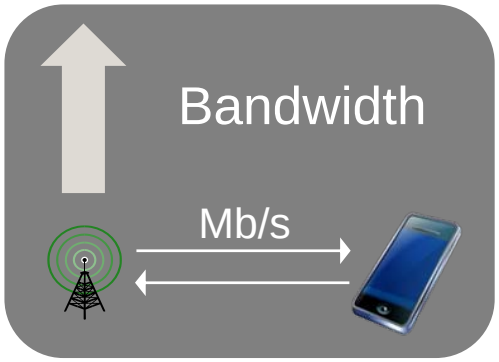
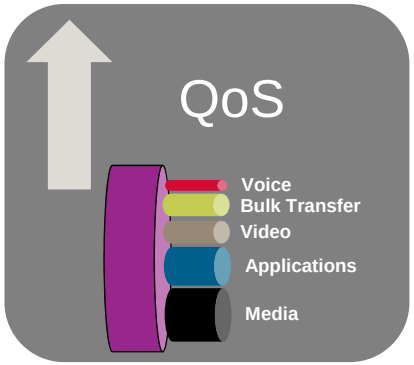
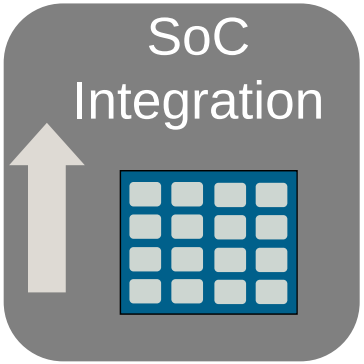
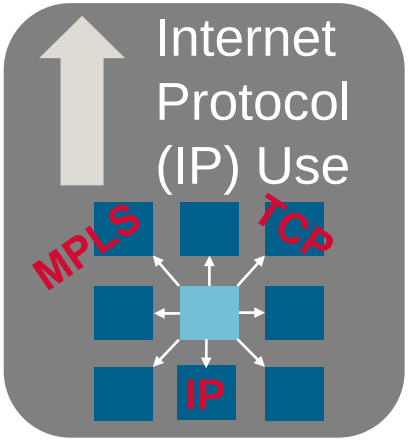
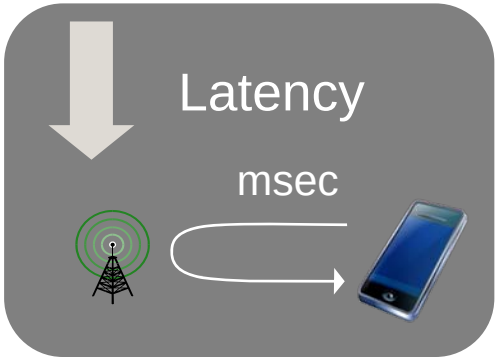
BTS Trends

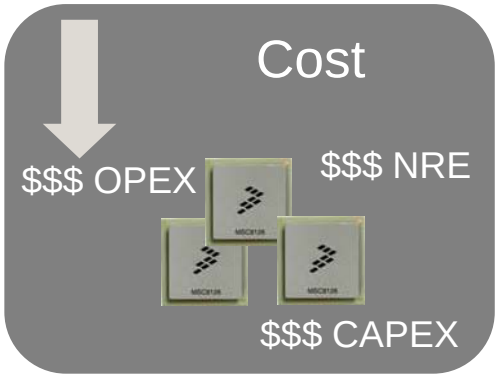












- Wireless infrastructure a significant driver for innovation in
  - Multicore SoCs
  - System level interconnects

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Trends in the Networking and A&D Markets

Networking Trends

- Internet Protocol (IP) everywhere
- VoIP adoption
- Triple-play convergence (voice, video & data)
- Ethernet expansion
- Wireless everything
- Power management and low-power processing
- Security elevation and secure processing nodes
- Standard interconnects
- High-performance in ever smaller form factors

A&D Trends

- **Increased processing performance**
- **Power management and low-power processing**
- **Delivery of voice, data and video**
- **Security and secure systems**
- **Deploying high technology in all phases of defense**
- **Standard interconnects**
- **Emergence of systems integration of off-the-shelf components in place of milspec manufacturing**
- **Industry consolidation**

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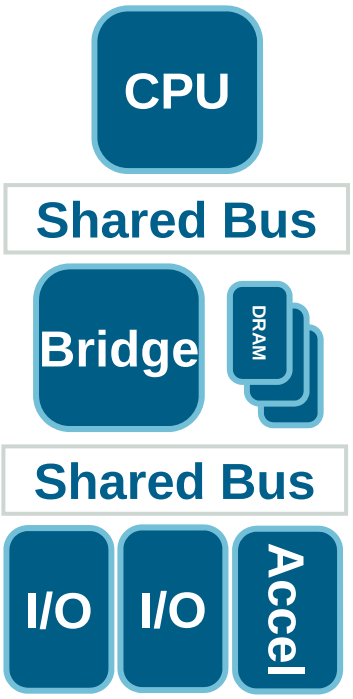
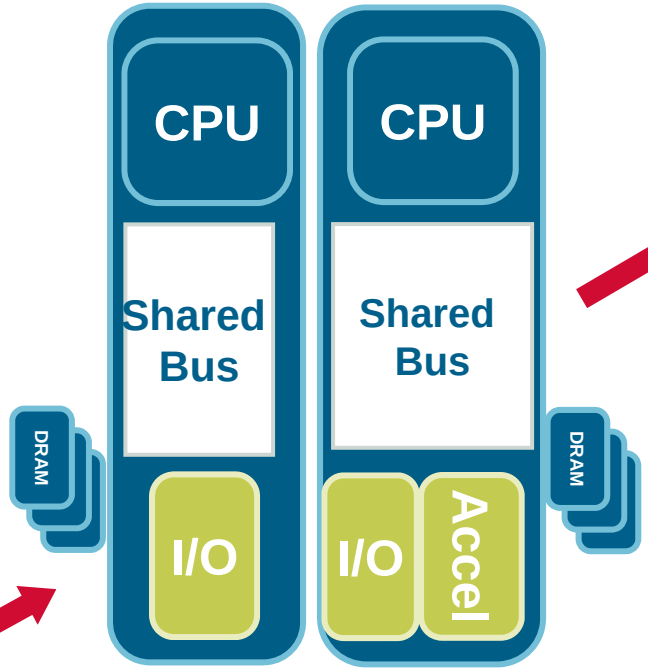
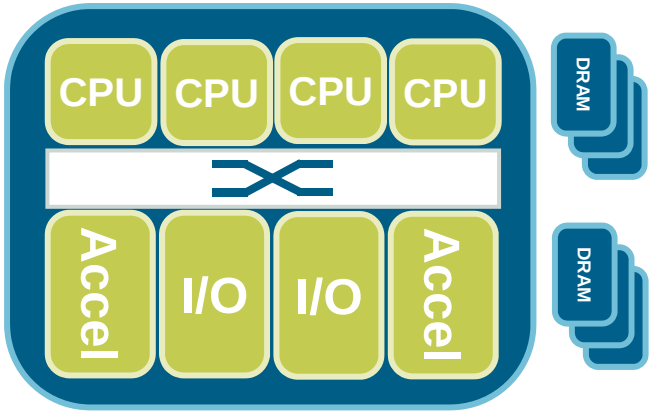
- **Multi-function device**
  - **Limited CPU integration with integrated I/O**







- **Multicore SoC**
  - **Full CPU, accelerator, I/O integration**
  - **Combined control and data plane functions**

- **Single-function devices**
  - **Connected via shared buses**

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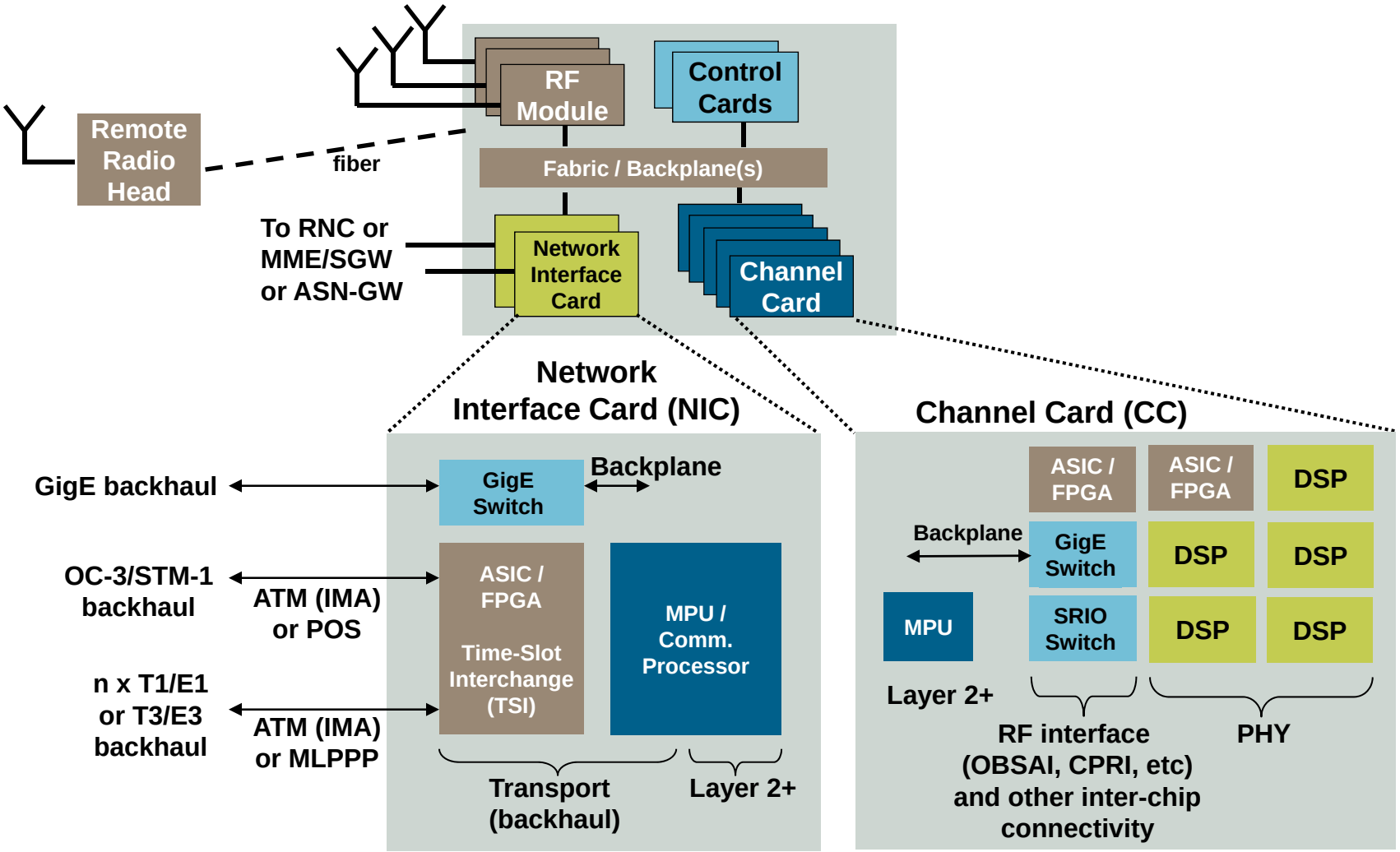
Broadband Wireless Base Station



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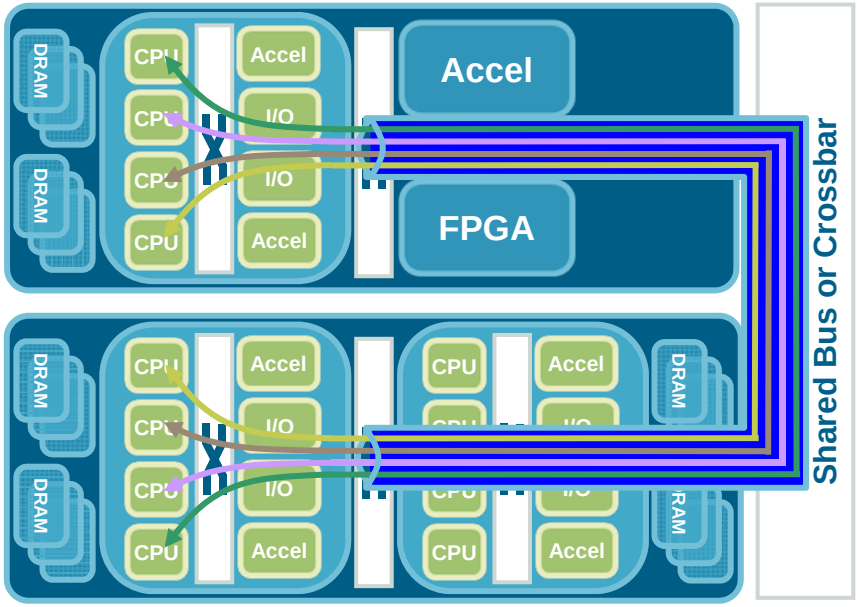
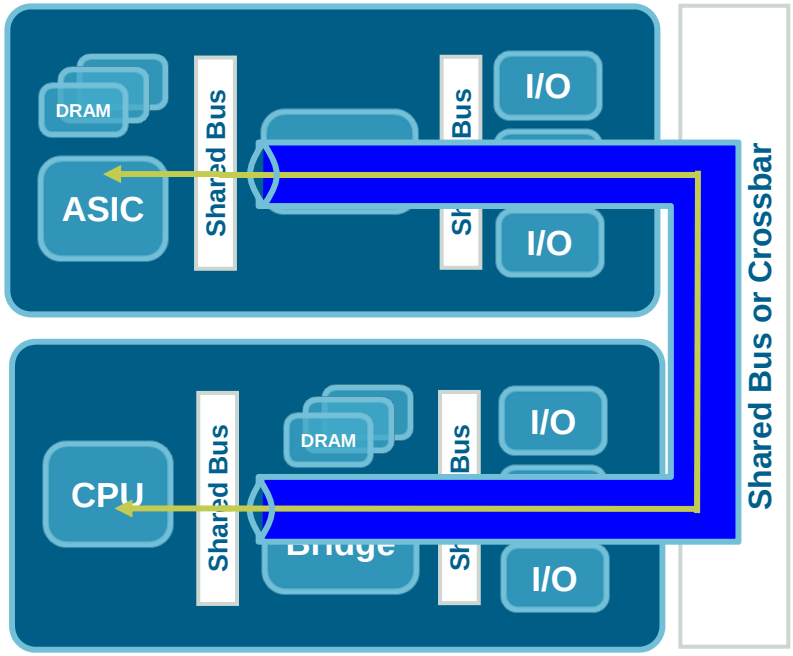
Streams and More Streams

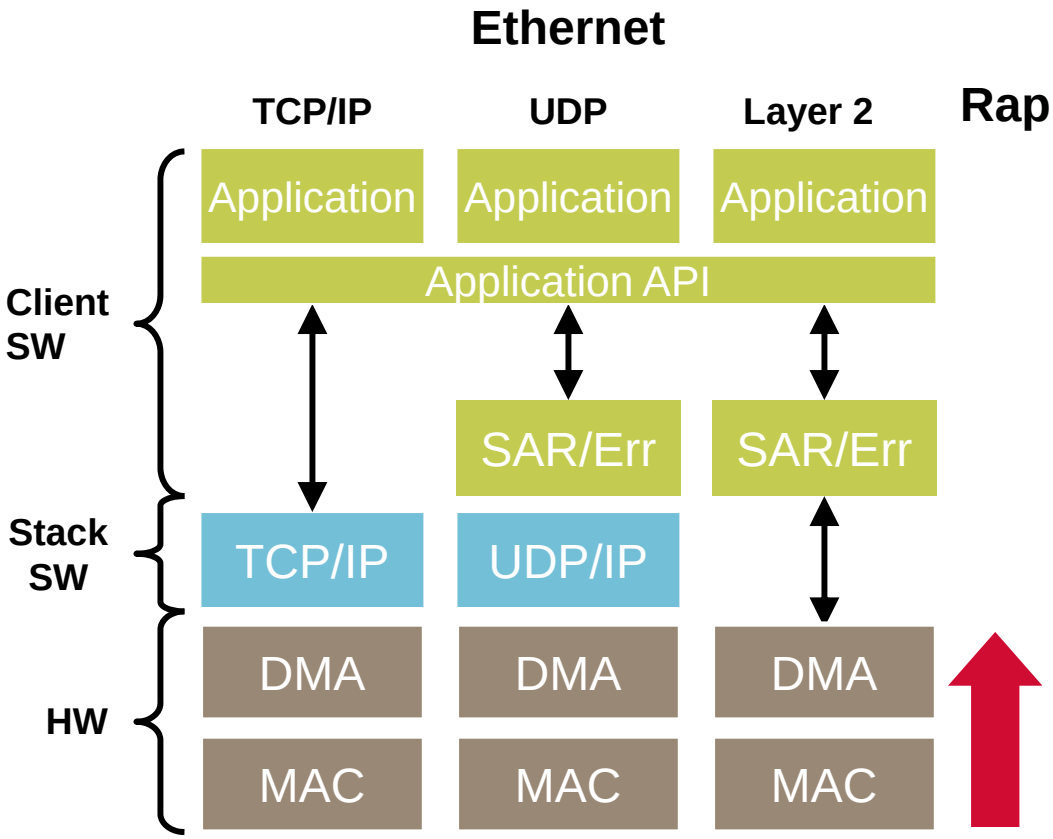
- Multicore SoCs
  - Convergence of control and dataplane
    - Driven by SoC integration trends
  - Many data streams between blocks and silicon devices





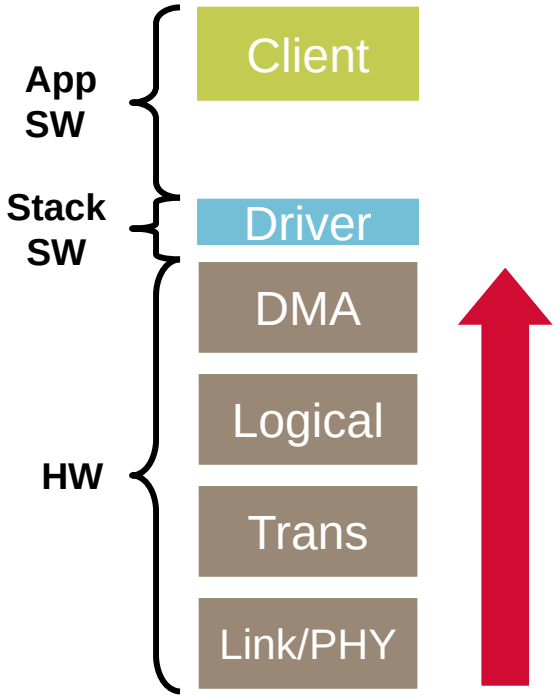
- Discrete and multi-function silicon
  - Single data stream between devices

It's the Logical Layer…



PCI Express® interface: Rd, Wr

RapidIO® interconnect: SWRITE, MSG, Streaming



- Applications driving innovation at logical layer of interconnects
  - Off-load moving upward in the stack
    - Logical layer implemented in hardware
      - Ethernet example of when this isn't the case
    - Power, performance and QoS are drivers

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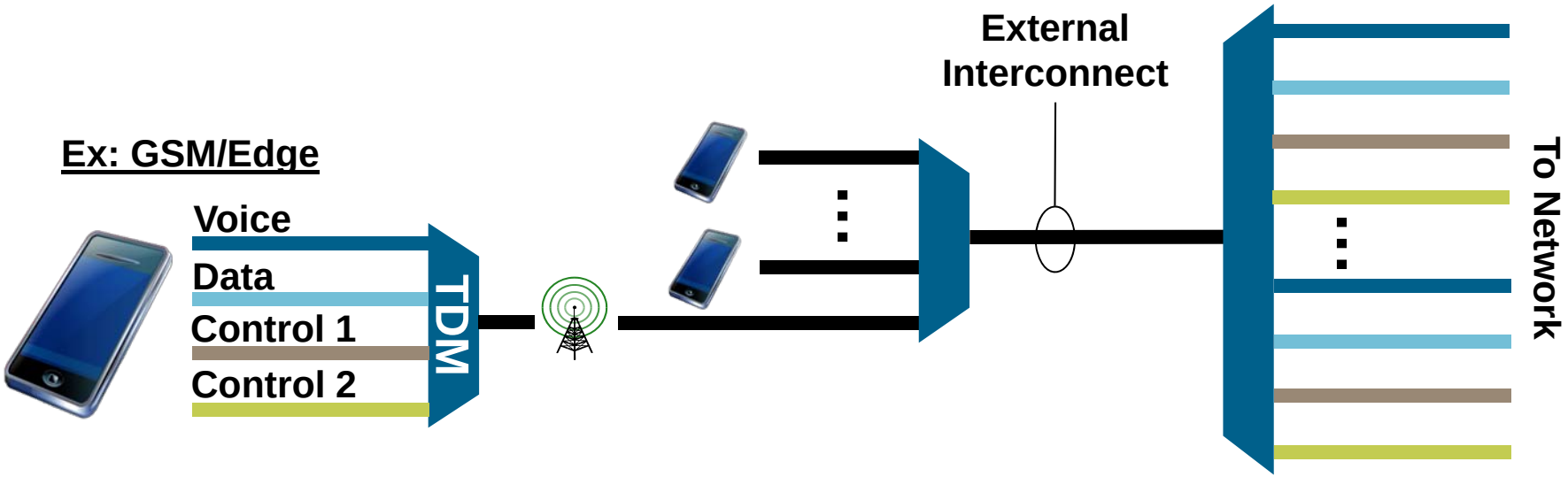
But It's Really About Channelization…

- Interconnects with native support for streams invoke a virtuous cycle
  - Opportunity to lower mux/demuxing in the system
    - Fewer proprietary headers required for stream differentiation
  - Reduces hardware and software overhead
  - Reduces power



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RapidIO and Channelization

- Flows
  - Four prioritized flows defined in specification
    - Three must be supported by all implementations
- Type 11 messaging
  - 4 Mailboxes
    - 4 KByte PDU
  - 64 Mailboxes
    - 256 Byte PDU

- Type 9 data streaming
  - 256 classes of service
  - 64K stream IDs

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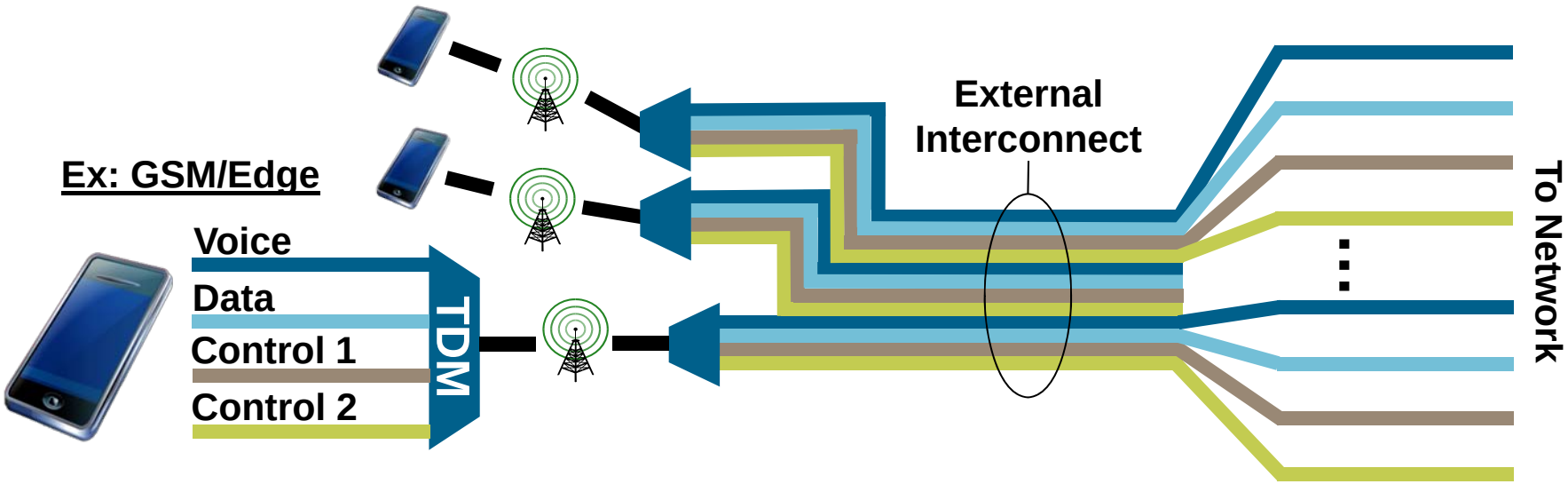
Streaming Support Grows Over Time

- Expect unraveling of stream muxing to occur gradually
  - Software won't change overnight even if hardware is supported
    - Multi-stream hardware support must be there first
      - Requires standards to exist ahead of hardware

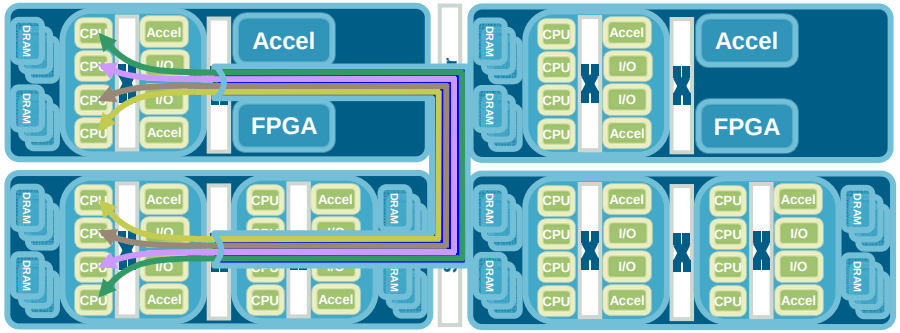


Today's System Requirements

Convergence of control and dataplane devices driven by multicore economics

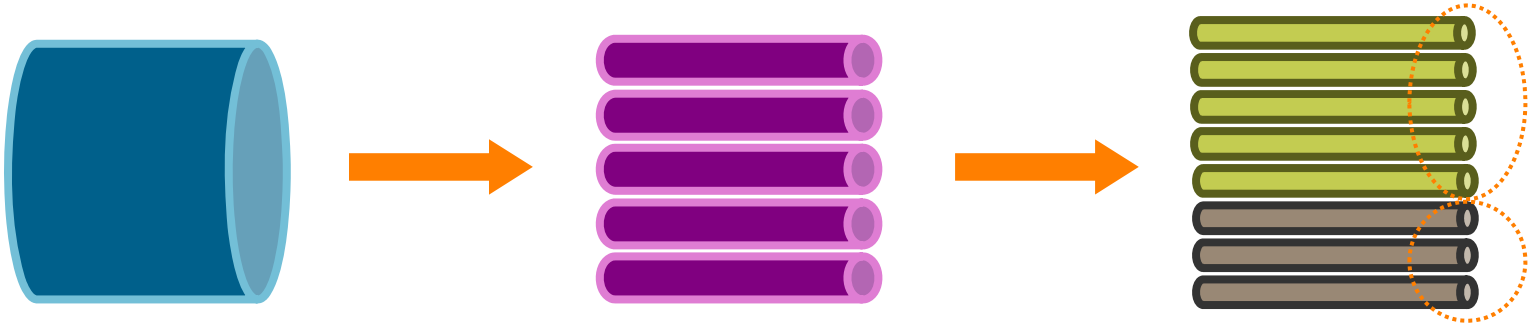
Multiple Baud Rates and Widths

Quality of Service



Stream Differentiation

Robust Flow Control



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RapidIO Value Proposition

- Built-in reliable delivery
  - Lossy delivery defined in Rev 2.0
- Five speeds with variety of widths
  - 1.25G, 2.5G, 3.125G, 5.0G, 6.25G; 1x-16x
- Multiple transaction types with channelization
- Multiple channelized flow control mechanisms
  - Link, source-based, end-to-end
- Multiple use paradigms
  - Memory-mapped R/W
  - Messages (doorbell, data)
  - Datagrams
- Efficient and low CPU-overhead

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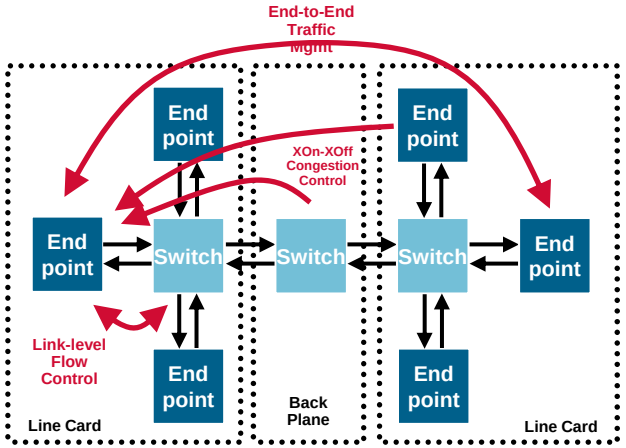
RapidIO Is Unique Evolving Logical Layer Standard

- RapidIO interconnect is leading evolution in logical layer protocols and QoS
  - Eight prioritized flows
  - Robust flow control
    - Link level
    - Congestion to source
    - End-to-end (traffic management)
  - Type 11 messaging transaction type
    - 4 KB max user PDU
    - 16 streams max per flow
  - Type 9 data streaming transaction type
    - 64 KB max user PDU
    - 256 classes-of-service (CoS) per flow
    - 65,536 streams/CoS per flow
    - Standardized traffic management
      - Stream setup/teardown
      - End-to-end flow control
      - Encapsulation



Type 11 Packet

Type 9 Packet

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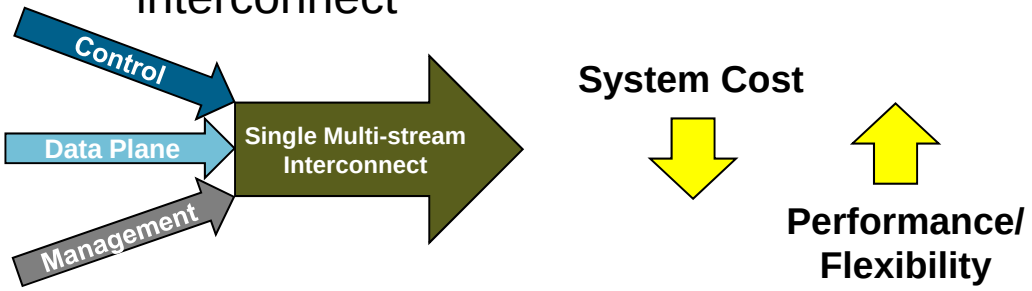
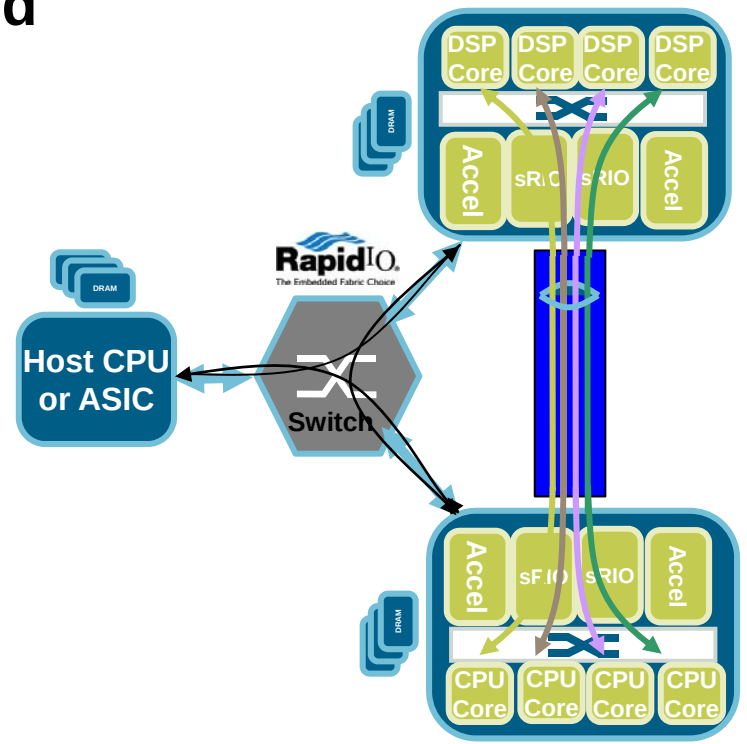
RMan for QorIQ: Taking RapidIO to a New Level

▶Multicore SoCs driving **application and interconnect convergence**

- Combine multiple streams over the same interconnect





▶Industry-first performance & QoS features

- Support for Rev 2.1 of RapidIO standard
  - Dual port @ x2/x1 or single @ x4/x2/x1
  - Up to 5 Gbaud per lane, total of 16 Gbps
- Type 9 - data streaming transaction support
  - Thousands of traffic streams
  - Realistic line-rate performance
- Robust quality-of-service features
  - Stream and priority-aware micro-architecture
  - End-to-end flow control

✓ **Increased performance**
✓ **Robust quality of service**
✓ **Many streams**
✓ **Lower system cost**
✓ **Simpler layout**

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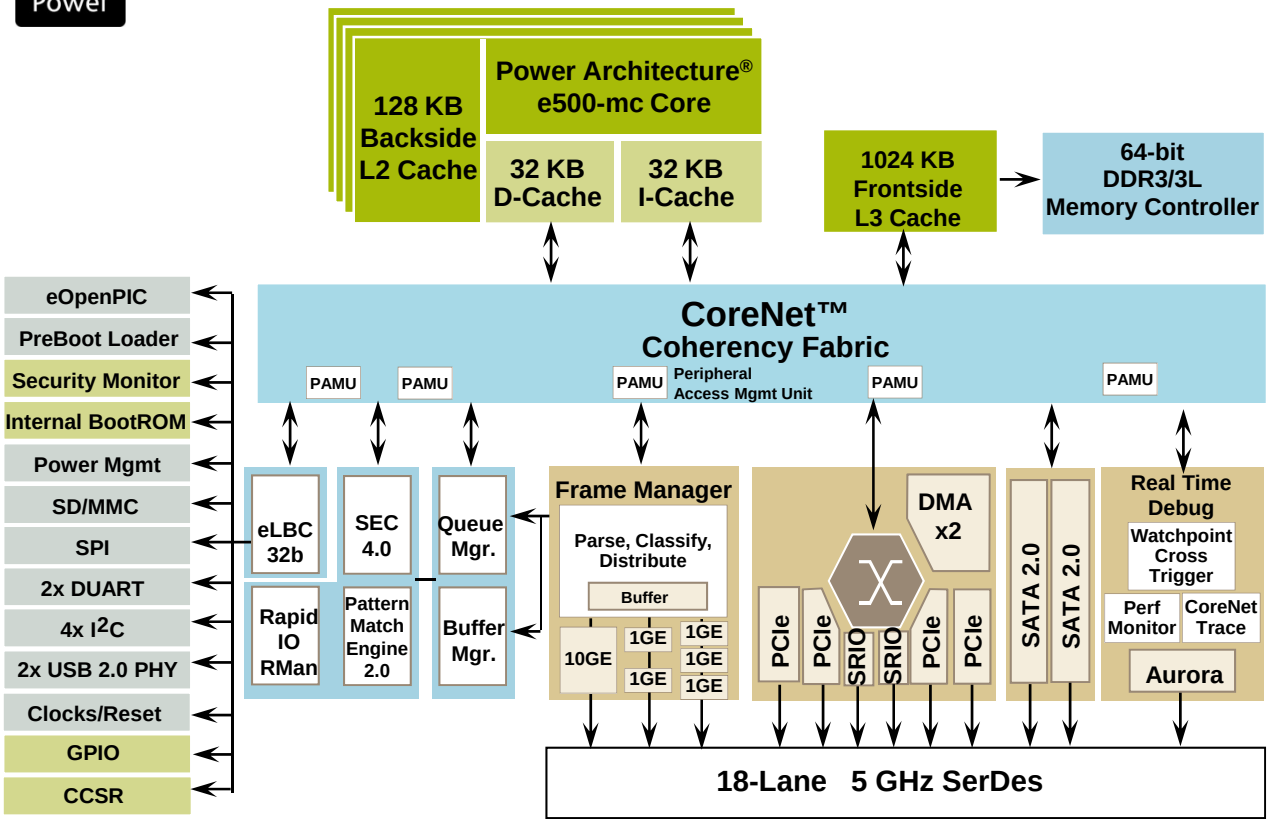
QorIQ P3 Series P3041 Block Diagram



- **Pin-compatible to P4080, P4040, P5020 & P5010**
- **45 nm SOI process**

Quad e500mc Power Architecture®
- 4 cores (up to 1.5GHz) with 128KB backside L2 cache
- 1 MB shared L3 cache w/ECC

Memory controller
- 32/64-bit DDR3/3L w/ECC up to 1.3 GHz

Ethernet
- 5 x 10/100/1000 Ethernet controllers
- 1 x 10 GE controllers

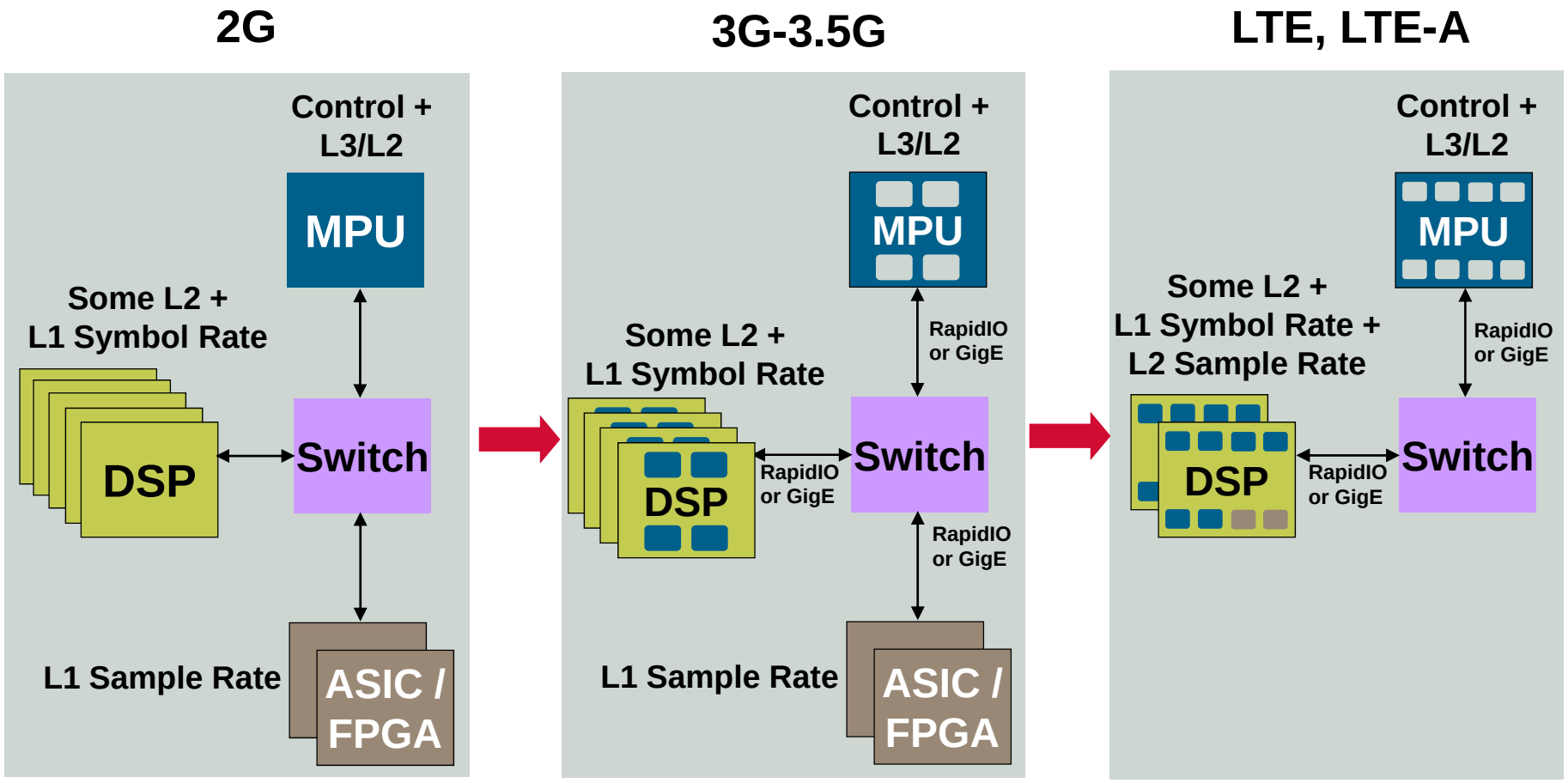
High speed interconnect
- 4 PCIe 2.0 controllers
- 2 SRIO 1.3 + 2.0 controllers
- 2 SATA 2.0
- 2 USB 2.0 w/PHY

CoreNet switch fabric

Trusted architecture

Datapath acceleration architecture
- Security Engine (SEC)
- Pattern Matching Engine (PME)
- Enhanced RapidIO Messaging (Rman)

One Channel Card Architecture Evolution



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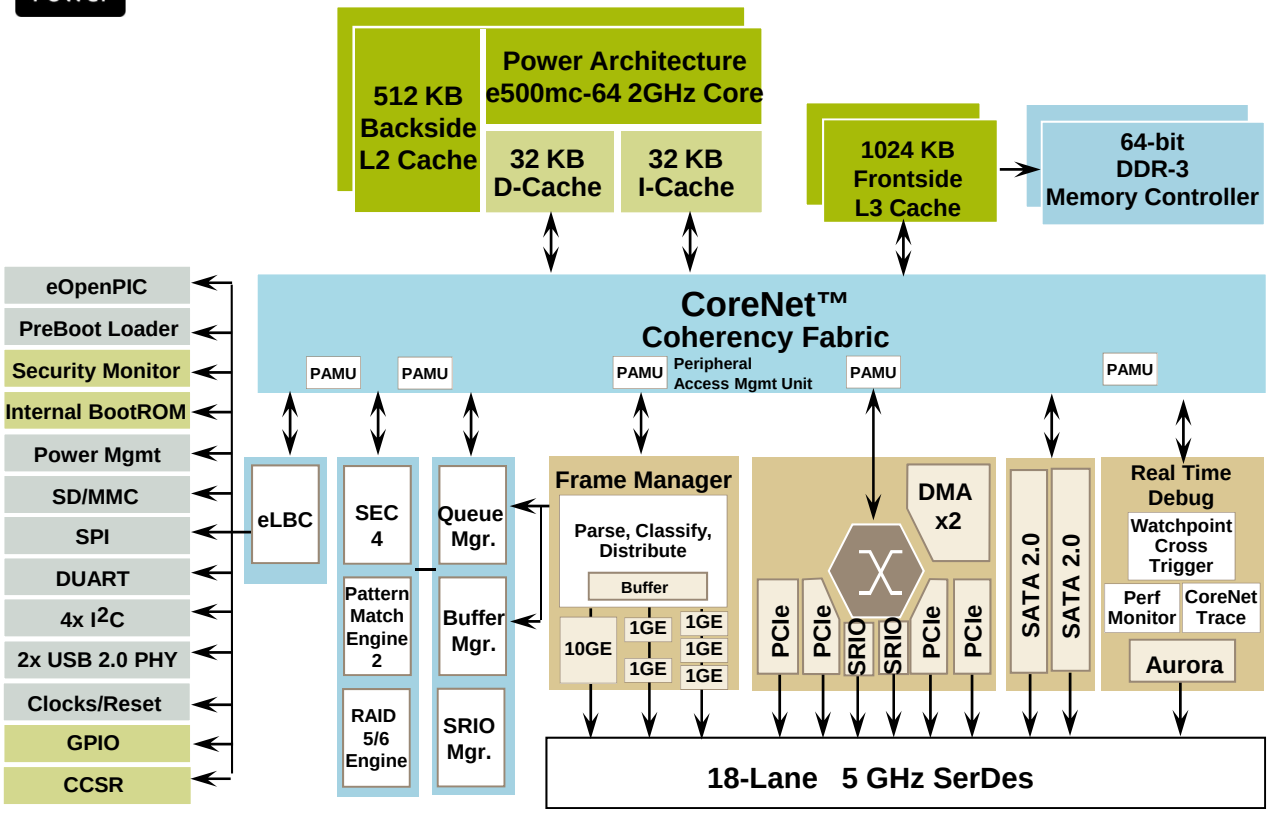
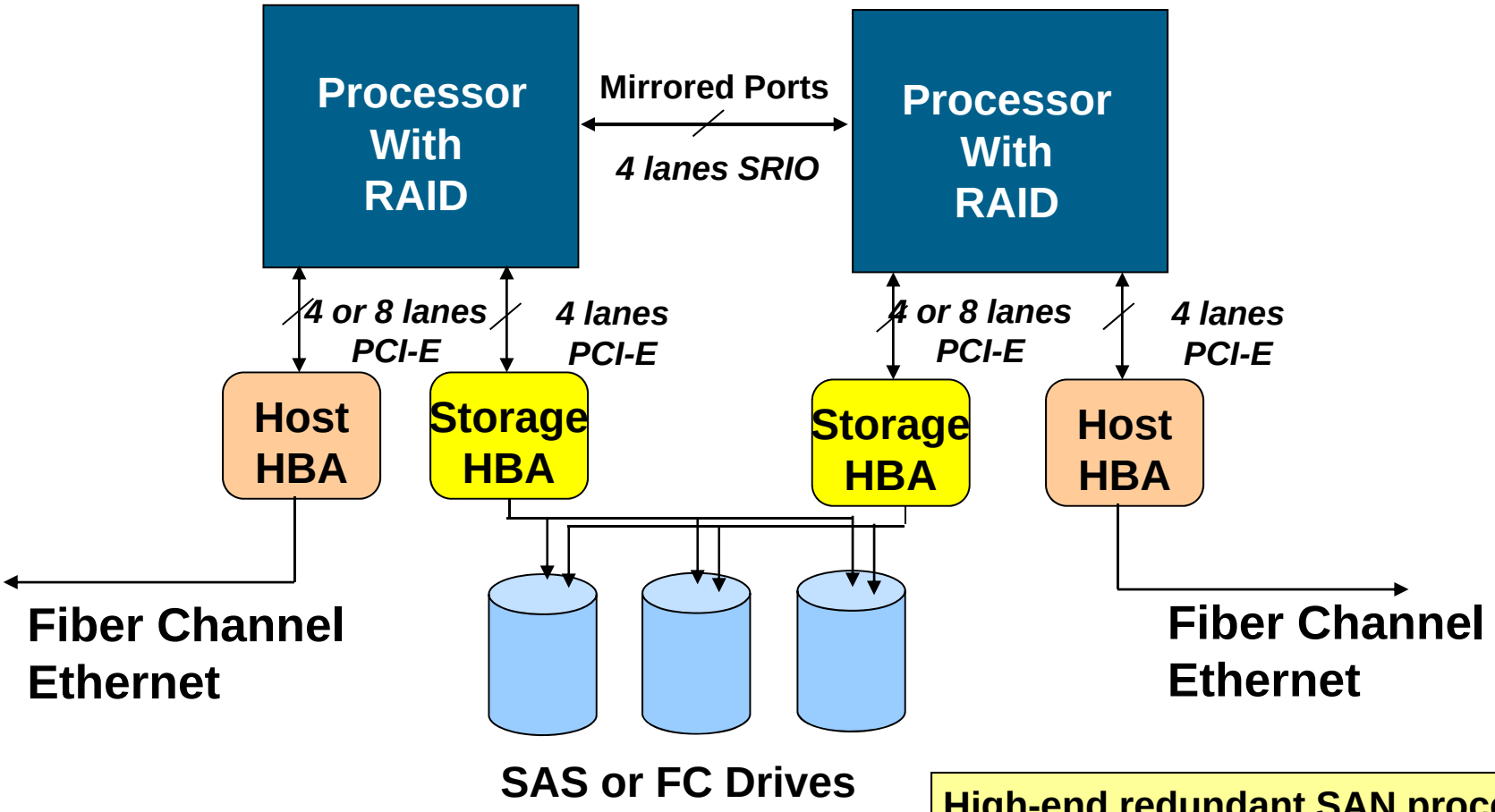
QorIQ P5 Series P5020 Block Diagram



- **Pin-compatible to P4080, P4040 and P3041**
- **45 nm SOI process**

- **2x e500mc-64 core, built on Power Architecture technology**
  - **2x 64-bit cores (up to 2+ GHz) with 512 KB backside L2 cache**
  - **Dual 1 MB shared L3 cache w/ECC**
- **Memory Controller**
  - **Dual 32/64-bit DDR3/3L w/ECC up to 1.3 GHz**
- **Ethernet**
  - **5 x 10/100/1000 Ethernet controllers**
  - **1 x 10 GE controller (XAUI)**
- **High speed interconnect**
  - **4 PCI Express 2.0 controllers**
  - **2 Serial RapidIO 1.3 + 2.0 controllers**
  - **2 SATA 3 Gb/s**
  - **2 USB 2.0 with PHY**
- **CoreNet switch fabric**
- **Trusted architecture**
- **Datapath acceleration architecture**
  - **Security Engine (SEC)**
  - **Pattern Matching Engine (PME)**
  - **RAID 5/6 engine**
  - **Enhanced RapidIO Messaging (Rman)**

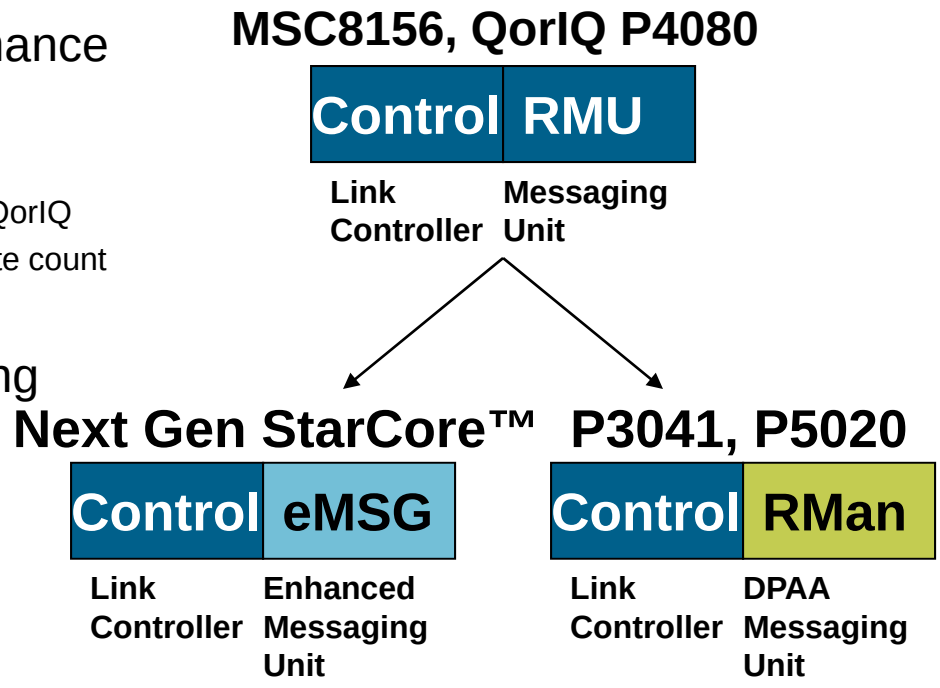
System Diagram
Redundant SAN RAID Processor



High-end redundant SAN processor
1.) RAID processing
2.) Movement of data
3.) Extensibility
4.) Virtualization of drives

Next Generation RapidIO Messaging Unit

- P4080 and all prior devices use existing SRIO messaging unit
  - QorIQ P4080 includes some messaging performance enhancements
- All future devices with SRIO will use new SRIO messaging unit
  - Existing R/W capability retained in existing link controller
  - Implemented as “eMSG” for DSP, “RMan” for QorIQ
  - Improves Type 11 messaging performance
    - Lower CPU overhead
    - Full descriptor-based queuing mechanism
      - Data-Path Architecture (DPAA) enabled for QorIQ
      - Updates descriptor with classification info/byte count
    - More queues
  - Adds support for Type 9 data streaming
    - Line rate with low CPU overhead
    - Enhanced QoS
  - Adds selected Rev 2.0 features
    - Add 5.0 Gbaud operation
    - 2x lane support
    - Extended Type 9 traffic management



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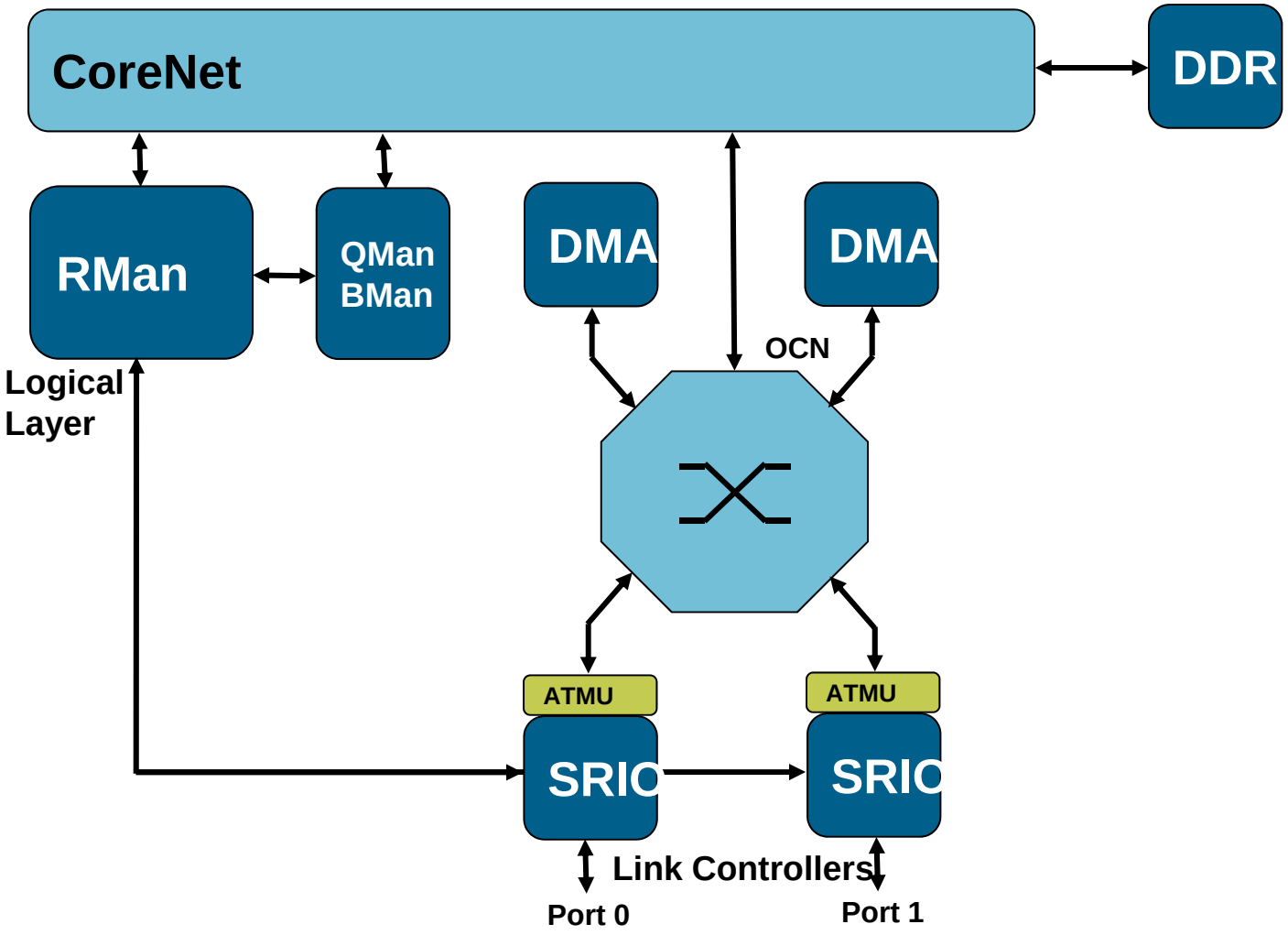
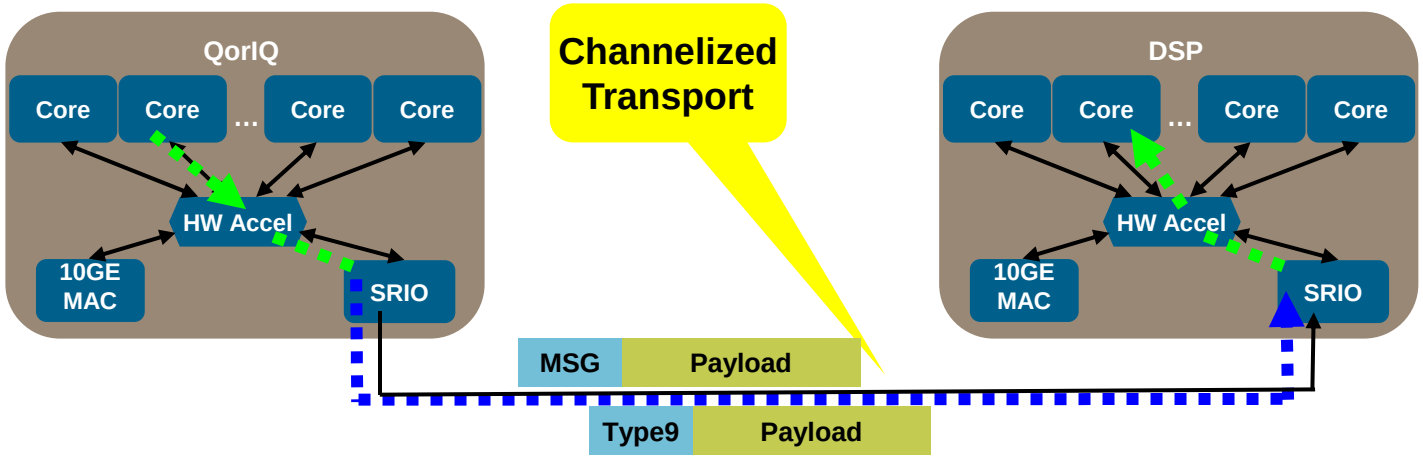
P5020/304x RMan Datapath



RMan: Next Gen RapidIO Interconnect for Freescale Multicore Processors

- Virtualizes RapidIO interconnect data transfers for QorIQ communication platforms
  - Very low CPU overhead
  - Enables zero overhead direct core-to-core communication
- Supports all messaging-style transaction types
  - Type 11 messaging
  - Type 10 doorbells
  - Type 9 data streaming
- Many queues allow multiple inbound/outbound queues per core
  - Hardware queue management via QorIQ Datapath Architecture (DPAA)
- Enhanced QoS
  - End-to-end per stream flow control

Core to Remote Core Transport



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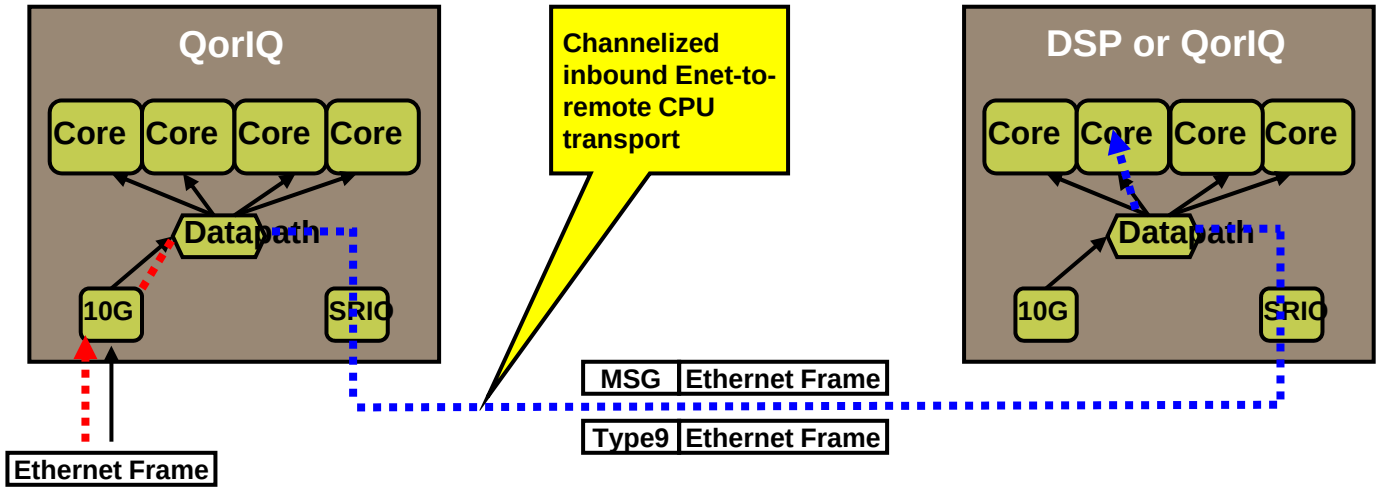
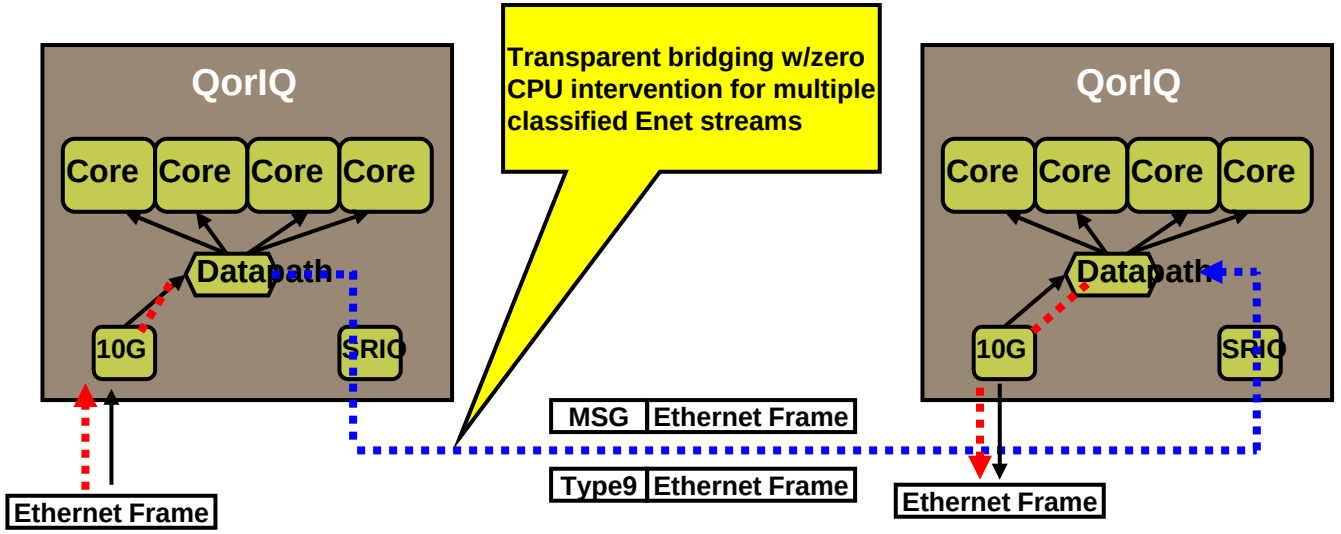
RMan Enables New Zero-CPU Overhead Use Models

Scalable Multicore System



Ethernet Bridging



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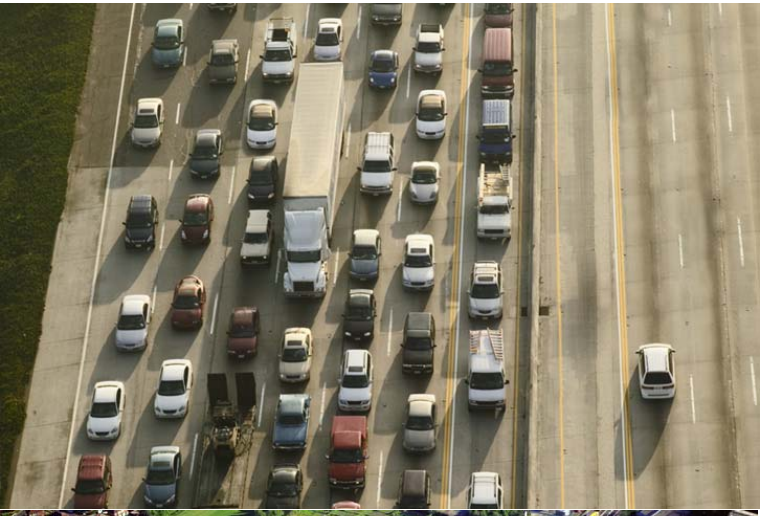
Conclusion



- Wireless infrastructure key example of multicore, multi-stream embedded applications
- Wireless is driving innovation in logical layer of high-speed interconnects
- Many other markets need high-speed QoS-enabled interconnects, including storage and A&D
- Hardware offload at higher layers of a channelized interconnect protocol helps meet future QoS, performance and power goals

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