

Intel[®] Serial Flash Memory (S33)

16-, 32-, and 64-Mbit

Datasheet

Product Features

- Architecture
 - SPI compatible serial interface
 - Eight 8-Kbyte parameter blocks; configurable as one 64-Kbyte main memory sector
 - 64-Kbyte main memory sectors
 - 16 Mbit (31 sectors)
 - 32 Mbit (63 sectors)
 - 64 Mbit (127 sectors)
- Voltage and Power
 - V_{cc} = 2.7 V to 3.6 V
 - Standby current: 15 μ A (Typ)
 - Read current: 3 mA (Typ) at 33.3 MHz; 6 mA (Typ) at 68 MHz
- Performance
 - 68-MHz fast read; 33.3 MHz standard read
 - 256-byte program buffer
- Software
 - Driver and file manager
- Security
 - One-Time Programmable Space
 - 64 unique factory device identifier bits
 - 64 user-programmable OTP bits
 - Additional 3920 user-programmable OTP bits
- Quality and Reliability
 - Operating temperature: -40 °C to +85 °C
 - 100K minimum erase cycles per sector (block)
 - 0.13 μ m ETOX[™] VIII process
- Density and Packaging
 - 16-/32-/64-Mbit densities in SOIC-16 package
 - 16-Mbit density in SOIC-8 package
- Industry standard packaging and pin-out



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Revision History

Date	Revision	Description
August 2006	001	Initial release

1.0 Introduction

This document describes the Intel® Serial Flash Memory (S33) device features, operation, and specifications.

The Intel® Serial Flash Memory (S33) device provides superior performance with enhanced security features and takes advantage of the high quality and reliability of the NOR-based Intel® 0.13 μm ETOX™ VIII process technology. Offered in 16-Mbit, 32-Mbit, and 64-Mbit densities, the Intel® Serial Flash Memory (S33) device maintains hardware and software compatibility with existing industry offerings to ensure ease of design.

The Intel® Serial Flash Memory (S33) takes advantage of the more than one billion flash unit manufacturing experience since and is ideal for code and data applications where simplified interface and low cost are required, such as in PC and notebooks, WLAN and DSL cards and routers, printers, TVs, DVD/CD players and recorders, and other consumer electronics devices.

1.1 Nomenclature

Block:	A group of flash cells that share common erase circuitry and erase simultaneously. For Serial Flash devices Blocks are also more commonly referred to as Sectors.
Clear:	Indicates a logic zero (0)
Page:	A 256-byte main memory segment that is aligned to 256-byte boundary
Parameter Block:	A 8-Kbyte memory segment that can be erased independently
Program:	To write data to the flash array
Sector:	A single 64-KByte main block or all eight 8-KByte parameter blocks
Set:	Indicates a logic one (1)

1.2 Acronyms

OTP:	One Time Programmable
PR:	Protection Register
PRD:	Protection Register Data
RFU:	Reserved for Future Use
SR:	Status Register
WSM:	Write State Machine

1.3 Conventions

0x:	Hexadecimal prefix
0b:	Binary prefix
k:	1,000
M:	1,000,000
Nibble:	4 bits
Byte:	8 bits
Word:	16 bits
Kword:	1,024 words
Kb:	1,024 bits
KB:	1,024 bytes
Mb:	1,048,576 bits
MB:	1,048,576 bytes
Brackets:	Square brackets ([]) will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4,1] and D[15:0]).
00FFh:	Denotes 16-bit hexadecimal numbers
00FF 00FFh:	Denotes 32-bit hexadecimal numbers

2.0 Functional Overview

This section provides an overview of the features and capabilities of the Intel® Serial Flash Memory (S33) device.

The Intel® Serial Flash Memory (S33) device is available in 16-, 32-, and 64-Mbit densities with a common SPI interface. The SPI interface consists of 8 pins. Six of these pins are signals; the other two are Vcc and ground.

The Intel® Serial Flash Memory (S33) device contains eight 8-Kbyte parameter blocks and up to 127 64-Kbyte main memory sectors. The eight 8-Kbyte parameter blocks can be treated as one 64-Kbyte main memory sector.

The Intel® Serial Flash Memory (S33) device includes new security features. Two 8-byte, thirty 16-byte, and one 10-byte individually lockable OTP protection registers can support multiple uses, including unique flash device identification.

A sector erase operation erases one of the device’s 64-Kbyte main memory sectors or all 8 8-Kbyte parameter blocks, independent of other memory sectors. A parameter block erase operation erases the targeted parameter block; it is ignored when the address is outside the parameter block space. Each block or memory sector can be independently erased 100,000 times. A bulk erase operation erases the entire chip.

Each device incorporates a Write Buffer of up to 256 bytes (128 words) to allow optimum programming performance. Page program operation uses the Write Buffer to program up to 256-bytes within a 256-byte-aligned main memory region. A given page can be programmed multiple times between erase cycles.

2.1 Memory Maps

Table 1. Intel® Serial Flash Memory (S33) Bottom Boot Memory Map (Sheet 1 of 2)

Size (KB)	Sector	Memory Addressing (Hex)	Memory Addressing (Hex)	Memory Addressing (Hex)
		64-Mbit	32-Mbit	16-Mbit
64	127	7F0000 - 7FFFFFFF		
64	126	7E0000 - 7EFFFF		
...		
64	64	400000 - 40FFFF		
64	63	3F0000 - 3FFFFFFF	3F0000 - 3FFFFFFF	
64	62	3E0000 - 3EFFFF	3E0000 - 3EFFFF	
...	
64	32	200000 - 20FFFF	200000 - 20FFFF	
64	31	1F0000- 1FFFFFFF	1F0000- 1FFFFFFF	1F0000- 1FFFFFFF
64	30	1E0000 - 1EFFFF	1E0000 - 1EFFFF	1E0000 - 1EFFFF
...
64	16	100000 - 10FFFF	100000 - 10FFFF	100000 - 10FFFF
64	15	F0000 - FFFFFF	F0000 - FFFFFF	F0000 - FFFFFF
64	14	E0000 - EFFFFF	E0000 - EFFFFF	E0000 - EFFFFF
...

Table 1. Intel® Serial Flash Memory (S33) Bottom Boot Memory Map (Sheet 2 of 2)

64	4	40000 - 4FFFF	40000 - 4FFFF	40000 - 4FFFF
64	3	30000 - 3FFFF	30000 - 3FFFF	30000 - 3FFFF
64	2	20000 - 2FFFF	20000 - 2FFFF	20000 - 2FFFF
64	1	10000 - 1FFFF	10000 - 1FFFF	10000 - 1FFFF
8	0-H	E000 - FFFF	E000 - FFFF	E000 - FFFF
8	0-G	C000 - DFFF	C000 - DFFF	C000 - DFFF
8	0-F	A000 - BFFF	A000 - BFFF	A000 - BFFF
8	0-E	8000 - 9FFF	8000 - 9FFF	8000 - 9FFF
8	0-D	6000 - 7FFF	6000 - 7FFF	6000 - 7FFF
8	0-C	4000 - 5FFF	4000 - 5FFF	4000 - 5FFF
8	0-B	2000 - 3FFF	2000 - 3FFF	2000 - 3FFF
8	0-A	0 - 1FFF	0 - 1FFF	0 - 1FFF

Table 2. Intel® Serial Flash Memory (S33) Top Boot Memory Map (Sheet 1 of 2)

Size (KB)	Sector	Memory Addressing (Hex)	Size (KB)	Sector	Memory Addressing (Hex)	Size (KB)	Sector	Memory Addressing (Hex)
		64-Mbit			32-Mbit			16-Mbit
8	127-H	7FE000 - 7FFFFFFF	8	63-H	3FE000 - 3FFFFFFF	8	31-H	1FE000 - 1FFFFFFF
8	127-G	7FC000 - 7FDFFF	8	63-G	3FC000 - 3FDFFF	8	31-G	1FC000 - 1FDFFF
8	127-F	7FA000 - 7FBFFF	8	63-F	3FA000 - 3FBFFF	8	31-F	1FA000 - 1FBFFF
8	127-E	7F8000 - 7F9FFF	8	63-E	3F8000 - 3F9FFF	8	31-E	1F8000 - 1F9FFF
8	127-D	7F6000 - 7F7FFF	8	63-D	3F6000 - 3F7FFF	8	31-D	1F6000 - 1F7FFF
8	127-C	7F4000 - 7F5FFF	8	63-C	3F4000 - 3F5FFF	8	31-C	1F4000 - 1F5FFF
8	127-B	7F2000 - 7F3FFF	8	63-B	3F2000 - 3F3FFF	8	31-B	1F2000 - 1F3FFF
8	127-A	7F0000 - 7F1FFF	8	63-A	3F0000 - 3F1FFF	8	31-A	1F0000 - 1F1FFF
64	126	7E0000 - 7EFFFF	64	62	3F0000 - 3FFFFFFF	64	30	1F0000 - 1FFFFFFF
64	125	7D0000 - 7DFFFF	64	61	3D0000 - 3DFFFF	64	29	1D0000 - 1DFFFF
...
64	97	610000 - 61FFFF	64	33	210000 - 21FFFF	64	1	10000 - 1FFFF
64	96	600000 - 60FFFF	64	32	200000 - 20FFFF	64	0	0 - FFFF
64	95	5F0000 - 5FFFFF	64	31	1F0000 - 1FFFFF			
64	94	5E0000 - 5EFFFF	64	30	1E0000 - 1EFFFF			
...			

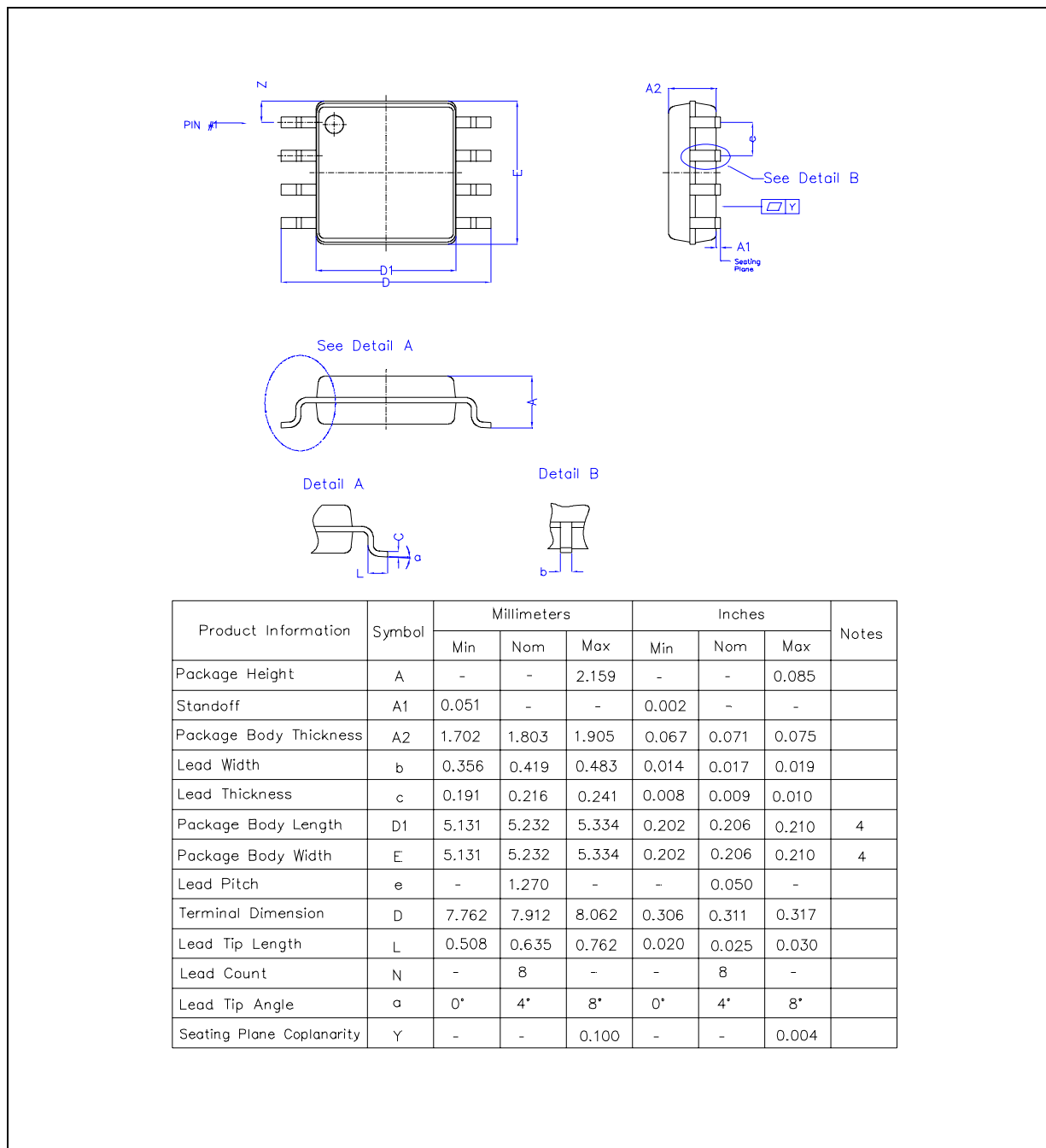
Table 2. Intel® Serial Flash Memory (S33) Top Boot Memory Map (Sheet 2 of 2)

64	65	410000 - 41FFFF	64	1	10000 - 1FFFF
64	64	400000 - 40FFFF	64	0	0 - FFFF
64	63	3F0000 - 3FFFFFF			
64	62	3E0000 - 3EFFFF			
...			
64	1	10000 - 1FFFF			
64	0	0 - FFFF			

3.0 Package Information

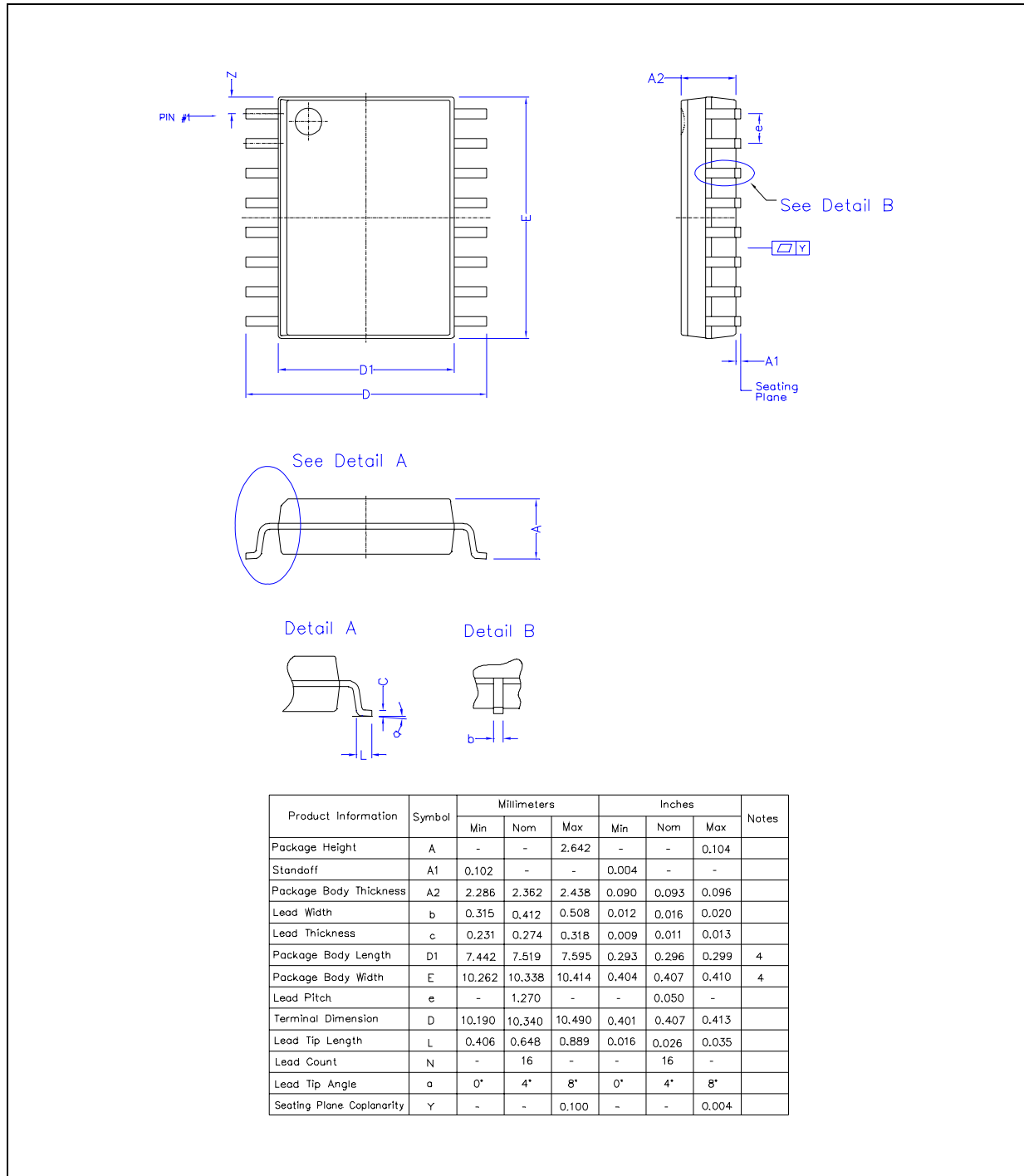
3.1 SOIC-8 Package

Figure 1. SOIC-8 Package Drawing and Specifications



3.2 SOIC-16 Package

Figure 2. SOIC-16 Package Drawing and Specifications

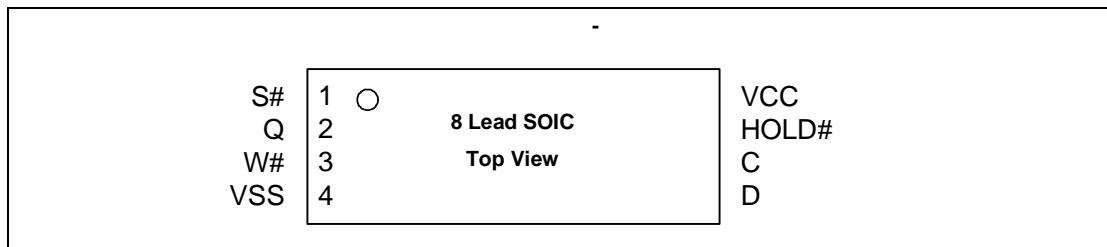


4.0 Pinouts and Signal Descriptions

The Intel® Serial Flash Memory (S33) device is available in two package types. The 16-Mbit density is supported on both SOIC-8 and SOIC-16 packages as shown in Figure 3, "SOIC-8 Pinout (16-Mbit)" and Figure 4, "SOIC-16 Package Pinout (16-/32-/64-Mbit)". The 16, 32-, and 64-Mbit densities are supported on the SOIC-16 package as shown in Figure 4, "SOIC-16 Package Pinout (16-/32-/64-Mbit)".

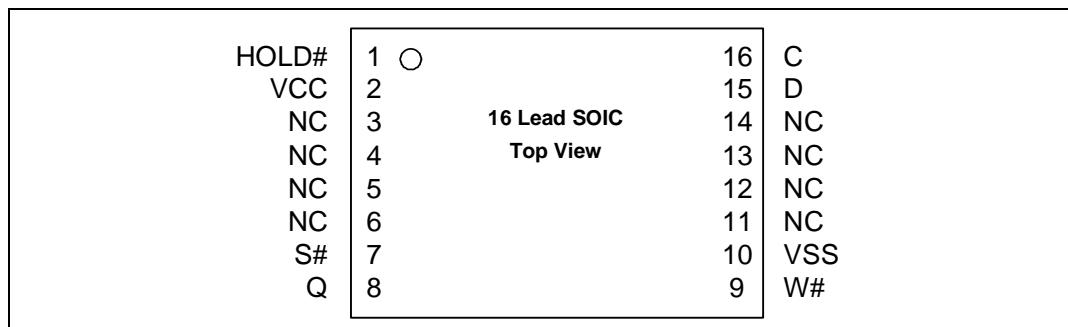
4.1 SOIC-8 Pinout (16-Mbit)

Figure 3. SOIC-8 Pinout (16-Mbit)



4.2 SOIC-16 Package Pinout (16-/32-/64-Mbit)

Figure 4. SOIC-16 Package Pinout (16-/32-/64-Mbit)



4.3 Signal Descriptions

Table 3. Signal Descriptions for the Intel® Serial Flash Memory (S33)

Symbol	Type	Name and Function
C	Input	SPI Clock: Provides the timing of the SPI interface. OP codes, addresses, and data are latched in on the rising edge. SPI output data transitions after the falling edge.
D	Input	SPI Data Input: Shifts all data (including OP codes, Address Bytes, as well as Data Bytes) into the device. All data is clocked in on the rising edge of "C", starting with the MSB. The rising edge input applies to Modes 0 & 3 as depicted in Figure 12, "Supported SPI Bus Operation Modes" on page 26 .
Q	Output	SPI Data Output: Shifts all data out of the device. All output data is clocked out after the falling edge of "C", starting with the MSB. The falling edge output applies to Modes 0 & 3 as depicted in Figure 12 on page 26 .
S#	Input	SPI Select: Falling S# edge triggers command writes to the SPI interface. Rising S# edge completes (or terminates) the SPI command cycle. When S# is high, "Q" is at high-Z.
HOLD#	Input	SPI HOLD: Internally freezes the Synchronization Clock and sets "Q" to high-Z. To enter the Hold condition, S# must be low. Refer to Section 8.1.2, "The Hold State" on page 26 for details.
W#	Input	Write Protect: Enables write protection. Refer to Table 20 on page 35 for details.
VCC	Power	Power Supply: Source voltage. Writes to the flash array are inhibited when $V_{CC} \leq V_{LKO}$. Operations at invalid V_{CC} should not be attempted.
VSS	Power	Ground: Connect to system ground. Do not float any VSS connection.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

Note: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Temperature under Bias Expanded ($T_{A, \text{Ambient}}$)	-40	+85	°C	4
Storage Temperature	-65	+125	°C	—
V_{CC} Voltage	-2.0	+5.6	V	1
I_{SH} Output Short Circuit Current	—	100	mA	3

Notes:

1. Voltage is referenced to V_{SS} . During infrequent non-periodic transitions, the voltage potential between V_{SS} and input/output pins may undershoot to -2.0 V for periods < 20 ns or overshoot to $V_{CCQ}(\text{max}) + 2.0$ V for periods < 20 ns.
2. During infrequent non-periodic transitions, the voltage potential between V_{CC} and the supplies may undershoot to -2.0 V for periods < 20 ns or $V_{SUPPLY}(\text{max}) + 2.0$ V for periods < 20 ns.
3. Output is shorted for no more than one second. No more than one output shorted at a time
4. Temperature specified is at ambient (T_{ambient}) and not the package (T_{case}).

5.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 6. Temperature and VCC Operating Condition of Intel® Serial Flash Memory (S33)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
T_C	Operating Temperature (case)	-40	+25	+85	°C	1
V_{CC}	V_{CC} Supply Voltage	2.7	3.0	3.6	V	

Note:

1. Temperature specified is at case(T_{case}) ambient(T_{ambient}).

5.3 Power Supply

This section provides an overview of system level considerations with regards to the flash device. It includes a brief description of power-up, power-down and decoupling design considerations.

5.3.1 Power-Up/Down Characteristics

The device is protected against accidental block erasure or programming during power transitions. After power-up, a T_{VSL} latency is required before S# can be brought low to issue a command.

5.3.2 Power Supply Decoupling

Flash memory devices require careful power supply de-coupling. Three basic power supply current considerations are 1) standby current levels, 2) active current levels, and 3) transient peaks produced when CE# and OE# are asserted and deasserted.

When the device is accessed, many internal conditions change. Circuits within the device enable charge-pumps, and internal logic states change at high speed. All of these internal activities produce transient signals. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and correct de-coupling capacitor selection suppress transient voltage peaks.

Because Intel® Multi-Level Cell (MLC) flash memory devices draw their power from VCC, VPP, and VCCQ, each power connection should have a 0.1 μ F ceramic capacitor to ground. High-frequency, inherently low-inductance capacitors should be placed as close as possible to package leads.

Additionally, for every eight devices used in the system, a 4.7 μ F electrolytic capacitor should be placed between power and ground close to the devices. The bulk capacitor is meant to overcome voltage droop caused by PCB trace inductance.

6.0 Electrical Characteristics

6.1 DC Current Specifications

Table 7. DC Current Characteristics

Symbol	Parameter	Typ	Max	Unit	Test Conditions	Notes
I_{LI}	Input Load Current		±2	μA	$V_{CC} = V_{CC\ Max}$; $V_{IN} = V_{CC}$ or V_{SS}	3
I_{LO}	Output Leakage Current		±2	μA	$V_{CC} = V_{CC\ Max}$; $V_{IN} = V_{CC}$ or V_{SS}	
I_{CCS}	V_{CC} Standby Current	15	70	μA	$S\# = V_{CC}$; $V_{IN} = V_{CC}$ or V_{SS}	4,6
I_{DPD}	V_{CC} Deep Power-Down Current	15	70	μA	$S\# = V_{CC}$; $V_{IN} = V_{CC}$ or V_{SS}	4
I_{CCR}	V_{CC} Read Current	2	4	mA	20 MHz; No Load	7
		3	5		33.3 MHz; No Load	
		5	8		50 MHz; No Load	
		6	10		68 MHz; No Load	
I_{CCP}	Page Program Current	18	55	mA	$S\# = V_{CC}$; 256-Byte Page	2,5
I_{CCE}	Parameter Block Erase Current	16	45	mA	$S\# = V_{CC}$	2,5
	Sector Erase Current	16	45	mA	$S\# = V_{CC}$	2,5
I_{CCB}	Bulk Erase Current	16	45	mA	$S\# = V_{CC}$	2,5

Notes:

- All currents are RMS unless noted. Typical values at typical V_{CC} , $T_C = +25^\circ\text{C}$.
- Sampled, not 100% tested.
- If $V_{IN} > V_{CC}$ the input load current increases to 10 μA max.
- I_{CCS} and I_{DPD} is the average current measured over any 5ms time interval 5μs after a $S\#$ deassertion.
- I_{CCP} , I_{CCE} measured over typical or max times.
- I_{CCS} will increase substantially if $W\#$ or $HOLD\#$ is toggled while in standby mode.
- I_{CCR} will increase if D is toggled during read.

6.2 DC Voltage Specifications

Table 8. DC Voltage Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions	Notes
V_{IL}	Input Low Voltage	0	$0.3 * V_{CC}$	V		1
V_{IH}	Input High Voltage	$0.7 * V_{CC}$	V_{CC}	V		1
V_{OL}	Output Low Voltage		0.1	V	$V_{CC} = V_{CC\ Min}$ $I_{OL} = 100\ \mu\text{A}$	
V_{OH}	Output High Voltage	$V_{CC} - 0.1$		V	$V_{CC} = V_{CC\ Min}$ $I_{OH} = -100\ \mu\text{A}$	
V_{LKO}	V_{CC} Lockout Voltage	2.0		V		

Note:

- V_{IL} can undershoot to -1.0 V for periods <2 ns and V_{IH} may overshoot to Maximum $V_{CC} + 1.0$ V for periods <2 ns.

6.3 Capacitance

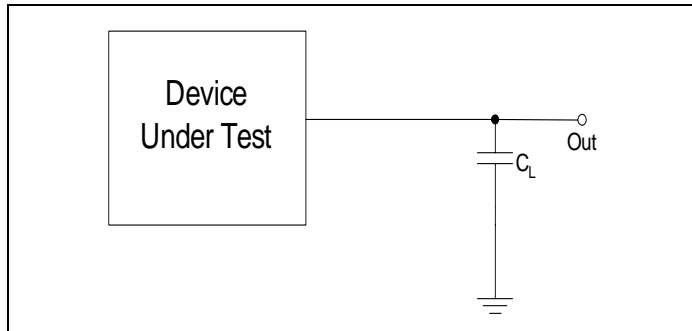
Table 9. Intel® Serial Flash Memory (S33) Device Capacitance

Symbol	Parameter ¹	Type	Max	Unit	Condition ²
C _{IN}	Input Capacitance	6	8	pF	V _{IN} = 0.0 V V _{CC} = 0 V V _{CC} = V _{CCmax}
C _{OUT}	Output Capacitance	8	12	pF	V _{OUT} = 0.0 V V _{CC} = 0 V V _{CC} = V _{CCmax}
Notes: 1. Sampled, not 100% tested. 2. T _A = +25 °C, f = 1 MHz.					

7.0 AC Characteristics

7.1 AC Test Conditions

Figure 5. Transient Equivalent Testing Load Circuit



Note: C_L Includes Jig Capacitance

Table 10. AC Measurement Conditions

Parameter	Min	Max	Unit
Load Capacitance (C_L)		30 ¹	pF
Input Rise and Fall Times	0.3	3	ns
Input VIL Timing Reference Voltages		0.3*Vcc	V
Input VIH Timing Reference Voltages	0.7*Vcc		V
Input Drive Voltages	0 for VIL, Vcc for VIH		V
Input Timing Reference Voltages	0.3Vcc to 0.7Vcc		V
Output Timing Reference Voltages	Vcc/2		V
Note:			
1. Output Hi-Z is defined as the point where data output is no longer driven.			

7.2 AC Timing Characteristics

7.2.1 Serial Input Characteristics

Table 11. Serial Input Characteristics

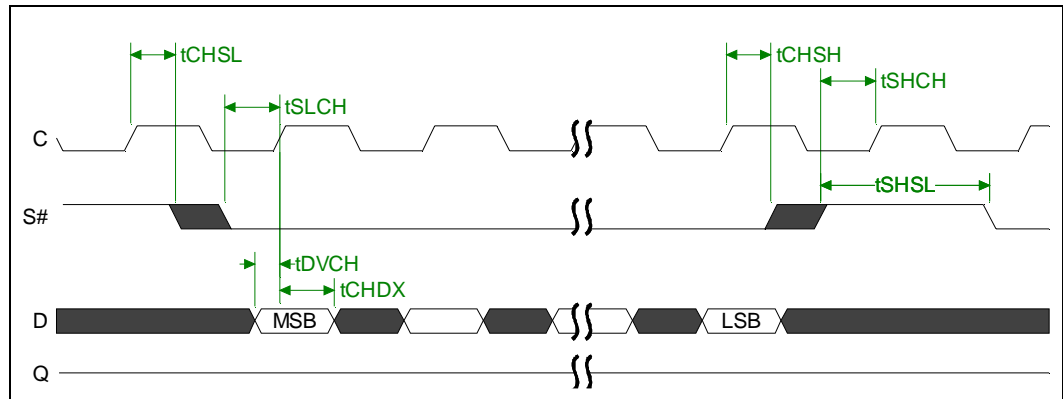
Sym	Parameter	Note	Min	Typ	Max	Unit
F _C	Clock Frequency for all instructions except READ		D.C.		68.0	MHz
F _R	Clock Frequency for READ		D.C.		33.3	MHz
T _{CH}	Clock High Time	1	7			ns
T _{CL}	Clock Low Time	1	7			ns
T _{CLCH}	Clock Rise Time (peak to peak)	2, 3,4	0.1			V/ns
T _{CHCL}	Clock Fall Time (peak to peak)	2, 3,4	0.1			V/ns
T _{CHSL}	S# Active Setup Time (relative to preceding C edge)		5			ns
T _{SLCH}	S# Active Setup Time (relative to subsequent C edge)		5			ns
T _{CHSH}	S# Inactive Hold Time (relative to C)		5			ns
T _{SHCH}	S# Inactive Setup Time (relative to C)		5			ns
T _{SHSL}	S# Deselect Time		100			ns
T _{DVCH}	Data Input Setup Time		2			ns
T _{CHDX}	Data Input Hold Time		5			ns

Notes:

1. T_{CH} + T_{CL} must be greater than or equal to 1/F_C(max).
2. Sampled, not 100% tested.
3. Expressed as a slew-rate

† Minimum clock rise/fall times guarantee functionality. Clock rise/fall times must fall within range specified in Figure 10, "AC Measurement Conditions" on page 20 for compliance to timing specs.

Figure 6. Serial Input Timing



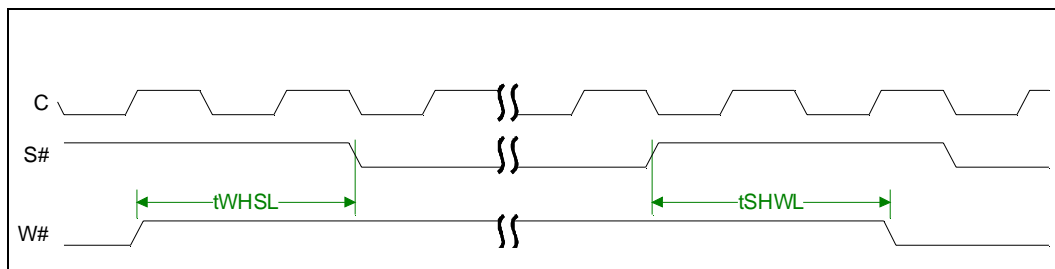
7.2.2 Write Protect Setup and Hold Timing

Table 12. Write Protect Setup and Hold Timing

Sym	Parameter	Note	Min	Typ	Max	Unit
T_{WHSL}	W# Setup Time	1	20			ns
T_{SHWL}	W# Hold Time	1	100			ns

Note:
1. Only applicable as a constraint for a WRSR instruction when SRWD is set to 1.

Figure 7. Write Protect Setup and Hold Timing during WRSR when SRWD=1



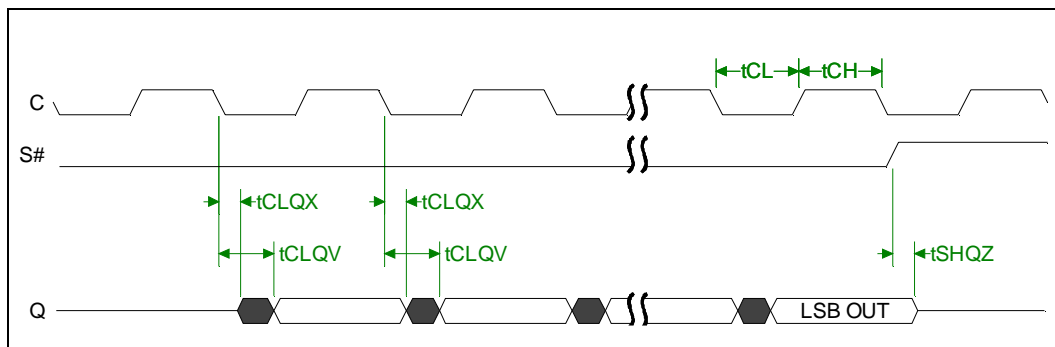
7.2.3 Output Timing

Table 13. Output Timing

Sym	Parameter	Note	Min	Typ	Max	Unit
T_{CLQV}	Clock Low to Output Valid (30 pF, 2.7v to 3.6v)				8	ns
T_{CLQV}	Clock Low to Output Valid (10 pF, 3.0v to 3.6v)				6	ns
T_{CLQX}	Output Hold Time		0			ns
T_{SHQZ}	Output Disable Time	1			8	ns

Note:
1. Sampled, not 100% tested.

Figure 8. Output Timing



7.2.4 Hold Timing

Table 14. Hold Timing

Sym	Parameter	Note	Min	Typ	Max	Unit
T_{CHHL}	HOLD # Assertion Hold Time (relative to C)		5			ns
T_{HLCH}	HOLD # Assertion Setup Time (relative to C)		5			ns
T_{HLQZ}	HOLD # Assertion to Output High-Z	1			8	ns
T_{CHHH}	HOLD # De-assertion Hold Time (relative to C)		5			ns
T_{HHCH}	HOLD # De-assertion Setup Time (relative to C)		5			ns
T_{HHQX}	HOLD # De-assertion to Output Low-Z	1			8	ns

Note:
1. Sampled, not 100% tested.

Figure 9. Hold Timing - Standard Usage

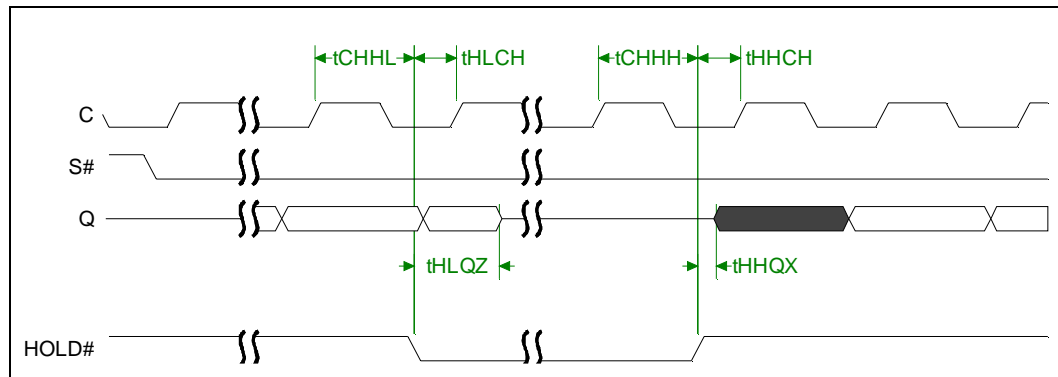
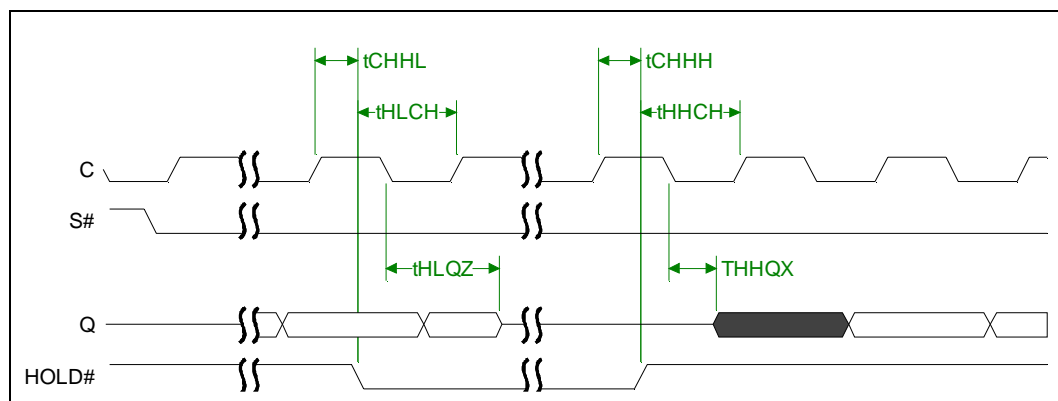


Figure 10. Hold Timing - Non-standard Usage

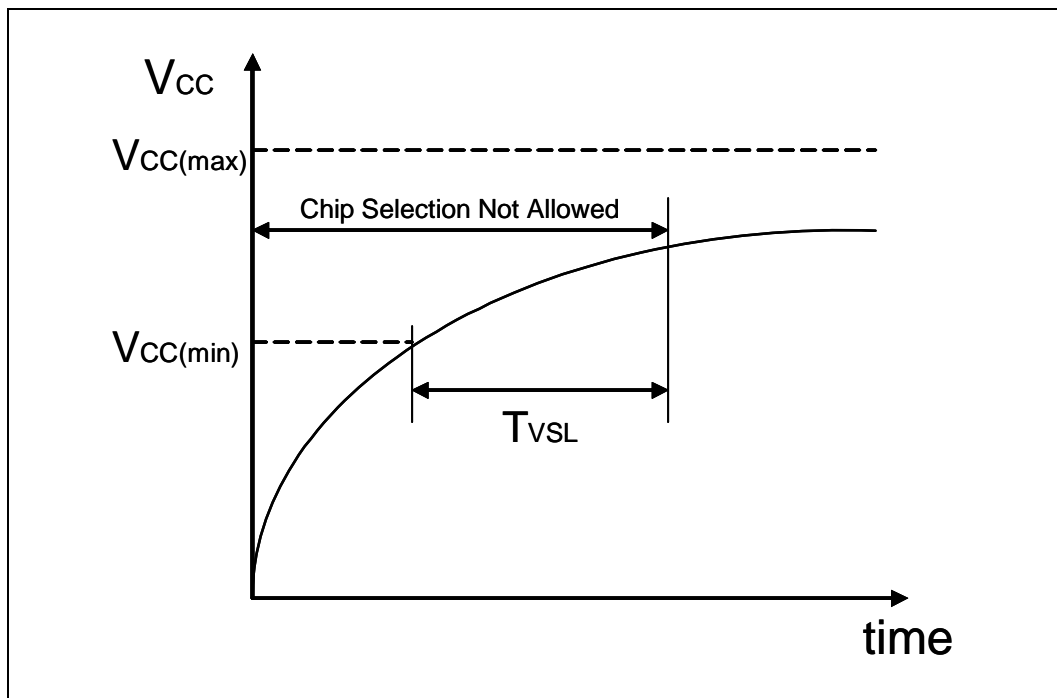


7.2.5 Other Timings

Table 15. Other Timings

Sym	Parameter	Note	Min	Typ	Max	Unit
T _{PP}	Page Program Time	1		1.4	10	ms
T _{BP}	Byte OTP Program Time	1		40	175	us
T _{SE}	Parameter Block Erase Time (8 kB)	1		0.3	2.5	s
	Sector Erase Time (64 kB)	1		0.7	4.0	s
T _{BE}	Bulk Erase Time (64M)	1		89.6	512	s
	Bulk Erase Time (32M)	1		44.8	256	s
	Bulk Erase Time (16M)	1		22.4	128	s
T _{VSL}	V _{CC} power valid to S# assertion (low)		60			us
T _{RDP}	Release from DPD mode into standby mode		60			us

Figure 11. TVSL Power-up Timing



8.0 Device Operations

This section provides an overview of the Intel® Serial Flash Memory (S33) device operations.

8.1 SPI Bus Operations

The SPI instruction cycle begins with a byte-wide OP Code that is initiated with the falling edge of S#. The 8-bit instruction is latched into "D" (Data Input), MSB first, on the rising edge of "C" (SPI clock).

Some OP Codes are followed by additional address, dummy and/or data bytes, MSB first. The number of input instruction bytes depends upon the OP Code. Refer to [Table 16, "SPI Command Set" on page 27](#) for the instruction protocols. Address and dummy bytes are input through "D" on the rising "C" edge. Depending upon the OP Code, the data bytes are either *input* data through the "D", or they are *output* data from "Q". On cycles that *input* data through "D", the output signal "Q" is at high-Z.

For instructions that change the memory contents or device configuration (such as a *Status Register Write* command), the rising S# edge must occur on a whole-byte increment, otherwise the command will be ignored.

For read operations, the instruction sequence can be botched (ignored) only if S# is raised before the input sequence is complete. After the required number of input bits is clocked into the device, a data stream is clocked out of "Q"; each bit is shifted out after the falling edge of "C" (MSB first). When data is streaming from "Q", raising S# will terminate the data stream and bring this output to high-Z.

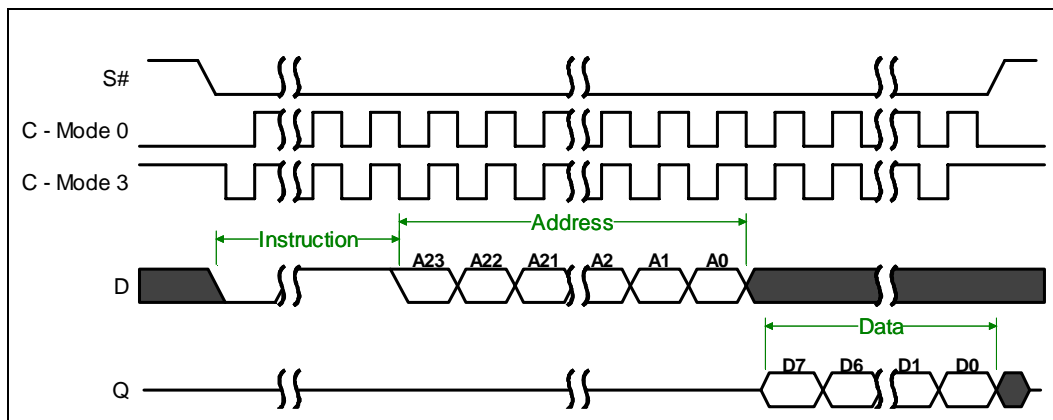
The rising S# edge *always* resets the SPI command interpreter and places the output in high-Z. It also does one of the following actions:

- Terminates the output data stream (Read operations)
- Kicks off program/erase algorithms
- Initiates changes to the SR
- Botches an SPI command when S# is raised too early (or too late for commands that alter the array or device configuration)
- Terminates a command and puts the device in standby mode (not in the case of a Program or Erase operation)

When S# is high and the internal algorithms are completed, the device will go into standby mode.

8.1.1 SPI Modes

This device supports SPI bus operations Mode 0 and Mode 3, as depicted in [Figure 12, "Supported SPI Bus Operation Modes" on page 26](#). The difference between the two modes is the default state of the clock signal ("C") when the SPI bus master is in standby. For Mode 0, the "C" is normally low; for Mode 3, "C" is normally high. For both modes, input data ("D") is sampled on the rising edge of "C", and output data ("Q") is updated on the falling edge of "C".

Figure 12. Supported SPI Bus Operation Modes


8.1.2 The Hold State

The HOLD# input signal freezes the internal SPI Clock (C) without resetting the device's clocking sequence. However, taking HOLD# to VIL does not terminate any program or erase algorithm that is currently in progress.

To enter the *Hold State*, the device must be selected (S# at VIL). The *Hold State* starts on the falling edge of the HOLD# signal, provided that it coincides with the SPI Clock at VIL as shown in [Figure 13 on page 26](#). The *Hold State* ends on the rising edge of HOLD#, provided that it coincides with the SPI Clock at VIL.

If the falling HOLD# edge does not coincide with the SPI Clock at VIL, the *Hold State* starts after the next falling edge of the SPI Clock as shown in [Figure 14 on page 27](#). Similarly, if the rising edge does not coincide with the SPI Clock at VIL, the *Hold State* ends after the next falling edge of the SPI Clock.

The command sequence will not necessarily abort if S# is raised to VIH while HOLD# is at VIL. Raising S# will complete the command sequence, regardless of the state of HOLD#. If a proper sequence was inputted prior to dropping HOLD# to VIL, the input data stream will be recognized as a valid command sequence.

During the *Hold State*, the SPI Data Output (Q) is at high impedance. The SPI Clock Input and the SPI Data Input (D) are *Don't Care*.

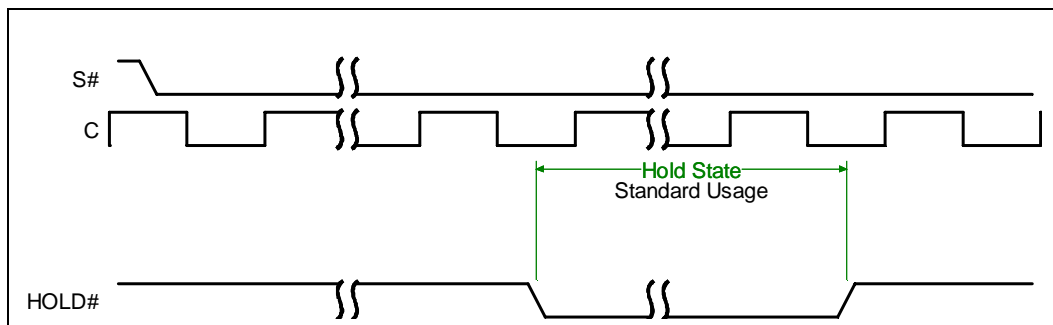
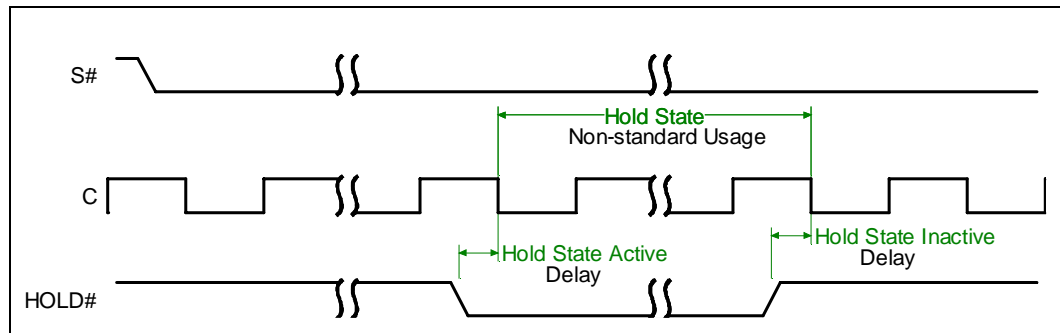
Figure 13. Hold State - Standard Usage


Figure 14. Hold State - Non-standard Usage



8.2 SPI Command Set

The SPI Command Set is found in [Table 16](#). This table defines the commands (and the Op Codes) that are supported by the SPI interface. All other Op Codes will be ignored. All commands support frequencies up to 68 MHz except for the Read Data Bytes command (03h). The Read Data Bytes command (03h) supports up to 33.3 MHz.

Table 16. SPI Command Set (Sheet 1 of 2)

Instruction	Op Code	Addr Bytes	Dummy Bytes	Data Bytes	Name and Function
Write SPI SR	01h	-	-	1	Overwrites SR bits 2-4 & 7 (BP[2:0] & SRWD). When W#=VIL & SRWD=1, the values of BP[2:0] & SRWD cannot be changed.
Page Program	02h	3	-	1 to 256-Byte	Programs up to 256-bytes within a 256-byte-aligned main memory region
Read Data Bytes	03h	3	-	1 to infinite	Supports up to 33.3 MHz Clock.
Write Disable	04h	-	-	-	Resets the WEL (Bit 1 of SR)
Read SPI SR	05h	-	-	1 to infinite	Continuously Polls the SR
Write Enable	06h	-	-	-	Sets the Write Enable Latch (WEL), which is bit 1 of SPI SR.
Fast Read Data Bytes	0Bh	3	1	1 to infinite	Supports up to 68 MHz Clock; protocol uses a dummy byte.
Clear SR Fail Flags	30h	-	-	-	Resets the Erase Fail Flag and the Program Fail Flag (SR bits 5 & 6, respectively)
Parameter Block Erase	40h	3	-	-	Erases the targeted parameter block; it is ignored when the address is outside parameter block space.
OTP Program	42h	3	-	1	Programs one byte of data in the OTP memory space.
Read OTP Data Bytes	4Bh	3	1	1 to infinite	Reads data in the OTP memory space. For details refer to Section 9.1.2, "Reading OTP Data" on page 39.
Read ID	9Fh	-	-	1 to 3	1st Byte = MFG ID, 2nd Byte = Upper Byte of Device ID, 3rd Byte = Lower Byte of Device ID
Release from DPD only	ABh	-	-	-	Brings the device out of DPD mode into standby mode after the TRDP latency.

Table 16. SPI Command Set (Sheet 2 of 2)

Instruction	Op Code	Addr Bytes	Dummy Bytes	Data Bytes	Name and Function
Deep Power-down	B9h	-	-	-	Puts device in DPD mode, whereby all commands are ignored except the <i>Release from DPD</i> command (ABh). In future SPI products, DPD current will be substantially lower than standby current.
Bulk Erase	C7h	-	-	-	Serially erases all main memory Sectors including the eight parameter blocks
Sector Erase	D8h	3	-	-	Erases a 64k-Byte Memory Sector; when addressing a parameter block, it will erase all eight 8k-Byte parameter blocks.

8.2.1 Write SPI SR Command (01h)

The *Write SPI SR* command allows the user to write to writable Status Register bits (i.e. bits 2, 3, 4 & 7). As with any command that writes to the device, the *Write Enable* command must be executed prior to the *Write SPI SR* command in order to set the WEL (Write Enable Latch). If the WEL is not set, the Write SPI SR command will be ignored.

If the device is in Hardware Protect mode, the Write SPI SR command will be ignored and the WEL will be unchanged.

Assuming the WEL is set and the device is not in Hardware Protect mode, the rising edge of S# updates the SPI SR within the TSHSL specification time. If the *Write SPI SR* command is botched (rising S# edge does not occur after exactly sixteen clock cycles), the writable SPI SR bits and the WEL will remain unchanged.

8.2.2 Page Program Command (02h)

The *Page Program* command programs 1 bit to 256 bytes of data with a *256-Byte Aligned* memory segment. This command is used for programming main array memory sectors including the parameter blocks; it is not used for OTP Programming.

The command sequence consists of an 8-bit Op Code, followed by a 24-bit address, followed by the data bytes to be programmed. The data to be programmed must be in whole-byte granularity; otherwise, the command sequence will be ignored. To program in bit granularity, the rest of the bits within the data byte can be set to "1".

The input data stream is loaded into a 256-Byte Program Buffer. The starting address of the Program Buffer is A[7:0] of the user-supplied address, and all subsequent bytes from the input data stream are loaded sequential into the Program Buffer. If the Program Buffer reaches its maximum address, it rolls over, and subsequent data bytes are sequentially loaded starting at the beginning of the Program Buffer.

If more than 256 bytes of data are provided in the command input stream, the Program Buffer will be over-written, replacing the data that was previously loaded. The command sequence ends when S# goes high. When the command sequence ends, the data in the program buffer is programmed in the *256-Byte Aligned* memory segment defined by A[23:8] of the user-supplied address.

A byte count is not required with this command; the end of the data stream is identified with the rising edge of S#.

As with any command that writes to the device or changes the memory contents, the *Write Enable* command must be executed prior to the *Page Program* command in order to set the WEL (Write Enable Latch). If the WEL is not set, the *Page Program* command will be ignored.

If the WEL is set and the address is protected, the program operation will not occur. Instead, the P_FAIL flag of the Status Register will become set and the WEL will become reset.

The *Page Program* command can be botched (cancelled) by failing to raise the S# edge on a whole-byte increment. If the *Page Program* command is botched:

- The WEL will not reset.
- SR Fail Flags (described in [Table 17](#)) will not be set.
- None of the bytes written into the program buffer will be programmed into the flash array.

Assuming the WEL is set, the address is unprotected, and the command is not botched, the rising edge of S# initiates the program operation. This program operation cannot be terminated without powering off the device, and doing so will result in unexpected data.

8.2.3 Read Data Bytes Command (03h)

The *Read Data Bytes* command requires a 3-byte address. After the last address byte is clocked in (on the rising clock edge), the first data bit is clocked out on the subsequent falling clock edge. Data clocks out continuously and sequentially as long as S# remains low. When the address reaches its maximum, it wraps back to zero. The *Read Data Byte* command supports up to 33.3 MHz.

8.2.4 Write Disable Command (04h)

The *Write Disable* command resets the WEL, which corresponds to bit 1 of the SPI SR. Resetting the WEL disables the following commands:

- Write SPI SR
- Page Program
- OTP Program
- Bulk Erase
- Parameter Block Erase
- Sector Erase

These commands can be re-enabled by executing the *Write Enable* command as described in [Section 8.2.6](#). At power-up, the WEL is reset.

8.2.5 Read SPI SR Command (05h)

The *Read SPI SR* command continuously polls the SPI Status Register. As long as S# remains low, a refreshed version of the status register is continuously clocked out. The *Read SPI SR* command does not require address bytes, data bytes or dummy bytes.

8.2.6 Write Enable Command (06h)

The *Write Enable* command sets the WEL, which corresponds to bit 1 of the SPI SR. Setting the WEL enables the following commands:

- Write SPI SR

- Page Program
- OTP Program
- Bulk Erase
- Parameter Block Erase
- Sector Erase

These commands can be disabled by executing the *Write Disable* command as described in [Section 8.2.4](#). At power-up, the WEL is reset.

8.2.7 Fast Read Data Bytes Command (0Bh)

The *Fast Read Data Bytes* command requires a 3-byte address. After the last address byte is clocked in (on the rising clock edge), a dummy byte latency occurs (8 clock cycles) before the first data bit is clocked out on the falling clock edge. Data clocks out continuously and sequentially as long as S# remains low. Refer to [section Section 8.4.1, “Fast Read” on page 35](#) for a detailed description of the *Fast Read Data Bytes* command. When the address reaches its maximum, it wraps back to zero. The *Fast Read Data Bytes* command supports up to 68 MHz, but it requires a dummy byte to allow time for the first Read latency.

8.2.8 Clear SR Fail Flags Command (30h)

The *Clear SR Fail Flags* command resets SR bit 5 (the Erase Fail Flag) and SR bit 6 (the Program Fail Flag). It is not necessary to set the WEL before the *Clear SR Fail Flags* command is executed; after this command is executed the WEL will be unchanged.

8.2.9 Parameter Block Erase Command (40h)

The *Parameter Block Erase* command is used to erase an 8k-byte Parameter block. The command sequence consists of the Op Code followed by an address within the targeted block.

As with any command that writes to the device or changes the memory contents, the *Write Enable* command must be executed prior to the *Parameter Block Erase* command in order to set the WEL (Write Enable Latch). If the WEL is not set, the *Parameter Block Erase* command will be ignored.

If the WEL is set and one of the following is true:

- the address is not an 8k-byte Parameter Block Address
- the address is protected

the erase operation will not occur. Instead, the E_FAIL flag of the Status Register will become set and the WEL will become reset.

The Parameter Block Erase command can be botched (cancelled) by failing to raise the S# edge after exactly thirty-two clock cycles. If the Parameter Block Erase command is botched, the WEL will not reset and the E_FAIL flag will not set.

Assuming the WEL is set, the address is an unprotected 8k-Byte Parameter Block Address, and the command is not botched, the rising edge of S# initiates the erase operation. This erase operation cannot be terminated without powering off the device and doing so will result in unexpected data.

8.2.10 OTP Program Command (42h)

The *OTP Program* command programs data in the OTP region, which is in a different address space from the main array data. Refer to [Section 9.1, "OTP Memory Space" on page 39](#) for details on the OTP region. The protocol of the *OTP Program* command is the same as the *Page Program* command, except that the *OTP Program* command requires exactly one byte of data; otherwise, the command will be ignored. To program the OTP in bit granularity, the rest of the bits within the data byte can be set to "1".

If the WEL is set and the address is not a valid OTP address, the program operation will not occur. Instead, the F_FAIL flag of the Status Register will become set and the WEL will become reset.

The OTP memory space can be programmed one or more times, provided that the OTP memory space is not locked (as described in [Section 9.1.3, "Lock Protection Registers" on page 39](#)). Subsequent OTP programming can be performed only on the unprogrammed bits (i.e. "1" data).

8.2.11 Read OTP Data Bytes Command (4Bh)

The *Read OTP Data Bytes* command reads data from the OTP region. Refer to [Section 9.1, "OTP Memory Space" on page 39](#) for details on the OTP region. The protocol of the *Read OTP Data Bytes* command is the same as the *Fast Read Data Bytes* command except that it will not wrap to the starting address after the OTP address is at its maximum; instead, the data will be indeterminate.

8.2.12 Read ID Command (9Fh)

The *Read ID* command reads three bytes of data. It does not require any address bytes, data bytes or dummy bytes. After inputting the Op code, three bytes are clocked out of the device: the MFG ID, the first byte of the Device ID, and the second byte of the Device ID. Refer to [Table 21, "Intel® Serial Flash Memory \(S33\) Device IDs" on page 41](#) for the MFG ID and Device IDs of Blanshard. If S# is held low after the third byte of data, the subsequent data is indeterminate.

8.2.13 Release from DPD Command (ABh)

In Deep Power-down mode, the only command that the SPI interface will recognize is the *Release from DPD* command. After issuing this command, the T_{RDP} latency is required before S# can go low to initiate another command. The only other way to release the device from DPD mode is to power it off and on.

When issuing a *Release from DPD* command, it is not necessary to raise S# after exactly eight clock cycles. After inputting the 8-bit Op Code, all subsequent bits in the command sequence will be ignored.

8.2.14 Deep Power-down Command (B9h)

The *Deep Power-down* command puts the device in DPD mode, whereby all commands are ignored except the *Release from DPD* command (ABh). In future SPI Flash devices, this mode will reduce the current consumption substantially, but a wake-up time will be required before the first read yields valid data.

8.2.15 Bulk Erase Command (C7h)

The *Bulk Erase* command serially erases the entire Main Array, including the parameter blocks (but excluding the OTP memory space).

As with any command that writes to the device or changes the memory contents, the *Write Enable* command must be executed prior to the *Bulk Erase* command in order to set the WEL (Write Enable Latch). If the WEL is not set, the *Bulk Erase* command will be ignored.

If the WEL is set and there is at least one memory sector that is protected, the erase operation will not occur. Instead, the E_FAIL flag of the Status Register will become set and the WEL will become reset.

The *Bulk Erase* command can be botched (cancelled) by failing to raise the S# edge after exactly eight clock cycles. If the *Bulk Erase* command is botched, the WEL will not reset and the E_FAIL flag will not set.

Assuming the WEL is set, all memory sectors are unprotected, and the command is not botched, the rising edge of S# initiates the erase operation. This erase operation cannot be terminated without powering off the device, and doing so will result in unexpected data.

8.2.16 Sector Erase Command (D8h)

The *Sector Erase* command is used to erase a 64k-Byte memory sector. The command sequence consists of an 8-bit Op code followed by a 24-bit address. If the address is within the parameter block address range ($A[\text{max:16}] = 0$), all eight parameter blocks will be erased. (With this characteristic, the device behaves as a symmetrically blocked device.)

As with any command that writes to the device or changes the memory contents, the *Write Enable* command must be executed prior to the *Sector Erase* command in order to set the WEL (Write Enable Latch). If the WEL is not set, the *Sector Erase* command will be ignored.

If the WEL is set and the address is protected, the erase operation will not occur. Instead, the E_FAIL flag of the Status Register will become set and the WEL will become reset.

The *Sector Erase* command can be botched (cancelled) by failing to raise the S# edge after exactly thirty-two clock cycles. If the *Sector Erase* command is botched, the WEL will not reset and the E_FAIL flag will not set.

Assuming the WEL is set, the address is an unprotected, and the command is not botched, the rising edge of S# initiates the erase operation, it cannot be terminated without powering off the device, and doing so will result in unexpected data.

8.3 SPI Status Register Definition

The SPI Status Register bit definition can be found in [Table 17](#). The SPI Status Register has program/erase fail flags, and it contains writable bits that define the program/erase protection within the Flash array. All Status Register bits are volatile.

Table 17. SPI Status Register Bit Definition

SR Bit	Bit Name	Bit Description	Power-up State	Write/Read Capability
7	SRWD	Status Register Write Disable - When this writeable bit is set and W# is low, none of the writable SPI SR bits can be changed including this bit (i.e. bits 2,3,4 & 7). For details, refer to Table 20, "Main Array Protection Modes" on page 35 . This bit is volatile.	0	Read/Write ⁽¹⁾
6	P_FAIL	Program Fail Flag - When set, this bit indicates that a program failure occurred. This bit will also be set when the user attempts to program a protected main memory region or a locked OTP region. However, the <i>Program Fail Flag</i> will not be set under the following scenarios: <ul style="list-style-type: none"> • Botched Command Sequence (i.e. S# edge not raised on a whole-byte increment) • <i>Write Enable Latch</i> bit is reset (i.e. SR[1]=0) After a series of program operations, this bit indicates whether one or more of these operations failed. Once set, this bit is reset with the <i>Clear SR Fail Flag</i> command.	0	read only ⁽²⁾
5	E_FAIL	Erase Fail Flag - When set, this bit indicates that an erase failure occurred. This bit will also be set when the user attempts to erase a protected main memory region. However, the <i>Erase Fail Flag</i> will not be set under the following scenarios: <ul style="list-style-type: none"> • Botched Command Sequence (i.e. S# edge not raised on a whole-byte increment). • <i>Write Enable Latch</i> bit is reset (i.e. SR[1]=0) After a series of erase operations, this bit indicates whether one or more of the operations failed. Once set, this bit is reset with the <i>Clear SR Fail Flag</i> command.	0	read only ⁽²⁾
4	BP2	Sector Protect Bits - These bits define the lock region of the Main Memory. A locked region is one or more adjacent memory sectors that are protected from program or erase. For further details, refer to Table 18 . When all three of these bits are 0, the entire Main Array is unlocked. These bits are volatile; at power-up, these bits are set to "1".	1	Read/Write ⁽¹⁾
3	BP1		1	Read/Write ⁽¹⁾
2	BP0		1	Read/Write ⁽¹⁾
1	WEL	Write Enable Latch - This bit must be set prior to the following SPI Commands: <ul style="list-style-type: none"> • Write SPI SR • Page Program • OTP Program • Bulk Erase • Parameter Block Erase • Sector Erase After issuing one of these commands, the <i>Write Enable Latch</i> (WEL) will reset when the command is completed. The WEL will not be reset if the command is botched by not raising S# on a whole-byte increment.	0	read only ⁽³⁾
0	WIP	Write in Process - When a program, erase, or write to the SR is in process (busy), the WIP reads as 1. When the WIP is zero, the SPI interface is in its ready state.	0	read only
<p>Notes:</p> <ol style="list-style-type: none"> 1. Refer to Table 20, "Main Array Protection Modes" on page 35 for writable conditions. 2. The Program and Erase Fail flags are not directly writable, but they can be reset with the <i>Clear SR Fail Flag</i> command. This is true regardless of the protection modes described in Table 20. 3. The WEL is not directly writable but it can be set with the <i>Write Enable</i> command and reset with the <i>Write Disable</i> command. This is true regardless of the protection modes described in Table 20. 				

8.3.1 Main Memory Protection

Main Memory program/erase Protection is defined by four Status Register bits and the W# input signal. Table 18 define the memory protection regions. Table 20 defines the SR and W# configurations for *Software Protection Mode* and *Hardware Protection Mode*.

Table 18. Main Array Protection Regions - Bottom Boot

Status Register Bits			Protected Main Memory Sectors		
BP2	BP1	BP0	64M	32M	16M ⁽¹⁾
0	0	0	None	None	None
0	0	1	Sectors 126 - 127 (upper 1/64)	Sector 63 (upper 1/64)	Sector 31 (upper 1/32)
0	1	0	Sectors 124 - 127 (upper 1/32)	Sectors 62 - 63 (upper 1/32)	Sectors 30 - 31 (upper 1/16)
0	1	1	Sectors 120 - 127 (upper 1/16)	Sectors 60 - 63 (upper 1/16)	Sectors 28 - 31 (upper 1/8)
1	0	0	Sectors 112 - 127 (upper 1/8)	Sectors 56 - 63 (upper 1/8)	Sectors 24 - 31 (upper 1/4)
1	0	1	Sectors 96 - 127 (upper 1/4)	Sectors 48 - 63 (upper 1/4)	Sectors 16 - 31 (upper 1/2)
1	1	0	Sectors 64 - 127 (upper 1/2)	Sectors 32 - 63 (upper 1/2)	All Sectors
1	1	1	All Sectors	All Sectors	All Sectors

Note:
1. 16M main memory protection scheme applies to 32M configured as 16M.

Table 19. Main Array Protection Regions - Top Boot

Status Register Bits			Protected Main Memory Sectors		
BP2	BP1	BP0	64M	32M	16M ⁽¹⁾
0	0	0	None	None	None
0	0	1	Sectors 0- 1 (lower 1/64)	Sector 0 (lower 1/64)	Sector 0 (lower 1/32)
0	1	0	Sectors 0-3 (lower 1/32)	Sectors 0-1 (lower 1/32)	Sectors 0-1 (lower 1/16)
0	1	1	Sectors 0-7 (lower 1/16)	Sectors 0-3 (lower 1/16)	Sectors 0-3 (lower 1/8)
1	0	0	Sectors 0- 15 (lower 1/8)	Sectors 0-7 (lower 1/8)	Sectors 0-7 (lower 1/4)
1	0	1	Sectors 0-31 (lower 1/4)	Sectors 0-15 (lower 1/4)	Sectors 0-15 (lower 1/2)
1	1	0	Sectors 0-63 (lower 1/2)	Sectors 0-31 (lower 1/2)	All Sectors
1	1	1	All Sectors	All Sectors	All Sectors

Note:
1. 16M main memory protection scheme applies to 32M configured as 16M.

Table 20. Main Array Protection Modes

W# Signal	SRWD Bit (SR[7])	Mode	Protection of SR
VIL	0	Software Protect	The SRWD bit (SR[7]) and the BP bits (SR[4:2]) are writable.
VIL	1	Hardware Protect	The SRWD bit (SR[7]) and the BP bits (SR[4:2]) are <i>not</i> writable. These bits cannot be altered without raising W# to VIH or device power-up. In this configuration, the Main Array Protection Regions cannot be changed.
VIH	0	Software Protect	The SRWD bit (SR[7]) and the BP bits (SR[4:2]) are writable.
VIH	1	Software Protect	The SRWD bit (SR[7]) and the BP bits (SR[4:2]) are writable.

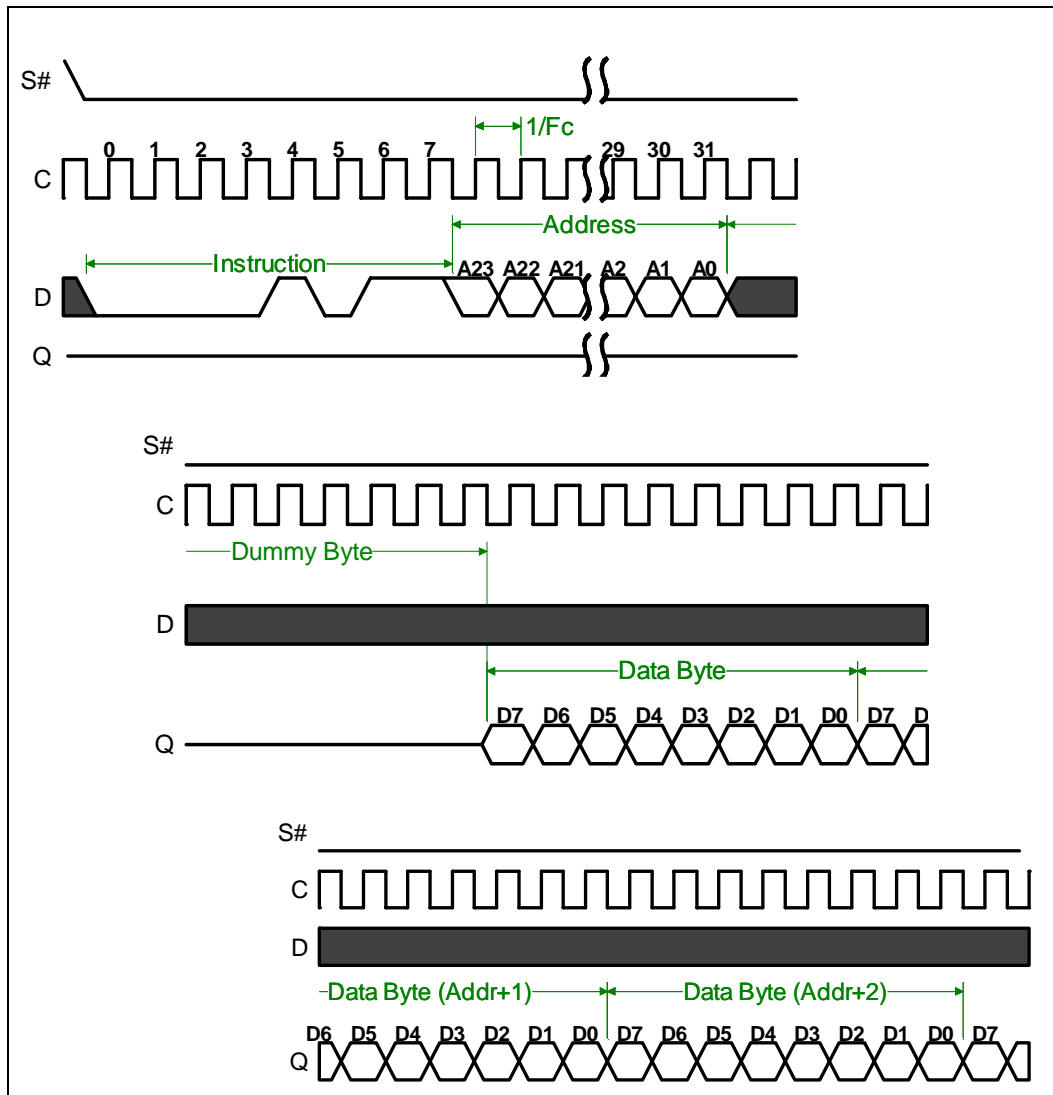
8.4 SPI Instruction Cycle Examples

In this section, two SPI instruction cycles are explained in detail to provide a thorough understanding of SPI instruction cycles in general. The intent of these examples is to provide a foundation for all SPI instructions.

8.4.1 Fast Read

A *Fast Read* instruction uses 0Bh as an OP Code. After clocking in the OP Code, a 3-byte address is clocked in (starting with the MSB), followed by a dummy byte. The output serial data stream is clocked out on the *falling* edge of "C", one-half cycle after the last dummy bit is clocked in. The timing diagram for a Fast Read command sequence can be found in [Figure 15, "Timing Diagram for SPI Fast Read Command Sequence"](#) on page 36.

Within the SPI interface, the address is automatically incremented internally as the data is clocked out continuously and sequentially, as long as S# remains low. The output data stream can be paused by bringing HOLD# low, and it can be continued by bring it high again. When the internal address reaches the last address within the device's range, it will wrap to address 0. When the user brings S# high, the instruction cycle is terminated, and the data output (Q signal) becomes tri-stated.

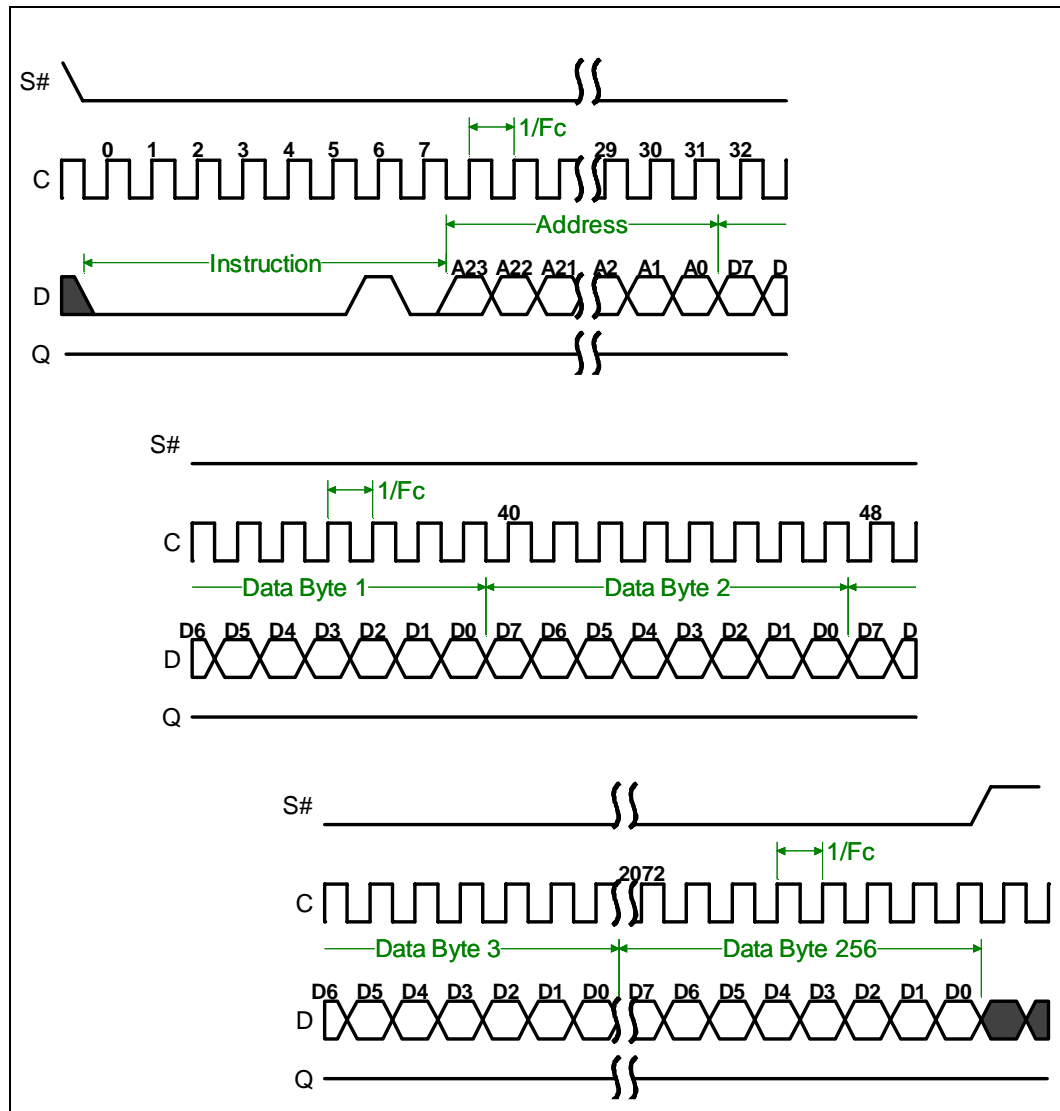
Figure 15. Timing Diagram for SPI Fast Read Command Sequence


8.4.2 Page Program

A *Page Program* instruction consists of an OP Code (02h) followed by a 3-byte address and a variable number of data bytes, up to the size of the program buffer (page). Assuming S# goes high on a whole-byte increment, the SPI module will instruct the WSM to initiate programming, otherwise the Page Program instruction will botch (and nothing will be programmed). The timing diagram for a Page Program command sequence can be found in [Figure 16, "Timing Diagram for SPI Page Program Command Sequence"](#) on page 37.

To monitor when the program algorithm is complete, an *SPI Read SR* command must be issued. The *SPI Read SR* command is the only instruction that the device will recognize while a Write is in process.

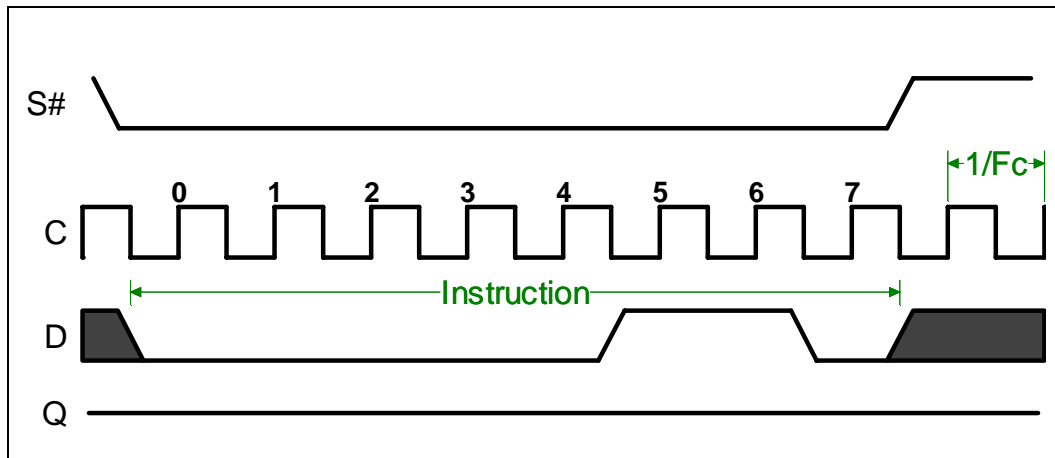
Figure 16. Timing Diagram for SPI Page Program Command Sequence



8.4.3 Write Enable

For write operations such as the *Page Program* operation, the single-byte *Write Enable* command sequence must be issued to set the *Write Enable Latch* (WEL) prior to issuing the *Page Program* operation. Without setting the WEL, the subsequent *Page Program* operation will be ignored. Just as with any other command that alters the configuration, the Write Enable command is completed on the rising edge of S#. The timing diagram for a *Write Enable* command sequence can be found in [Figure 17, "Timing Diagram for Write Enable Command Sequence"](#) on page 38.

Figure 17. Timing Diagram for Write Enable Command Sequence



9.0 Security Features

This section describes the security features of the Intel® Serial Flash Memory (S33) device that go beyond the typical SPI Flash feature set.

9.1 OTP Memory Space

The Intel® Serial Flash Memory (S33) contains two 8-Byte, thirty 16-Byte, and one 10-Byte individually lockable OTP regions (protection registers) within an address space that is separate from the Main Array. Refer to [Figure 18, “OTP Memory Map” on page 40](#) for a pictorial representation of the OTP memory space.

The two 8-Byte protection registers are intended for increased system security. Protection register values can “mate” a flash component with system CPU/ASIC to prevent device substitution. Intel’s factory programs one 8-Byte protection register with a unique, unchangeable 64-bit number. The other 64-bits are blank so customers can program them for a similar purpose.

Once programmed, each customer segment (one 8-Byte segment, thirty 16-Byte segments, and one 10-Byte segment) can be locked to prevent further reprogramming.

9.1.1 Programming OTP Address Space

For the description and SPI protocol of the OTP Program command, refer to [Table 16, “SPI Command Set” on page 27](#). The protocol of this command is the same as Page Program.

The OTP Program command can be issued multiple times to any given OTP address, but this address space can never be erased. After a given OTP segment is programmed, it can be locked to prevent further programming with the Lock Protection registers, which are describe in [Section 9.1.3](#).

The valid address range for OTP Program is depicted in [Figure 18, “OTP Memory Map” on page 40](#). OTP Program operations outside the valid OTP address range will be ignored.

9.1.2 Reading OTP Data

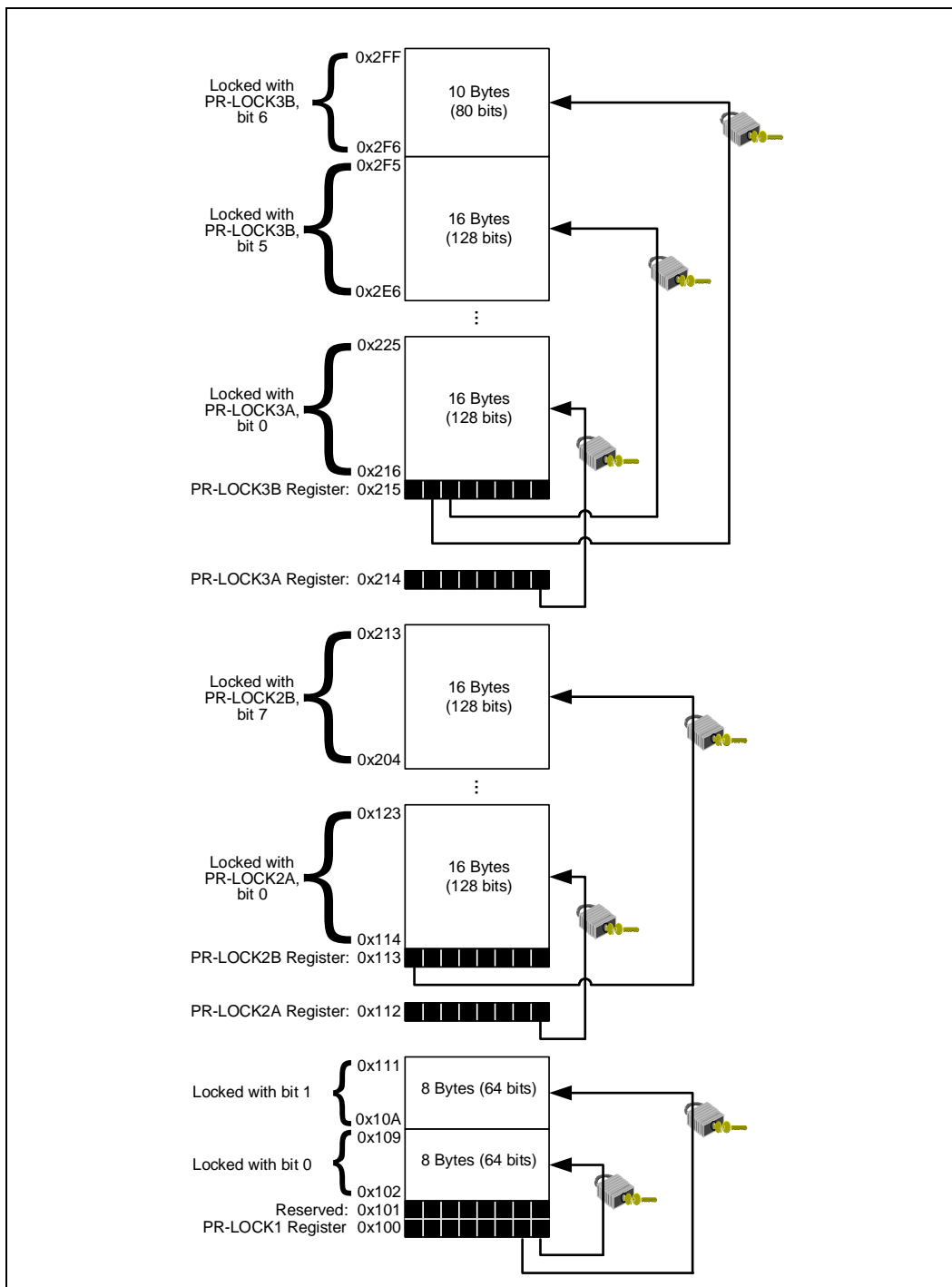
For the description and SPI protocol of the OTP Read command, refer to [Table 16, “SPI Command Set” on page 27](#). The protocol of this command is the same as Fast Read.

The valid address range for OTP Reads is depicted in [Figure 18, “OTP Memory Map” on page 40](#). OTP Read operations outside the valid OTP address range will yield Indeterminate data.

9.1.3 Lock Protection Registers

The Lock Protection Registers (PR-LOCK1, PR-LOCK2, and PR-LOCK3) are illustrated in [Figure 18, “OTP Memory Map” on page 40](#). PR-LOCK1 is used to permanently lock OTP addresses 0x102 through 0x111; PR-LOCK2 is used to permanently lock OTP addresses 0x114 through 0x213; PR-LOCK3 is used to permanently lock OTP addresses 0x216 through 0x2FF.

Figure 18. OTP Memory Map



Note: OTP Bytes 0x102 through 0x109 will be programmed at Intel's factory with an unchangeable, unique identifier, and bit 0 of PR-LOCK1 register will be programmed to 0.

10.0 Intel® Serial Flash Memory (S33) ID Codes

The Manufacturer ID is 89h, and the Device IDs are found in [Table 21](#).

Through the SPI Command Set, OP code 9Fh is required. The first byte of Read data is the Manufacturing ID (89h); the second byte is the upper byte of the Device ID, and the third byte is the lower byte of the Device ID.

Table 21. Intel® Serial Flash Memory (S33) Device IDs

Device	Device ID (Device Code)	Mode
Blanshard 64M	8913	Bottom Boot
Blanshard 32M	8912	Bottom Boot
Blanshard 16M	8911	Bottom Boot
Blanshard 64M	8917	Top Boot
Blanshard 32M	8916	Top Boot
Blanshard 16M	8915	Top Boot

Appendix A Write State Machine (WSM)

Table 22 and Table 23 shows the command state transitions (Next State Table) based on incoming commands.

Table 22. Chip State and Output State Transitions (Sheet 1 of 2)

Current Chip State	Command Input to Chip and Resulting Chip Next State (1 of 2)								
	Write SPI SR	Page Program	Read Data Bytes	Write Disable	Read SPI SR	Write Enable	Fast Read Data Bytes	Clear SR Fail Flags	Param Block Erase
	01h	02h	03h	04h	05h	06h	08h	30h	40h
Ready, WEL=0	Ready WEL=0 (command ignored)								Ready WEL=0 (command ignored)
Ready, WEL=1	Ready. If Software Protected, SR Write occurs and WEL=0. Else, command is ignored and WEL=1. (see note 1)	If targeted address is protected, device is Ready and WEL=1. Else, device is busy and WEL=x. (see note 2)	Ready WEL doesn't change (Array Data Output)	Ready WEL=0	Ready WEL doesn't change (SR Output)	Ready WEL=1	Ready WEL doesn't change (Array Data Output)	Ready WEL doesn't change	If targeted address is protected and a valid parameter block address, device is Ready and WEL=1. Else, device is busy and WEL=x. (see note 2)
DPD, WEL=x	DPD, WEL doesn't change (command ignored)								
Busy	Busy (command ignored)				Busy (SR Output)	Busy (command ignored)			

Notes:

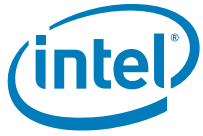
1. Refer to [Table 20](#) for details on HW/SW protection.
2. Refer to [Table 20](#) for details on address protection.
3. Refer to [Section 9.0, "Security Features"](#) for details on OTP protection.
4. Refer to [Table 17](#) for details on the Status Register.

Table 23. Chip State and Output State Transitions (Sheet 2 of 2)

Current Chip State	Command Input to Chip and resulting Chip Next State (2 of 2)								
	OTP Program	Read OTP Data Bytes	Read JEDEC ID	Release from DPD	Deep Power-down	Bulk Erase	Sector Erase	Power Cycle (off, then on)	Program or Erase Operation Completes
	42h	4Bh	9Fh	ABh	B9h	C7h	D8h		
Ready, WEL=0	Ready WEL=0 (command ignored)	Ready WEL doesn't change (OTP Data Output)	Ready WEL doesn't change (ID Output)	Ready WEL doesn't change	DPD, WEL doesn't change	Ready WEL=0 (command ignored)		Ready, SR= 1Ch (see note 4)	N/A
Ready, WEL=1	If targeted address is protected, device is Ready and WEL=1. Else, device is busy and WEL=x. (see note 3)					If any main memory is protected, device is Ready and WEL=1. Else, device is busy and WEL=x. (see note 2)	If targeted address is protected, device is Ready and WEL=1. Else, device is busy and WEL=x. (see note 2)		
DPD, WEL=x	DPD, WEL doesn't change (command ignored)					DPD, WEL doesn't change (command ignored)			
Busy	Busy (command ignored)								Ready, WEL = 0

Notes:

1. Refer to [Table 20](#) for details on HW/SW protection.
2. Refer to [Table 20](#) for details on address protection.
3. Refer to [Section 9.0, "Security Features"](#) for details on OTP protection.
4. Refer to [Table 17](#) for details on the Status Register.



Appendix B Additional Information

Order/Document Number	Document/Tool

Appendix C Ordering Information

Figure 19. Ordering Information

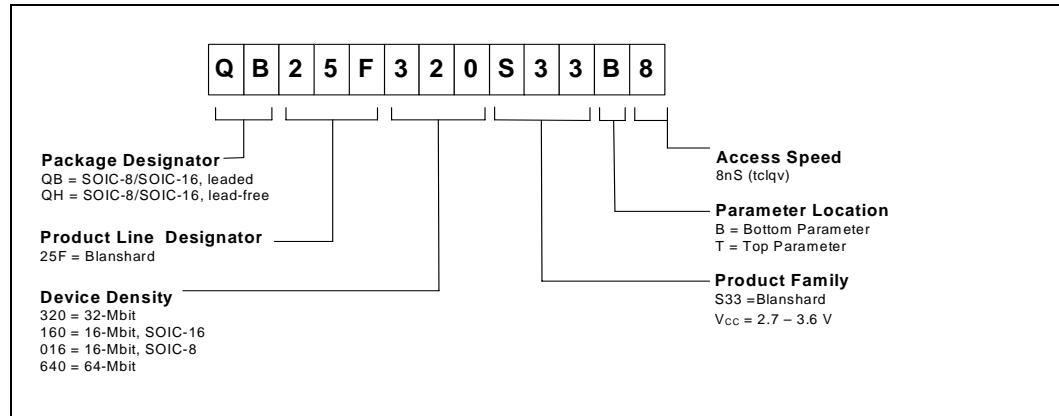


Table 24. Valid Combinations for Intel® Serial Flash Memory (S33)

32-Mbit
QB25F320S33B8
QB25F320S33T8
QH25F320S33B8
QH25F320S33T8

Notes:

- The Top Boot parts are available only on special request, they cannot be ordered.