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USING DRAGONKAT II LCD CHIP-SET IN HAND-WRITING APPLICATIONS

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INTRODUCTION

DragonKat II is a chip-set solution offered by Motorola for high density graphic LCD systems (with 146 mux and more than 160 segments). It includes a microcontroller (MCU) MC68HC05L11, a cascadable LCD backplane (or common) driver MC141512 and a cascadable LCD segment (or column) driver MC141514. When linked up to a touch sensitive panel, the system can accept and display handwriting inputs. The purpose of this document is to illustrate a pen-based system using this chip set. First the display output unit will be described. Then follows the hand-writing input system. Finally, they are integrated and a demonstration software for doing handwriting/erasing will be presented.

USING DRAGONKAT II LCD CHIP-SET TO BUILD A 164 x 320 LCD SYSTEM

MC68HC05L11 is a fully static single chip CMOS microcomputer. It has 448 bytes of RAM of which 64 bytes are for stack, 3584 bytes of ROM, one crystal oscillator generating clock for a real time clock and one PLL frequency synthesizer for MCU's system clock, 38 bidirectional I/O lines, 2 serial communication interfaces (an SCI[1] and an SPI[2]), one 16-bit timer, a memory management unit to page in as much as 8 Mega-bytes logical address into a 64k physical address and a special LCD Control Unit. This MCU has all the features that make it an ideal part for electronic organizer, personal data bank, dictionary, game and other handheld terminal or measurement equipment applications.

The segment driver MC141514, as in Figure 1, is designed to generate segment-driving waveforms[3] for passive LCD panels. (It is customary to name the vertical lines of a LCD panel as segments and its horizontal lines as backplanes. Pixels are positioned at where these lines intercept.) MC141514 has 160 outputs and is cascadable for higher segment count. Inside there is a Static RAM matrix of 146 rows by 160 bits for image storage.

1. Serial Communications Interface (SCI) supports full-duplex asnychrono as communication with standard NRZ format in number of standard baud rates
2. Serial Peripherals Interface (SPI)is a Motorola's proprietary standard for snychronous communication

3. See MC141514 Product Specification.

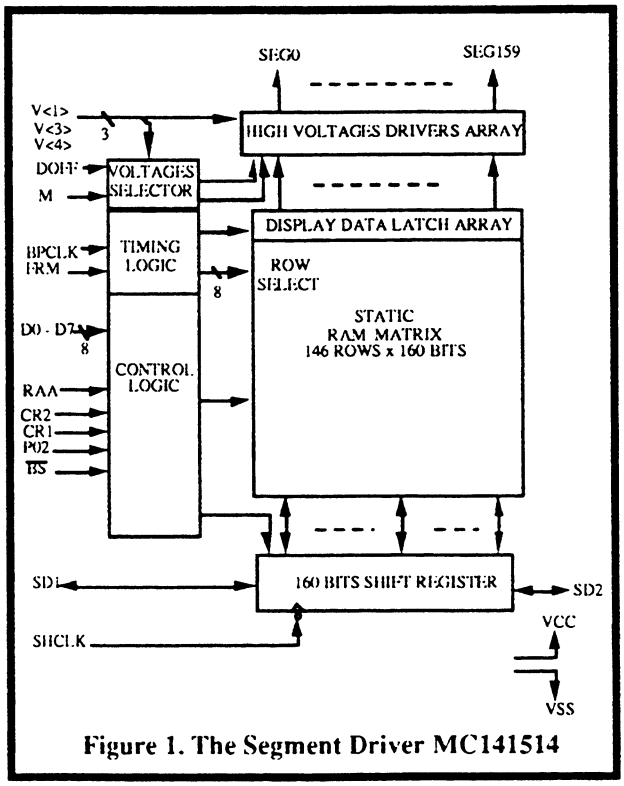

Figure 1. The Segment Driver MC141514

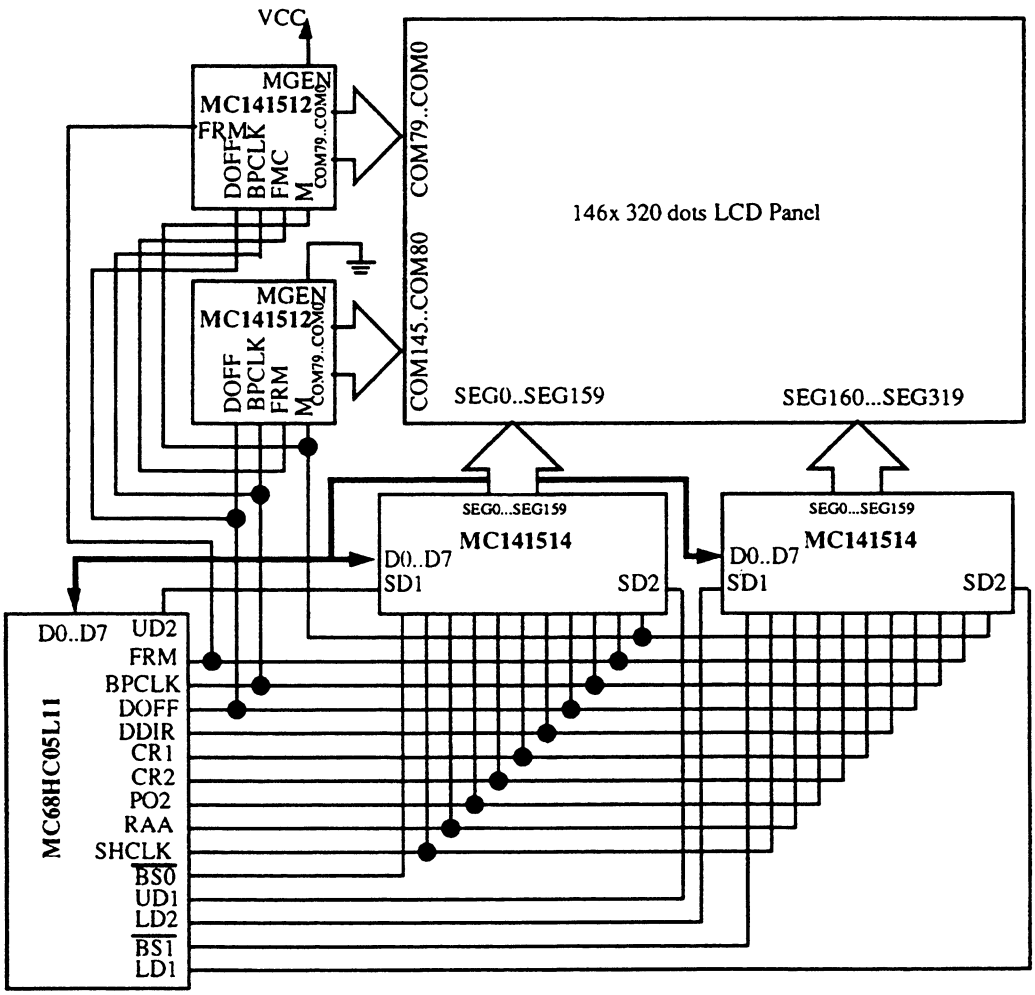

Figure 2. A 146x320 LCD SYSTEM

Any of these rows can be selected and its contents fetched for segment output display or transferred to a 160-bit wide bidirectional shift register in a parallel fashion. Conversely, the content of the 160-bit bidirectional shift register can be stored in any of the 146 rows. The bidirectional shift register serves as the gateway for transporting video data between the MCU and segment drivers. Since the content is stored in the segment driver(s), the LCD screen refresh is handled automatically by an internal wrap-around counter that sequentially scans each row for segment output in a repetitive manner. The MCU is required to access the segment driver(s) only if the screen content is to be altered.

The backplane driver MC141512 is designed to supply the backplane waveforms to a passive LCD panel. The mechanism is driven by a marching "1" along 80-bit shift register. At the start of a refresh cycle, the Frame signal (FRM) feeds a logic one momentarily into the first bit of the shift register. The lone "1" is shifted to the next higher order bit successively on each BPCLK pulse. Effectively each row of pixels on the LCD screen is sequentially selected during a refresh cycle.

Figure 2 shows an LCD system built with the DragonKat II chip-set. It consists of two backplane drivers, two segment drivers, one MCU and an LCD panel. The MCU communicates with the drivers through a special circuit block, the LCD Control Unit, as shown on Figure 3. This unit is designed to facilitate graphic manipulations such as smooth scrolling in "x" or "y" directions, variable pitch editing and window partitioning. However, it must work with the two drivers (the backplane driver MC141512 and the segment driver MC141514) in order to perform graphic functions. It can be divided into three functional blocks: a serial data interface, a parallel control interface and a timing generator as shown in Figure 3. The timing generator provides the necessary signals for system synchronization. The unit, most of the time, communicates with its drivers through the serial and parallel interfaces. Which are designed for different purposes: the serial interface is for video data transfer while the parallel one is for issuing commands. It is vital to have a serial transfer mechanism because of

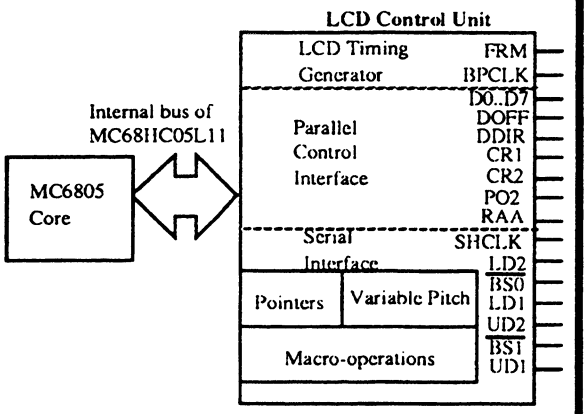

Figure 3. The LCD Control Unit

its capability to shift data bit by bit. Also, it can shift to the left or right so as to allow smooth horizontal scroll in either directions. Figure 2 also shows the physical connections between the serial interface and the bidirectional shift registers of the segment drivers. As mentioned before the bidirectional shift register is a gateway for transporting video data, it can also serve as a parallel dump for a row of video content. Its length is same as the width of the video RAM. In our case here, the segment driver MC141516 has 160 bits per row of video RAM, therfore, the bidirectional shift register is 160 bits long. It can be easily observed that the serial connections are closed to form a loop. In Figure 2, there are two of these loops. Usually, only one loop is enough to support a long single LCD panel because more than one segment drivers can be cascaded to form a longer loop. However, the system shown uses two loops to support a single panel (one segment driver per loop) to shorten the loop path so as to increase the accessing speed. In the normal case, a separate loop drives each half of a split panel.

Other than serial data transfer operations, the serial port has a few more supporting circuits built-in i.e. the pointers, the variable pitch access logic and a macro-operations block. The macro-operations block can do four macro-operations while the pointers and variable pitch access block set up boundary conditions and access pitch respectively for these macro-operations. Macro-operations are either on a sequential (SEQ) or on a one-shot (OSH) access basis. Two sequential access options allow the MCU to either read from or write into the bidirectional shift register(s) of the segment driver(s) within a specified window boundary and at various pitch widths sequentially. For instance, a sequential-write at a 10-bit pitch width allows the MCU to write into the serial stream a 10-bit word at a time which is then shifted serially into the segment drivers. The transfer is automatically carried out as soon as a 10-bit word has been written into a register of the LCD Control Unit. After the transfer, the interface will stop for the next 10-bit word from the processor. This transfer-and-wait process is repeated within a window which is specified by the left and right pointers of the LCD Control Unit. These two pointers can be flexibly adjusted to fit in window of any size. The width can be as wide as the whole screen or just a pixel. For data outside this window, the interface will carry out a non-stop shift until the specified end-point. With this interface a row of display data can then be composed in the bidirectional shift register loop before the MCU orders the segment drivers to copy this row of data into their internal Static RAM in a parallel fashion. The MCU does it by issuing a command, encrypted with a row address, to the segment drivers through the parallel interface. It is a typical cycle that a row of display data is loaded into the bidirectional shift register and written back to the same row after it has been edited by the processor. This cycle can be viewed as accessing some part of the screen in rectangular coordinates - the row address as the Y-coordinate and the location pointed by one of the two pointers as the X-coordinate, particularly if the macro-operation "One-Shot Replace" is used. "One-Shot Replace" will replace a number of dots as specified by the variable pitch register after the first pointer with the new content prepared by the MCU. The transfer is one-shot and the loop will stop only after it has reverted back to its original position. Such an LCD system allows for a natural way of manipulating graphics on the LCD panel via a rectangular coordinating system. Unlike some conventional LCD systems which coordinations are somehow tied with the 8-bit RAM structure, it eases much effort when only a bit of content needs to be changed, which is most often the case in handwriting applications.

The Handwriting Input Mechanism

An input device for handwriting is a touch sensitive panel. It is transparent and can be laid on top of the LCD panel. With the appropriate setup, the points of touch can be located by an A/D converter (MC1415150). Detected points expressed in rectangular coordinates are brought to the processor for scaling and transformation and put on the LCD. If the sampling is fast enough, one would see a continuous trace on the LCD screen recording the movement of the touch.

This panel is a passive device and it needs both a hardware and a software driver for handwriting purpose. Figure 4 shows the hardware driver of the touch sensitive panel system. The panel shown is coupled to a transistor ladder which is responsible for configuring the circuit for different sampling set-ups. The ladder circuit is controlled by I/O port C. After the establishment of the right circuit configuration, the MCU through the Serial Peripheral Interface commands the A/D converter to translate an analog voltage into a digital numeric.

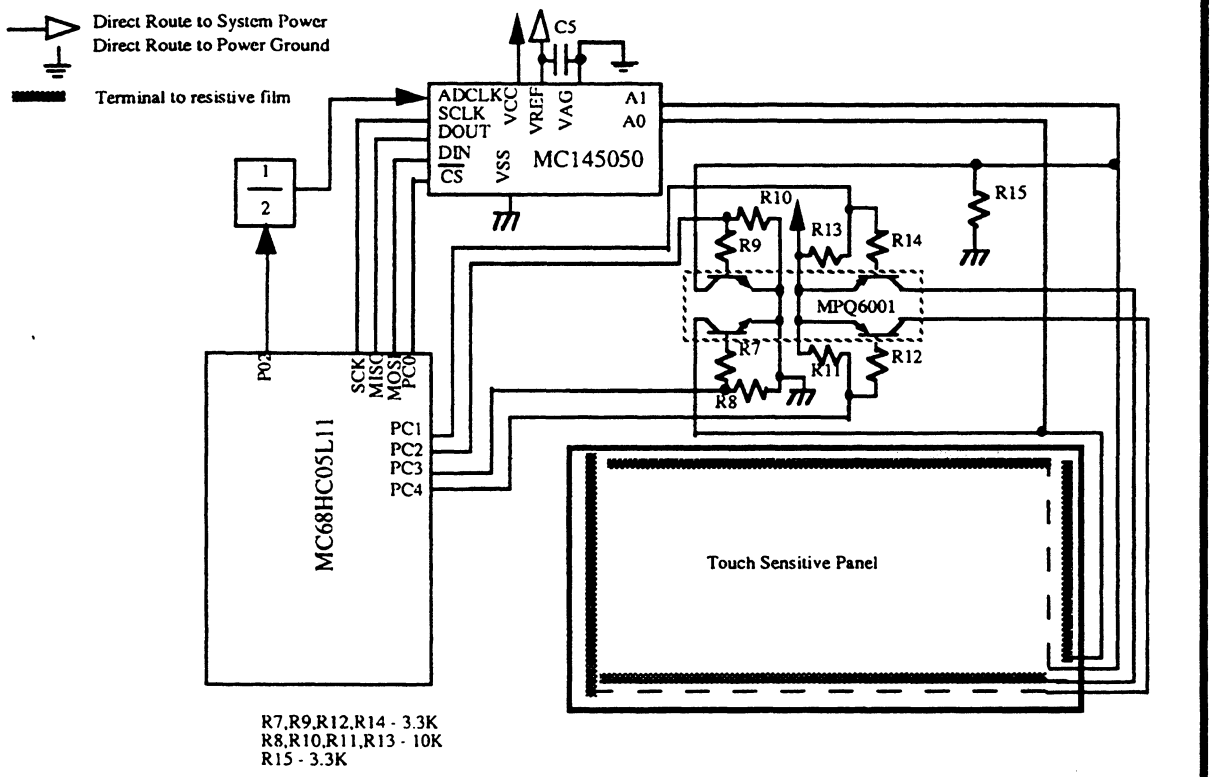

Figure 4. The Hardware Support Of The Touch Sensitive Panel

The touch sensitive panel has two layers of transparent, evenly doped resistive film sandwiching a thin spacer and mounted on a supporting glass. There are four terminals located along the four edges of the panel. A pair of terminals connects to opposite sides the upper film (e.g. in the horizontal direction) while another pair connects similarly to the lower film (e.g. in the vertical direction). Separated by a thin spacer, these films are electrically isolated from each other in the idle state. However, if a pressure is applied with a sharp pen, the stylus will push the upper film down to make contact with the lower film. Also, if a reference voltage is applied across the terminals of the upper film while the other pair remains in high impedance, the voltage should drop linearly across the upper film in vertical direction. The point of contact of the two films transforms the terminals of the lower film to become the wiper of a potentiometer. Because the resistance across the layer is uniform, the voltage at the contact point should be proportional to its distance from the ground-referenced edge. As a result, the voltage at either terminal of the lower film carries information about the Y coordinate of the stylus. The same procedure can be applied to measure the X coordinate of the stylus by role-swapping the two pairs of terminals. The mechanism is simple and its accuracy depends on the linearity of the resistive film and the resolution of the A/D converter. However, there is another problem. Like most mechanical devices (e.g. a keyboard), the touch sensitive panel suffers from contact bounce. To verify good contact closure, the system has to switch one pair of terminals to the reference voltage source and then connect one of the terminals of the other pair to a high value pull-down resistor (but not too high in order to overcome the capacitive effect across the films). A good contact is ensured if the voltage across this resistor is greater than a threshold. In Figure 5, the software checks for a good contact before sampling the X and Y coordinates. However, the process is not ended until a reconfirmation for a good contact is done after polling in X and Y because of the fact that a good contact might be lost during sampling for X and Y. Valid samples will be further processed and then sent to the LCD system for output.

A PROTOTYPE FOR HAND-WRITING APPLICATION

It is relatively straight-forward to implement handwriting input in a DragonKat II- based system. Figure 5 shows the circuit diagram of such a system. It is just the combination of the Figure 1 and 3 with the touch sensi-

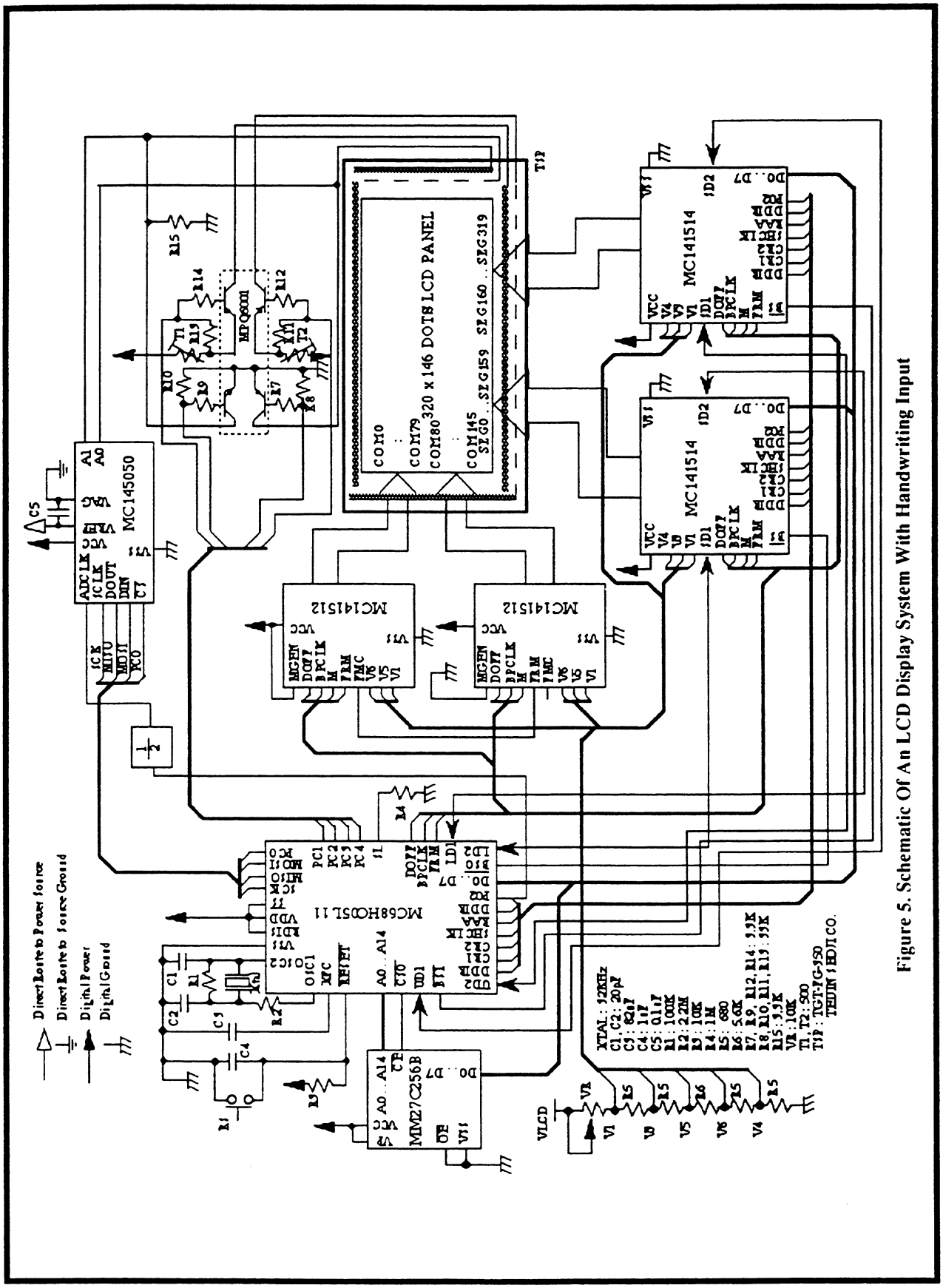

Figure 5. Schematic Of An LCD Display System With Handwriting Input

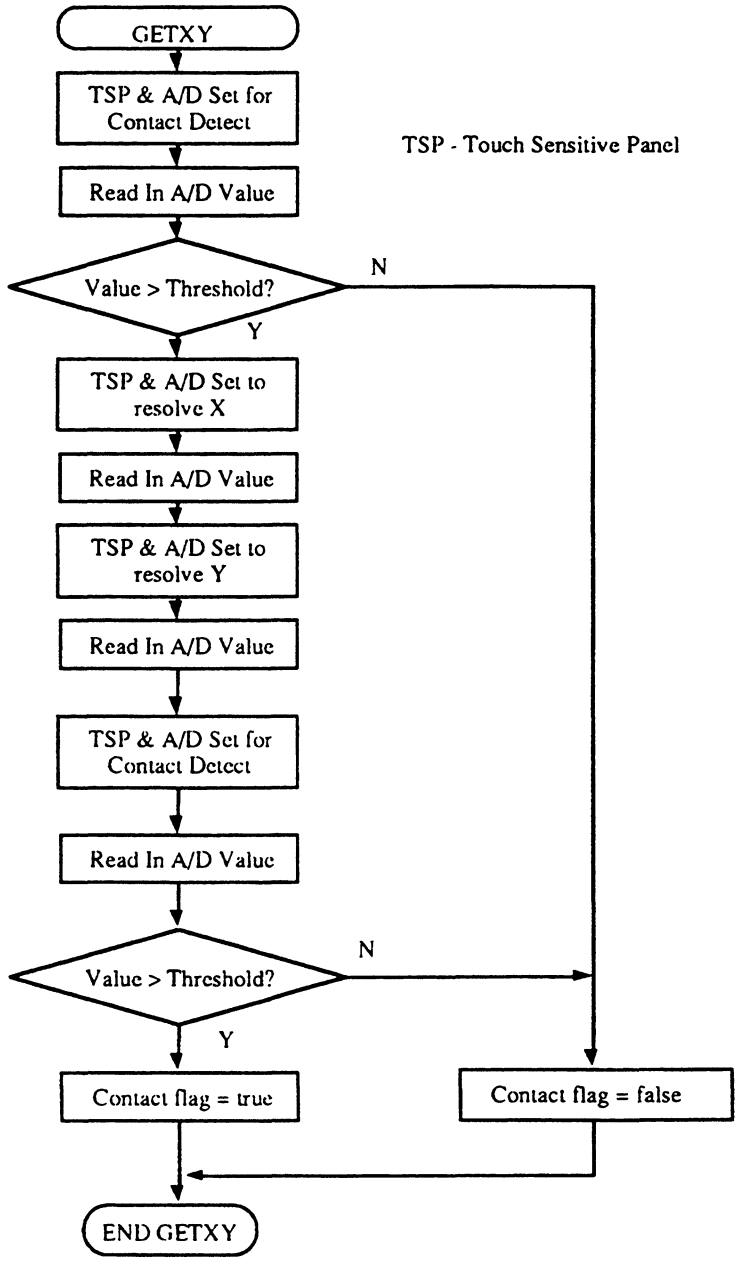

Figure 6. The Software Driver For The Touch Sensitive Panel System

tive tablet overlaid on the top of the LCD panel. The MCU samples the touch sensitive tablet for handwriting input. If a valid contact is found, after a sample conversion, the dot can be transferred to the LCD system for display. Furthermore, the user can intercept the software flow for different intepretations on the pen-based inputs in applications such as straight-lines drawing, polygon building and even pattern hatching. The large effective area of the tablet allows icons to be displayed for pen selections. A touch-and-execute procedure makes the system very user-friendly and obviates the need for an elaborate keyboard in a pocket equipment.

SOFTWARE OF THE PROTOTYPE

Figure 7 shows the flow chart of a sample program which emulates a blank paper and an eraser. The system routine DRAWRUB starts up to do hand-writing with its Eraser Flag disabled. It will first clean the screen and pops up an Eraser Icon at the upper righthand corner of the screen. It then enables a 16-bit timer interrupt before it goes to WAIT[4]. The Timer will then periodically call up the processor to scan for user inputs. The main part

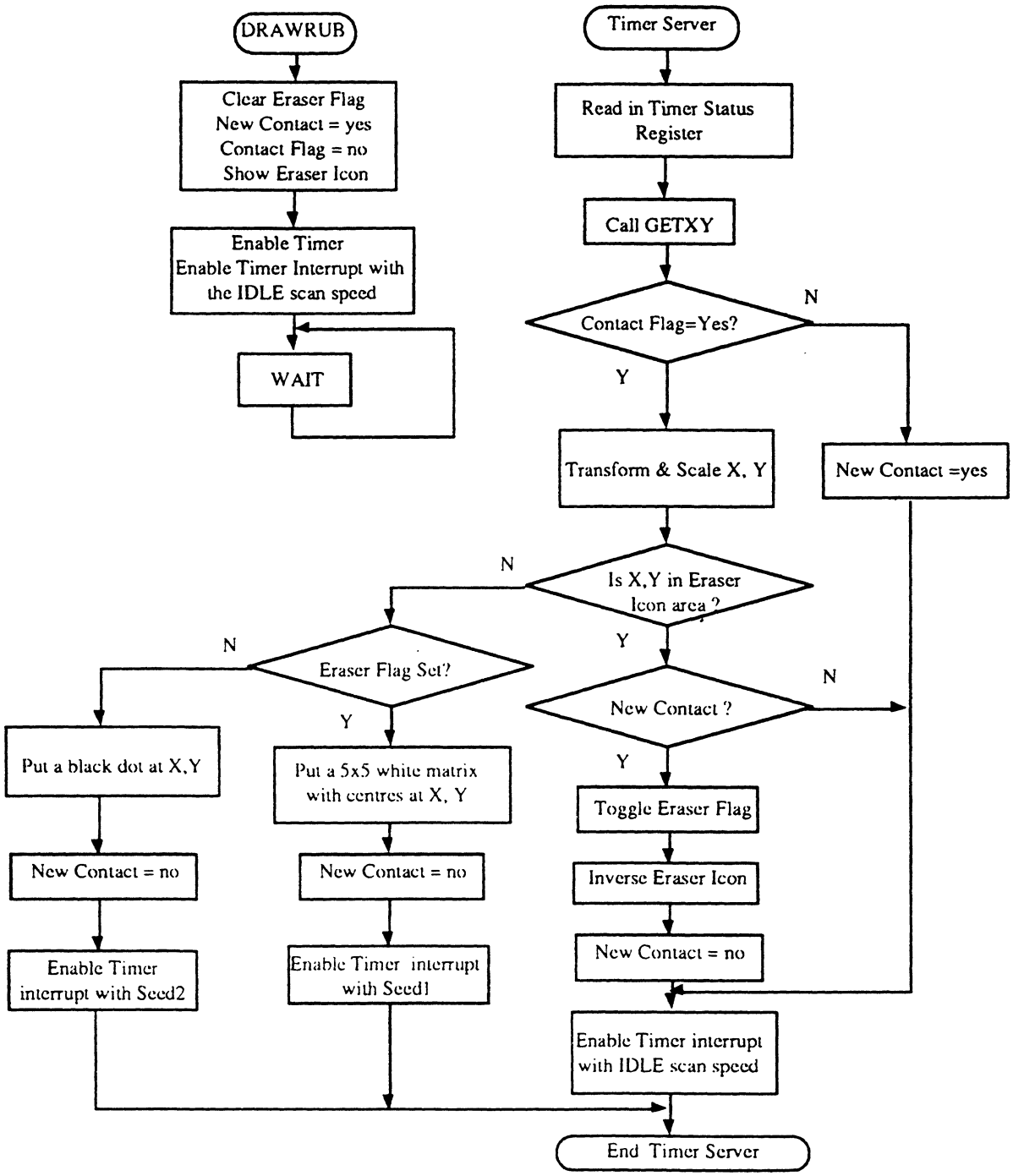

Figure 7. The Software For Electronic Handwriting And Erasing

of the scan-and-print job is resident in the Timer Server routine. The Timer Server is the routine to where the processor will branch as soon as it is waken up by a timer interrupt. It will first access the timer status register. The Timer Output Compare flag will be cleared as it writes a next interrupt count into the Output Compare Register. Otherwise the same interrupt request may keep on interrupting the processor as soon as it is out of the Timer Server. Then the MCU branches to scan for contact closures. It simply calls the routine GETXY as shown as Figure 6. Out of GETXY, the processor examines the Contact Flag. If a good contact is found, the processor resolves the X,Y coordinates on the LCD panel and then checks if the stylus is pointing to the area within the Eraser Icon. If so, it further examines the New Contact flag to determine whether it is a fresh

[4] A power saving mode of MC68HC05.

touch. Only a fresh touch can trigger the Eraser Icon. This trigger will cause the processer to inverse the Eraser Icon and toggle the Eraser Flag. However if the coordinates are out of Eraser Icon, the routine will either carry out the erasing routine or the writing routine depending on the Eraser Flag. The writing routine is listed in Figure 6 which just puts a black dot at the X,Y location while the erasing routine will clean up a square of an effective area around to the stylus. Both routines end with Enabling the Timer with different speed settings for the fact that writing and erasing might have different repetitive rates. Also if no good contact is found, the Timer Server will be exited with the New Contact flag asserted and the timer interrupt is enabled with the IDLE speed set. As a result, the system may have different scan rates for erasing, for writing and for idle scanning. On exiting the Server, the processor loops back to WAIT and repeats the same procedure. The attached appendix lists the source code for the software and it starts up with the screen as shown in Figure 8. A 16x16 eraser icon is located at the upper right hand corner of the LCD panel.

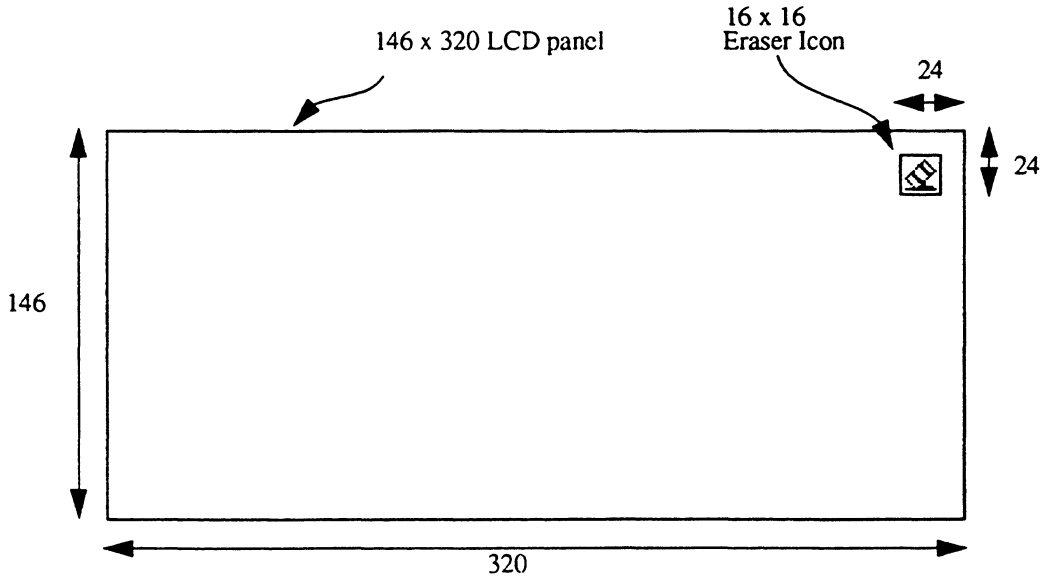

Figure 8. The Start Up Screen Of The Demonstration Software

APPENDIX : THE LISTING OF THE DEMONSTRATION SOFTWARE

```
                    ****************** LCD CONTROL REGISTER ********************
0028                    MODE    EQU     $28     MODE AND ATTRIBUTE REGISTER
0000                    SEQ     EQU     0
0001                    OSH     EQU     1
0002                    S0      EQU     2
0003                    S1      EQU     3
0004                    INVA    EQU     4
0005                    INVB    EQU     5
0006                    MOD     EQU     6
0007                    RSW     EQU     7       REGISTER SWITCH

0029                    LFTPTR  EQU     $29     LEFT POINTER
002B                    RGTPTR  EQU     $2B     RIGHT POINTER
002D                    SHTREG  EQU     $2D     SHIFT REGISTER
002D                    LOOP    EQU     $2D     LOOP SIZE REGISTER
002F                    HP      EQU     $2F     HORIZONTAL PITCH REGISTER

0030                    STATUS  EQU     $30     STATUS REGISTER AND ITS BITS
DEFINITION
0000                    RDY     EQU     0
0001                    ACT     EQU     1
0002                    HPOF    EQU     2
0003                    RGST    EQU     3

0030                    PSCALAR EQU     $30     PRESCALAR REGISTER FOR MUX
RATIO SELECTION
0031                    SEGMENT EQU     $31     SEGMENT CONTROL REGISTER

0032                    LCDMREG EQU     $32     LCD MODE REGISTER AND ITS BITS
DEFINITION
0000                    DON     EQU     0
0001                    CR1     EQU     1
0002                    CR2     EQU     2
0003                    DDIR    EQU     3
0004                    BS0     EQU     4
0005                    BS1     EQU     5
0006                    DPAN    EQU     6
0007                    MSW     EQU     7

                    ****************** SYSTEM CLOCK REGISTERS ******************
0021                    CTL21   EQU     $21     CONTROL REGISTER $21
0004                    PLLI    EQU     4
0005                    FS0     EQU     5
0006                    FS1     EQU     6

0025                    CTL25   EQU     $25     CONTROL REGISTER $25
0000                    CLKS    EQU     0
0003                    PORTI   EQU     3
0007                    TIMI    EQU     7

                    ****************** TIMER REGISTERS *************************
0012                    TCR     EQU     $12     TIMER CONTROL REGISTER
0000                    OLVL1   EQU     0
0001                    IEDG    EQU     1
0002                    OLVL2   EQU     2
0004                    OCIE2   EQU     4
0005                    TOIE    EQU     5
0006                    OCIE1   EQU     6
0007                    ICIE    EQU     7

0013                    TSR     EQU     $13     TIMER STATUS REGISTER
0004                    OCF2    EQU     4
```

```
0005                    TOF     EQU     5
0006                    OCF1    EQU     6
0007                    ICF     EQU     7

0016                    OUTCMP1 EQU     $16     TIMER OUTPUT COMPARE1 REGISTER

0018                    TIMER   EQU     $18     TIMER COUNT REGISTER

001A                    ATIMER  EQU     $1A     ALTERNATE COUNT REGISTER

001C                    OUTCMP2 EQU     $1C     TIMER OUTPUT COMPARE2 REGISTER

                    ****************** SPI REGISTERS ****************************
0022                    SPCR    EQU     $22     SPI CONTROL REGISTER
0000                    SPR0    EQU     0
0001                    SPR1    EQU     1
0002                    CPHA    EQU     2
0003                    CPOL    EQU     3
0004                    MSTR    EQU     4
0006                    SPE     EQU     6
0007                    SPIE    EQU     7

0023                    SPSR    EQU     $23     SPI STATUS REGISTER
0004                    MODF    EQU     4
0006                    WCOL    EQU     6
0007                    SPIF    EQU     7

0024                    SPDR    EQU     $24     SPI DATA I/O REGISTER

                    ****************** CONTROL PORTS ****************************
0008                    PORTCDR EQU     $08     PORTC DATA DIRECTION REGISTER
0002                    PORTC   EQU     $02     PORTC DATA REGISTER
0000                    ADSEL_  EQU     0       SELECT A TO D CONVERTER
0001                    UPVREF_ EQU     1       DISCONNECT/CONNECT THE VREF
FOR UPPER FILM
0002                    UPGND   EQU     2       CONNECT/DISCONNECT THE GND FOR
UPPER FILM
0004                    LWVREF_ EQU     4       DISCONNECT/CONNECT THE VREF
FOR LOW FILM
0003                    LWGND   EQU     3       CONNECT/DISCONNECT THE GND FOR
LOW FILM

                    ****************** CONSTANTS ********************************
0028                    SEED1H  EQU     $28
0000                    SEED1L  EQU     $00
001F                    SEED2H  EQU     $1F
0000                    SEED2L  EQU     $00
00FF                    IDLEH   EQU     $FF
0000                    IDLEL   EQU     $00
00C0                    TRIGGERH EQU    $C0
0000                    TRIGGERL EQU $00
0001                    WICONX1H EQU$01
0028                    WICONX1L EQU$28
0001                    WICONX2H EQU$01
0037                    WICONX2L EQU$37
0008                    WICONY1 EQU     $8
0017                    WICONY2 EQU     $17
0000                    LFTBDH  EQU$00
0060                    LFTBDL  EQU     $60
0000                    TOPBDH  EQU     $00
0090                    TOPBDL  EQU     $90

0001                    FLLOOPH EQU     $1
003F                    FLLOOPL EQU     $3F
009F                    HFLOOP  EQU     $9F
0091                    SCNHGT  EQU     145
```

```
                    ****************** VARIABLES AND FLAGS ********************
0050                    TSPFLGS EQU     $50
0000                    CONTACT EQU     0       GOOD/BAD CONTACT - CONTACT FLAG
0001                    NEWCONT EQU     1       NEW/OLD CONTACT - NEW CONTACT
FLAG
0002                    ERASER  EQU     2       ON/OFF ERASER - ERASER FLAG

0052                    X       EQU     $52     STORAGE OF X COORDINATE
0054                    Y       EQU     $54     STORAGE OF Y COORDINATE
0056                    YD      EQU     $56     DUMMY VARIABLE
0057                    FN      EQU     $57     FOR LONG OPERATIONS
0059                    SN      EQU     $59     FOR LONG OPERATIONS

0200                            ORG     $200
                    ****************** DRAWRUB **********************************
0200 10 25              DRAWRUB BSET    CLKS,CTL25      SELECT PLL CLOCK
0202 1B 21                      BCLR    FS0,CTL21       SET SYSTEM CLOCK TO
2.44MHZ
0204 1C 21                      BSET    FS1,CTL21
0206 08 21 FD                   BRSET   PLLI,CTL21,*
0209 09 21 FD                   BRCLR   PLLI,CTL21,*    WAIT FOR PLL STABLE

                    ***************** SET UP CONTROL PORTS **********************
020C 10 08                      BSET    ADSEL_,PORTCDR
020E 12 08                      BSET    UPVREF_,PORTCDR
0210 14 08                      BSET    UPGND,PORTCDR
0212 18 08                      BSET    LWVREF_,PORTCDR
0214 16 08                      BSET    LWGND,PORTCDR
0216 10 02                      BSET    ADSEL_,PORTC

                        * SET TRANSISTORS LADDER TO IDLE *
0218 12 02                      BSET    UPVREF_,PORTC
021A 15 02                      BCLR    UPGND,PORTC
021C 18 02                      BSET    LWVREF_,PORTC
021E 17 02                      BCLR    LWGND,PORTC

                        * SET UP LCD SYSTEM *
0220 1E 32                      BSET    MSW,LCDMREG
0222 A6 91                      LDA     #SCNHGT
0224 B7 31                      STA     SEGMENT
0226 A6 20                      LDA     #$20
0228 B7 30                      STA     PSCALAR
022A 1F 32                      BCLR    MSW,LCDMREG
022C 10 32                      BSET    DON,LCDMREG
022E 12 32                      BSET    CR1,LCDMREG
0230 14 32                      BSET    CR2,LCDMREG
0232 18 32                      BSET    BS0,LCDMREG
0234 1A 32                      BSET    BS1,LCDMREG
0236 1C 32                      BSET    DPAN,LCDMREG
0238 A6 04                      LDA     #%00000100
023A B7 31                      STA     SEGMENT
023C 13 32                      BCLR    CR1,LCDMREG
023E 15 32                      BCLR    CR2,LCDMREG
0240 A6 92                      LDA     #SCNHGT+1
0242 4A                 CLRROW  DECA
0243 B7 31                      STA     SEGMENT
0245 26 FB                      BNE     CLRROW
0247 3F 29                      CLR     LFTPTR
0249 3F 2A                      CLR     LFTPTR+1

024B 3F 50                      CLR     TSPFLGS         CLEAR ALL FLAGS
024D 12 50                      BSET    NEWCONT,TSPFLGS NEXT CONTACT IS NEW
024F CD 05 3A                   JSR     PUTICON

                        * CHECK A/D CIRCUIT *
0252 1C 22                      BSET    SPE,SPCR
```

```
0254 11 02              A_DCHK  BCLR    ADSEL_,PORTC
0256 A6 B0                      LDA     #$B0
0258 B7 24                      STA     SPDR
025A 0F 23 FD                   BRCLR   SPIF,SPSR,*
025D B6 24                      LDA     SPDR
025F B7 57                      STA     FN
0261 3F 24                      CLR     SPDR
0263 0F 23 FD                   BRCLR   SPIF,SPSR,*
0266 10 02                      BSET    ADSEL_,PORTC
0268 B6 24                      LDA     SPDR
026A B7 58                      STA     FN+1
026C A6 80                      LDA     #$80
026E B7 59                      STA     SN
0270 4F                         CLRA
0271 B7 5A                      STA     SN+1
0273 CD 02 B0                   JSR     LONGCMP
0276 27 07                      BEQ     A_DOK
0278 A6 20                      LDA     #$20
027A 4A                 A_DWAIT DECA
027B 26 FD                      BNE     A_DWAIT
027D 20 D5                      BRA     A_DCHK
                        A_DOK

                        * ENABLE TIMER INTERRUPT *

027F 16 25                      BSET    PORTI,CTL25     ENABLING TIMER
0281 B6 18                      LDA     TIMER
0283 B7 57                      STA     FN
0285 B6 19                      LDA     TIMER+1
0287 B7 58                      STA     FN+1
0289 A6 FF                      LDA     #IDLEH
028B B7 59                      STA     SN
028D A6 00                      LDA     #IDLEL
028F B7 5A                      STA     SN+1
0291 CD 02 A3                   JSR     LONGADD
0294 B6 13                      LDA     TSR     CLEAR OCF2 FOR SYSTEM SECURITY
0296 B6 57                      LDA     FN
0298 B7 16                      STA     OUTCMP1
029A B6 58                      LDA     FN+1
029C B7 17                      STA     OUTCMP1+1
029E 1C 12                      BSET    OCIE1,TCR       ENABLING OUTPUT
COMPARE1 INTERRUPT

                        * ENTER WAIT *
02A0 8F                 TOWAIT  WAIT
02A1 20 FD                      BRA     TOWAIT
                  ********** END OF DRAWRUB **************************

                  ********** LONG CALCULATIONS SUBROUTINES ************
                  ****************************************************
                        *       LONGADD - DOUBLE BYTE ADDITION
                        *               FN:FN+1 = MSB,LSB OF THE FISRT NUMBER
                        *               SN:SN+1 = MSB,LSB OF THE SECOND NUMBER
                        *       FORMULA FN = FN + SN
                  ****************************************************

02A3 B6 58              LONGADD LDA     FN+1
02A5 BB 5A                      ADD     SN+1
02A7 B7 58                      STA     FN+1
02A9 B6 57                      LDA     FN
02AB B9 59                      ADC     SN
02AD B7 57                      STA     FN
02AF 81                         RTS


                  ****************************************************
                    *       LONGCMP - COMPARE TWO UNSIGNED DOUBLE BYTE NUMBERS
```

```
                    *               FN:FN+1 = MSB,LSB OF FIRST NUMBER
                    *               SN:SN+1 = MSB,LSB OF SECOND NUMBER
                    ************************************************************

02B0 B6 57          LONGCMP LDA     FN
02B2 B1 59                  CMP     SN
02B4 26 04                  BNE     LCMPQT
02B6 B6 58                  LDA     FN+1
02B8 B1 5A                  CMP     SN+1
02BA 81             LCMPQT  RTS

                    ************************************************************
                    *       LONGSUB - DOUBLE BYTE SUBTRACTION
                    *               FN:FN+1 = MSB,LSB OF THE FIRST NUMBER
                    *               SN:SN+1 = MSB,LSB OF THE SECOND NUMBER
                    *       FORMULA FN = FN - SN
                    ************************************************************

02BB B6 58          LONGSUB LDA     FN+1
02BD B0 5A                  SUB     SN+1
02BF B7 58                  STA     FN+1
02C1 B6 57                  LDA     FN
02C3 B2 59                  SBC     SN
02C5 B7 57                  STA     FN
02C7 81                     RTS
                     ****************** END OF CALCULATIONS SUBROUTINES *********

                    ****************** TIMERSERVER *******************************
                    TIMERSERVER
02C8 B6 13                  LDA     TSR     NEXT ACCESS TO OUTCMP1 WILL
CLEAR FLAG
02CA CD 04 2C               JSR     GETXY
02CD 00 50 04               BRSET   CONTACT,TSPFLGS,GOODCONTACTIF GOOD
CONTACT
02D0 12 50                  BSET    NEWCONT,TSPFLGS         NEXT CONTACT
IS NEW
02D2 20 65                  BRA     IDLING
                    GOODCONTACT
02D4 34 52                  LSR     X
02D6 36 53                  ROR     X+1
02D8 B6 53                  LDA     X+1
02DA B7 58                  STA     FN+1
02DC B6 52                  LDA     X
02DE B7 57                  STA     FN

02E0 A6 00                  LDA     #LFTBDH
02E2 B7 59                  STA     SN
02E4 A6 60                  LDA     #LFTBDL
02E6 B7 5A                  STA     SN+1
02E8 CD 02 BB               JSR     LONGSUB
02EB 25 3D                  BCS     SETRATE
                    INLFTBOUND
02ED A6 01                  LDA     #FLLOOPH
02EF B7 59                  STA     SN
02F1 A6 3F                  LDA     #FLLOOPL
02F3 B7 5A                  STA     SN+1
02F5 CD 02 B0               JSR     LONGCMP
02F8 22 30                  BHI     SETRATE

                    INRGTBOUND
02FA B6 57                  LDA     FN
02FC B7 52                  STA     X
02FE B6 58                  LDA     FN+1
0300 B7 53                  STA     X+1

0302 34 54                  LSR     Y
0304 36 55                  ROR     Y+1
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0306 34 54                      LSR     Y
0308 36 55                      ROR     Y+1
030A B6 54                      LDA     Y
030C B7 57                      STA     FN
030E B6 55                      LDA     Y+1
0310 B7 58                      STA     FN+1
0312 A6 00                      LDA     #TOPBDH
0314 B7 59                      STA     SN
0316 A6 90                      LDA     #TOPBDL
0318 B7 5A                      STA     SN+1
031A CD 02 BB                   JSR     LONGSUB
031D 25 0B                      BCS     SETRATE

031F 3F 59                      CLR     SN
0321 A6 91                      LDA     #SCNHGT
0323 B7 5A                      STA     SN+1
0325 CD 02 B0                   JSR     LONGCMP
0328 23 15                      BLS     PASS2

                        SETRATE
032A 04 50 06                   BRSET   ERASER,TSPFLGS,SETRATE1
032D A6 1F                      LDA     #SEED2H
032F AE 00                      LDX     #SEED2L
0331 20 41                      BRA     GENRATE
                        SETRATE1
0333 A6 28                      LDA     #SEED1H
0335 AE 00                      LDX     #SEED1L
0337 20 3B                      BRA     GENRATE
                        IDLING
0339 A6 00                      LDA     #IDLEL
033B AE FF                      LDX     #IDLEH
033D 20 35                      BRA     GENRATE
                        PASS2
033F B6 58                      LDA     FN+1
0341 B7 54                      STA     Y               Y BECOMES ONE BYTE
VARIABLE NOW

                        * CHECK X,Y IN ERASER ICON *
0343 B6 54                      LDA     Y
0345 A1 08                      CMP     #WICONY1
0347 25 4E                      BLO     NOTICON
0349 A1 17                      CMP     #WICONY2
034B 22 4A                      BHI     NOTICON
034D B6 52                      LDA     X
034F B7 57                      STA     FN
0351 B6 53                      LDA     X+1
0353 B7 58                      STA     FN+1
0355 A6 28                      LDA     #WICONX1L
0357 B7 59                      STA     SN
0359 A6 01                      LDA     #WICONX1H
035B B7 5A                      STA     SN+1
035D CD 02 B0                   JSR     LONGCMP
0360 25 35                      BLO     NOTICON
0362 A6 37                      LDA     #WICONX2L
0364 B7 59                      STA     SN
0366 A6 01                      LDA     #WICONX2H
0368 B7 5A                      STA     SN+1
036A CD 02 B0                   JSR     LONGCMP
036D 22 28                      BHI     NOTICON
036F 02 50 1A                   BRSET   NEWCONT,TSPFLGS,ICON
0372 20 C5                      BRA     IDLING
                        GENRATE
0374 B7 59                      STA     SN
0376 BF 5A                      STX     SN+1
0378 B6 18                      LDA     TIMER
037A B7 57                      STA     FN
037C B6 19                      LDA     TIMER+1
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037E B7 58                      STA     FN+1
0380 CD 02 A3                   JSR     LONGADD
0383 B6 57                      LDA     FN
0385 B7 16                      STA     OUTCMP1
0387 B6 58                      LDA     FN+1
0389 B7 17                      STA     OUTCMP1+1
038B 80                         RTI

038C A6 04              ICON    LDA#$04
038E B8 50                      EOR     TSPFLGS         TOGGLING ERASER FLAG
0390 CD 05 03                   JSR     INVERSE
0393 13 50                      BCLR    NEWCONT,TSPFLGS
0395 20 A2                      BRA     IDLING

                        NOTICON
0397 04 50 4F                   BRSET   ERASER,TSPFLGS,DOERASE
039A B6 52                      LDA     X
039C B7 57                      STA     FN
039E B6 53                      LDA     X+1
03A0 B7 58                      STA     FN+1
03A2 A6 9F                      LDA     #HFLOOP
03A4 B7 5A                      STA     SN+1
03A6 3F 59                      CLR     SN
03A8 CD 02 BB                   JSR     LONGSUB
03AB 25 06                      BCS     RGTHFSCREEN
03AD 19 32                      BCLR    BS0,LCDMREG
03AF 1A 32                      BSET    BS1,LCDMREG
03B1 20 04                      BRA     PUTDOT

                        RGTHFSCREEN
03B3 18 32                      BSET    BS0,LCDMREG
03B5 1B 32                      BCLR    BS1,LCDMREG
                        PUTDOT
03B7 B6 57                      LDA     FN
03B9 B7 2B                      STA     RGTPTR
03BB B6 58                      LDA     FN+1
03BD B7 2C                      STA     RGTPTR+1
03BF 12 32                      BSET    CR1,LCDMREG
03C1 15 32                      BCLR    CR2,LCDMREG
03C3 B6 54                      LDA     Y
03C5 B7 31                      STA     SEGMENT
03C7 1E 28                      BSET    RSW,MODE
03C9 3F 2E                      CLR     LOOP+1
03CB A6 9F                      LDA     #HFLOOP
03CD B7 2D                      STA     LOOP
03CF 1F 28                      BCLR    RSW,MODE
03D1 A6 01                      LDA     #$01
03D3 B7 2E                      STA     SHTREG+1
03D5 3F 2F                      CLR     HP
03D7 A6 42                      LDA     #%01000010
03D9 B7 28                      STA     MODE
03DB 06 30 FD                   BRSET   RGST,STATUS,*
03DE 12 32                      BSET    CR1,LCDMREG
03E0 B6 54                      LDA     Y
03E2 B7 31                      STA     SEGMENT
03E4 13 50                      BCLR    NEWCONT,TSPFLGS
03E6 CC 03 2A                   JMP     SETRATE

                        DOERASE
03E9 1A 32                      BSET    BS1,LCDMREG
03EB 18 32                      BSET    BS0,LCDMREG
03ED A6 05                      LDA     #5
03EF B7 56                      STA     YD
03F1 B6 52                      LDA     X
03F3 B7 2B                      STA     RGTPTR
03F5 B6 53                      LDA     X+1
03F7 B7 2C                      STA     RGTPTR+1
```

```
03F9 1E 28                      BSET    RSW,MODE
03FB A6 01                      LDA     #FLLOOPH
03FD B7 2D                      STA     LOOP
03FF A6 3F                      LDA     #FLLOOPL
0401 B7 2E                      STA     LOOP+1
0403 1F 28                      BCLR    RSW,MODE
0405 A6 04                      LDA     #4
0407 B7 2F                      STA     HP
0409 15 32                      BCLR    CR2,LCDMREG
040B B6 54                      LDA     Y
                        REDO
040D 12 32                      BSET    CR1,LCDMREG
040F B7 31                      STA     SEGMENT
0411 3F 2E                      CLR     SHTREG+1
0413 AE 42                      LDX     #%01000010
0415 BF 28                      STX     MODE

0417 06 30 FD                   BRSET   RGST,STATUS,*
041A 13 32                      BCLR    CR1,LCDMREG
041C B7 31                      STA     SEGMENT
041E 4C                         INCA
041F A1 91                      CMP     #SCNHGT
0421 22 04                      BHI     EQUIP
0423 3A 56                      DEC     YD
0425 26 E6                      BNE     REDO
                        EQUIP
0427 13 50                      BCLR    NEWCONT,TSPFLGS
0429 CC 03 2A                   JMP     SETRATE


                    ****************** GETXY ************************************
042C 18 02              GETXY   BSET    LWVREF_,PORTC   NOW THE LOWER FILM IS
ENERGIZED
                        * CONTACT DETECTION *
042E 11 02                      BCLR    ADSEL_,PORTC
0430 A6 10                      LDA     #$10            CONTACT DETECTION
0432 B7 24                      STA     SPDR
0434 0F 23 FD                   BRCLR   SPIF,SPSR,*
0437 3F 24                      CLR     SPDR
0439 0F 23 FD                   BRCLR   SPIF,SPSR,*
043C 10 02                      BSET    ADSEL_,PORTC
043E 18 02                      BSET    LWVREF_,PORTC
0440 A6 0A                      LDA     #10     A TO D NEEDS >=88 CYCLES FOR
CONVERSION
                        CYCLES88
0442 4A                         DECA
0443 26 FD                      BNE     CYCLES88

                        * GET CONTACT AND COMMAND FOR CONVERTING X *
0445 19 02                      BCLR    LWVREF_,PORTC
0447 16 02                      BSET    LWGND,PORTC
0449 11 02                      BCLR    ADSEL_,PORTC
044B A6 10                      LDA     #$10    GET CONTACT LEVEL
044D B7 24                      STA     SPDR
044F 0F 23 FD                   BRCLR   SPIF,SPSR,*
0452 B6 24                      LDA     SPDR
0454 B7 57                      STA     FN
0456 3F 24                      CLR     SPDR
0458 0F 23 FD                   BRCLR   SPIF,SPSR,*
045B B6 24                      LDA     SPDR
045D B7 58                      STA     FN+1
045F 10 02                      BSET    ADSEL_,PORTC
0461 18 02                      BSET    LWVREF_,PORTC
0463 17 02                      BCLR    LWGND,PORTC
                        * CHECK CONTACT LEVEL IN FN IS LARGER THAN TRIGGER *
0465 A6 C0                      LDA     #TRIGGERH       PROCESS TAKES 35
CYCLES
```

```
0467 B7 59                      STA     SN
0469 A6 00                      LDA     #TRIGGERL
046B B7 5A                      STA     SN+1
046D CD 02 B0                   JSR     LONGCMP
0470 24 03                      BHS     PASSCONT1
                        FAILEXIT
0472 11 50                      BCLR    CONTACT,TSPFLGS
0474 81                         RTS
                        PASSCONT1
                        * NEEDS EXTRA 53 CYCLES
0475 A6 09                      LDA     #$9
0477 4A                 CYC53   DECA
0478 26 FD                      BNE     CYC53

                        * GET X AND COMMAND FOR CONVERTING Y *
047A 13 02                      BCLR    UPVREF_,PORTC
047C 14 02                      BSET    UPGND,PORTC
047E 11 02                      BCLR    ADSEL_,PORTC
0480 A6 00                      LDA     #$00            GET X, CONVERTING Y
0482 B7 24                      STA     SPDR
0484 0F 23 FD                   BRCLR   SPIF,SPSR,*
0487 B6 24                      LDA     SPDR
0489 B7 53                      STA     X+1
048B 3F 24                      CLR     SPDR
048D 0F 23 FD                   BRCLR   SPIF,SPSR,*
0490 B6 24                      LDA     SPDR
0492 A4 C0                      AND     #$C0
0494 B7 52                      STA     X
0496 10 02                      BSET    ADSEL_,PORTC
0498 12 02                      BSET    UPVREF_,PORTC
049A 15 02                      BCLR    UPGND,PORTC
049C 38 52                      LSL     X               PROCESS TAKES 25 CYCLES
049E 39 53                      ROL     X+1
04A0 39 52                      ROL     X
04A2 39 53                      ROL     X+1
04A4 39 52                      ROL     X
                        * A TO D NEEDS EXTRA 63 CYCLES
04A6 A6 0A                      LDA     #$A             A TO D NEEDS >=88
CYCLES FOR CONVERSION
                        CYCLES63
04A8 4A                         DECA
04A9 26 FD                      BNE     CYCLES63
                        * GET Y AND COMMAND FOR ANOTHER CONTACT *
04AB 19 02                      BCLR    LWVREF_,PORTC
04AD 11 02                      BCLR    ADSEL_,PORTC
04AF A6 10                      LDA     #$10            GET Y
04B1 B7 24                      STA     SPDR
04B3 0F 23 FD                   BRCLR   SPIF,SPSR,*
04B6 B6 24                      LDA     SPDR
04B8 B7 55                      STA     Y+1
04BA 3F 24                      CLR     SPDR
04BC 0F 23 FD                   BRCLR   SPIF,SPSR,*
04BF B6 24                      LDA     SPDR
04C1 A4 C0                      AND     #$C0
04C3 B7 54                      STA     Y
04C5 10 02                      BSET    ADSEL_,PORTC
04C7 18 02                      BSET    LWVREF_,PORTC
04C9 38 54                      LSL     Y               PROCESS TAKES 25
CYCLES
04CB 39 55                      ROL     Y+1
04CD 39 54                      ROL     Y
04CF 39 55                      ROL     Y+1
04D1 39 54                      ROL     Y

                        * A TO D NEEDS EXTRA 63 CYCLES
04D3 A6 0A                      LDA     #$A             A TO D NEEDS >=88
CYCLES FOR CONVERSION
```

```
                        CYC53_2
04D5 4A                         DECA
04D6 26 FD                      BNE     CYC53_2

                        * GET ANOTHER CONTACT *
04D8 11 02                      BCLR    ADSEL_,PORTC
04DA A6 10                      LDA     #$10            GET CONTACT
04DC B7 24                      STA     SPDR
04DE 0F 23 FD                   BRCLR   SPIF,SPSR,*
04E1 B6 24                      LDA     SPDR
04E3 B7 57                      STA     FN
04E5 3F 24                      CLR     SPDR
04E7 0F 23 FD                   BRCLR   SPIF,SPSR,*
04EA B6 24                      LDA     SPDR
04EC B7 58                      STA     FN+1
04EE 10 02                      BSET    ADSEL_,PORTC
                        * CHECK CONTACT LEVEL IN FN IS LARGER THAN TRIGGER *
04F0 A6 C0                      LDA     #TRIGGERH
04F2 B7 59                      STA     SN
04F4 A6 00                      LDA     #TRIGGERL
04F6 B7 5A                      STA     SN+1
04F8 CD 02 B0                   JSR     LONGCMP
04FB 24 03                      BHS     SUCCESS
04FD CC 04 72                   JMP     FAILEXIT
                        SUCCESS
0500 10 50                      BSET    CONTACT,TSPFLGS
0502 81                         RTS

                    ***************** INVERSE ***********************************
                        INVERSE
0503 1B 32                      BCLR    BS1,LCDMREG
0505 18 32                      BSET    BS0,LCDMREG
0507 3F 2B                      CLR     RGTPTR
0509 A6 97                      LDA     #$97
050B B7 2C                      STA     RGTPTR+1
050D 1E 28                      BSET    RSW,MODE
050F A6 9F                      LDA     #HFLOOP
0511 B7 2E                      STA     LOOP+1
0513 3F 2D                      CLR     LOOP
0515 1F 28                      BCLR    RSW,MODE
0517 A6 88                      LDA     #$88
0519 B7 2A                      STA     LFTPTR+1
051B A6 0F                      LDA     #$F
051D B7 2F                      STA     HP
051F 15 32                      BCLR    CR2,LCDMREG
0521 AE 08                      LDX     #WICONY1
                        NEXTROW1
0523 12 32                      BSET    CR1,LCDMREG
0525 BF 31                      STX     SEGMENT
0527 A6 61                      LDA     #%01100001
0529 B7 28                      STA     MODE
052B 06 30 FD                   BRSET   RGST,STATUS,*
052E 13 32                      BCLR    CR1,LCDMREG
0530 BF 31                      STX     SEGMENT
0532 5C                         INCX
0533 A3 17                      CPX     #WICONY2
0535 23 EC                      BLS     NEXTROW1
0537 3F 2A                      CLR     LFTPTR+1
0539 81                         RTS

                    ***************** PUTICON ***********************************
                        PUTICON
053A 1B 32                      BCLR    BS1,LCDMREG
053C 18 32                      BSET    BS0,LCDMREG
053E 3F 2B                      CLR     RGTPTR
0540 A6 87                      LDA     #$87
0542 B7 2C                      STA     RGTPTR+1
```

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0544 1E 28                          BSET    RSW,MODE
0546 A6 9F                          LDA     #HFLOOP
0548 B7 2E                          STA     LOOP+1
054A 3F 2D                          CLR     LOOP
054C 1F 28                          BCLR    RSW,MODE
054E A6 0F                          LDA     #$F
0550 B7 2F                          STA     HP
0552 15 32                          BCLR    CR2,LCDMREG
0554 5F                             CLRX
0555 A6 08                          LDA     #WICONY1
                            NEXTROW
0557 B7 56                          STA     YD
0559 12 32                          BSET    CR1,LCDMREG
055B B7 31                          STA     SEGMENT
055D D6 05 7C                       LDA     ICONBASE,X
0560 B7 2D                          STA     SHTREG
0562 5C                             INCX
0563 D6 05 7C                       LDA     ICONBASE,X
0566 B7 2E                          STA     SHTREG+1
0568 A6 42                          LDA     #%01000010
056A B7 28                          STA     MODE
056C 5C                             INCX
056D 06 30 FD                       BRSET   RGST,STATUS,*
0570 13 32                          BCLR    CR1,LCDMREG
0572 B6 56                          LDA     YD
0574 B7 31                          STA     SEGMENT
0576 4C                             INCA
0577 A1 10                          CMP     #$10
0579 26 DC                          BNE     NEXTROW
057B 81                             RTS
                            ICONBASE
057C FF FF 80 01 80 41              FCB     $FF,$FF,$80,$01,$80,$41,$80,$A1
     80 A1
0584 81 91 82 C9 84 65              FCB     $81,$91,$82,$C9,$84,$65,$8C,$39
     8C 39
058C 96 11 A3 21 91 C1              FCB     $96,$11,$A3,$21,$91,$C1,$88,$C1
     88 C1
0594 85 F9 BF FD 80 01              FCB     $85,$F9,$BF,$FD,$80,$01,$FF,$FF
     FF FF

7FF6                                ORG     $7FF6
7FF6 02 C8                  VTIMER  FDB     TIMERSERVER

7FFE                                ORG     $7FFE
7FFE 02 00                  VRESET  FDB     DRAWRUB
```

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