AN10365

Surface mount reflow soldering

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Document information

Info	Content
Keywords	surface mount, reflow soldering, component handling
Abstract	This application note provides guidelines for the board mounting and handling of NXP semiconductor packages.

Revision history

Rev	Date	Description
06	20120730	amendments to Section 2.4
05	20110906	added Section 2.4
04	20090813	text amendments to Section 2.1, 2.3, 4.3, 5.1; Section 6 “Component handling” added; items added to Section 8 “References”; Export control disclaimer added to Section 9.2 “Disclaimers”.
03	20080422	various text amendments to Section 1, 2.1, 2.2, 2.3, 3, 4.1, 4.2, 4.3 and 6.
02	20060726	updates in Table 1, Table 8 and on page 20: the minimum peak reflow temperature when using SnPb solder is changed from 210 °C to 215 °C.
01	20050524	initial version.

Contact information

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1. Introduction

This application note provides guidelines for board mounting of surface mount semiconductor packages. Nowadays, reflow soldering is a widely spread technology for soldering of surface mount semiconductor packages. For some of the newer semiconductor packages, such as a Ball Grid Array (BGA), reflow soldering is the only suitable method.

This application note describes the materials for reflow soldering: the Printed-Circuit Board (PCB), semiconductor packages and solder paste. One of the key features of the PCB is the footprint design. The footprint design describes the recommended solder land on the PCB to make a reliable solder joint between the semiconductor package and the PCB. A proven solder material is SnPb, but due to legislation, the industry has changed, to a large extent, to Pb-free solutions such as Sn/Ag/Cu (SAC). Process requirements for solder paste printing and reflow soldering, for SnPb and Pb-free, are also discussed in this application note. This document concludes with sections on inspection and repair and component handling.

2. Materials

2.1 Printed-circuit boards and footprints

Printed-Circuit Boards (PCBs) are not only used as mechanical carriers for electronic components; they also provide the electronic interconnection between these components and also between these components and the outside world. These electronic components may be semiconductors, or other types such as capacitors and resistors. Through component selection and the use of Cu interconnections between the components, an electronic system, such as a mobile phone, can be assembled on a PCB. The substrates used for mounting the packages can be made of a variety of materials with different properties such as FR4, FR5, BT, flexible polymers (polyimides or polyamid) etc.

Due to the increased transistor density in the latest semiconductor technologies, and higher current (power) handling requirements, generation of heat has become a major limitation of semiconductor performance. By applying an exposed pad or heat sink in the semiconductor package, in combination with thermal vias in the PCB, the heat can be transferred from the active die to the outside world. Four examples of vias capped in different ways, are shown in Figure 1. Note that the only difference lies in the solder resist pattern.

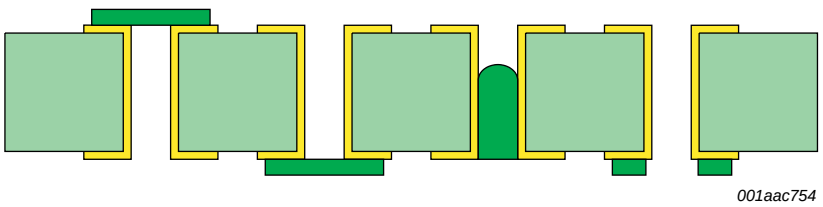


Fig 1. Capped vias; from left to right: via tenting from top, via tenting from bottom, via capping from bottom, via encroached from bottom

Common board finishes include NiAu, Organic Solderability Preservative (OSP), and immersion Sn. Although finishes may look different after reflow, and some appear to have better wetting characteristics than others, all common finishes can be used, provided that they are in accordance with the specifications.

Examples of other issues in board quality are tolerances on the pad and solder resist dimensions and component placement, maximum board dimensions, and flatness.

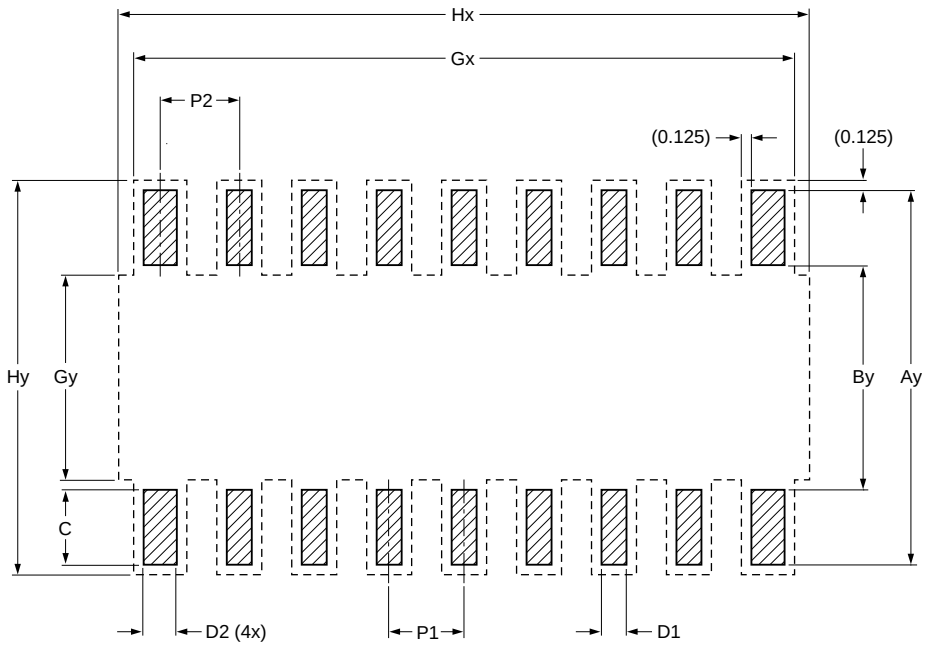
The application board is usually a mix of large and small components together with thermal design features. In board designs where large components or thermal design features are in close proximity to small components, solderability issues may arise.

A footprint design describes the recommended dimensions of the solder lands on the PCB, to make reliable solder joints between the semiconductor package and the PCB. The package outline and PCB footprints of NXP semiconductor packages can be found by clicking “Packages” in the “Looking for products” panel on the product information page of the NXP Semiconductors web site at the URL given in “Contact information” at the bottom of page 2. The unique identifier for the PCB footprint is the NXP package outline code (the package SOT or SOD number).

For general guidelines on board design, see *IPC-7351: Generic requirements for surface mount devices and land pattern standard*.

The next paragraph explains how to read the PCB footprint. Figure 2 shows an example of a PCB footprint, as found on the NXP Semiconductors web site.

Footprint information for reflow soldering of SSOP20 package **SOT266-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

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Fig 2. PCB footprint for the SOT266-1 package (SSOP20)

All footprints within a package family (in this example all SSOP packages) use the same generic footprint drawing, regardless of the actual number of package terminals. In this example, it is not accidental that the generic footprint drawing shows 18 terminals, whereas the SSOP20 package has 20 terminals. The table on the PCB footprint, below the drawing, shows the actual dimensions for the specific package outline (with 20 terminals), while the generic drawing is used to illustrate the dimensions. The real package outline (with the correct number of terminals) can be found by clicking "Packages" in the "Looking for products" panel on the product information page of the NXP Semiconductors web site at the URL given in "Contact information" at the bottom of page 2.

The soldering process is carried out under a set of process parameters that includes accuracies in the process, and semiconductor package, board, and stencil tolerances. The footprint design is directly related to these aspects of the soldering process; the calculation of these dimensions is based on process parameters that are compliant with modern machines and a state-of-the-art process.

A solder resist layer (also known as a solder mask layer) is usually applied to the board, to isolate the solder lands and tracks. If this solder resist extends onto the Cu, the remaining area to be soldered is solder resist defined. This is sometimes referred to as Solder Mask Defined (SMD). Figure 3 shows solder resist defined pads; yellow is Cu and dark green is solder resist. The Cu underneath the solder resist is shown in a lighter shade of green.

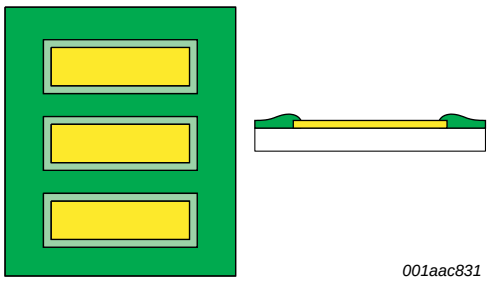

Fig 3. Solder resist defined solder lands

The alternative situation is that the solder resist layer starts outside of the Cu. In that case, the solder lands are Cu defined. This is sometimes referred to as Non Solder Mask Defined (NSMD). A Cu defined layout is shown in Figure 4 (white is the bare board).

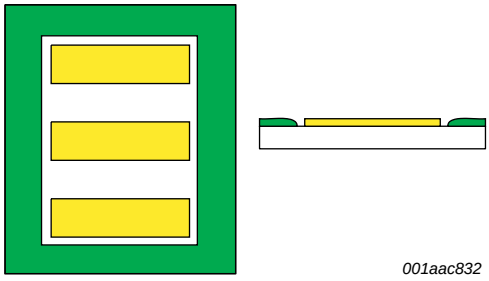

Fig 4. Cu defined solder lands

A layout can also be partially solder resist defined and partially Cu defined.

Note that a solder resist defined layout requires the application of a solder resist bridge between two terminals. There is a minimum width of solder resist that can be applied by board suppliers. This fact, in combination with a maximum solder resist placement accuracy, implies that solder resist defined layouts are not always possible. For semiconductor packages with a small pitch it is not possible to apply a solder resist bridge between two terminals, and a Cu defined or combination layout must be used.

If a solder land is solder resist defined, the Cu must extend far enough underneath the solder resist to allow for tolerances in Cu etching and solder resist placement during board production. Similarly, if a solder land is Cu defined, the solder resist must lie sufficiently far away from the solder land to prevent bleeding of the solder resist onto the Cu pad. Typical values for these distances are 50 μm to 75 μm.

The footprints referred to in this document indicate the areas that can be soldered.

The footprint shown in Figure 2 is redefined for both a solder resist and a Cu layout in Figure 5. Note that the overlap/gap between the solder resist and the Cu is 0.05 mm in this particular example.

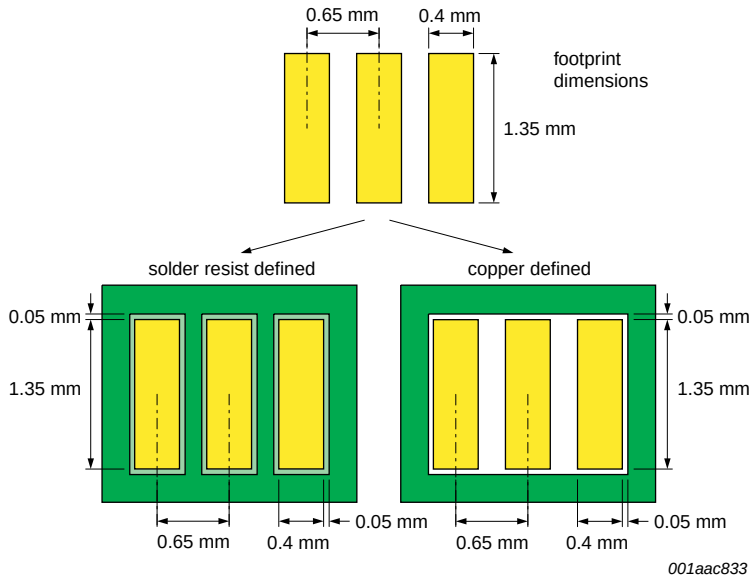

Fig 5. Solder land dimensions for SOT266-1 package, either solder resist or Cu defined

2.2 Semiconductor packages

Semiconductor packages can be divided into groups. In this document, they are categorized according to the shape of the terminals, as this has the largest influence on board assembly. Accordingly, the three main semiconductor family types are:

- leaded packages
- leadless packages with solder balls
- leadless packages with solder lands

Apart from the terminals, packages can have heat sinks and/or ground connections.

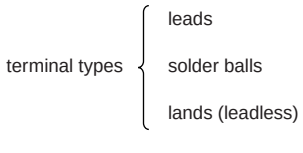

Fig 6. Package types

Leaded packages

- Coplanarity is an important issue: coplanarity must be within the specifications (refer to the package outline drawing) in order to prevent the occurrence of open circuits or bad joints; poor coplanarity may also increase problems caused by board warpage
- The tips of leads, where they are cut out of the lead frame, do not have to be wetted after reflow
- Within NXP Semiconductors, two possible lead finishes are applied: pure Sn, and NiPdAu. The finish used depends on the package family. SnPb finish is still used, but only for selected applications.
- Leaded packages can be reflow soldered: standard gullwing packages can be wave soldered only if the lead pitch is equal to, or larger than, 0.65 mm and if no exposed heatsink is present. Wave soldering smaller pitches will lead to a higher defect level.

a. Gullwing b. Flatpack

Fig 7. Example of leaded packages

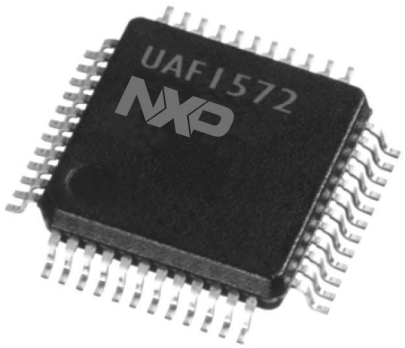

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Fig 8. Example of leaded package: QFP

Leadless packages with solder balls

- These semiconductor packages are particularly good at self-alignment, as the package body is essentially suspended over molten solder during reflow; therefore, this package type results in a robust reflow soldering process
- The balls are made of SnPb, or SAC for Pb-free applications
- Packages with solder balls can only be reflow soldered, they cannot be wave soldered

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Fig 9. Example of leadless packages with solder balls: BGA, TFBGA

Leadless packages with solder lands

- The exposed lead frame edges at the sides of the semiconductor packages are often not finished - these do not have to be wetted for a proper joint
- Possible solder land finishes are pure Sn or NiPdAu for Pb-free applications and in exceptions SnPb
- Leadless packages with solder lands can only be reflow soldered, they cannot be wave soldered

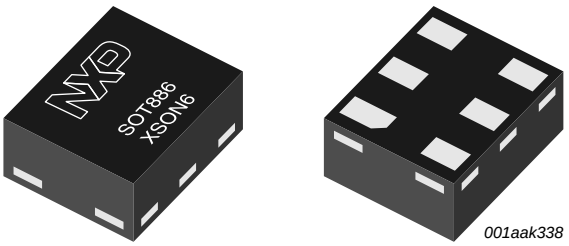

Fig 10. Example of leadless packages with solder lands: QFN (including ultra small), SON

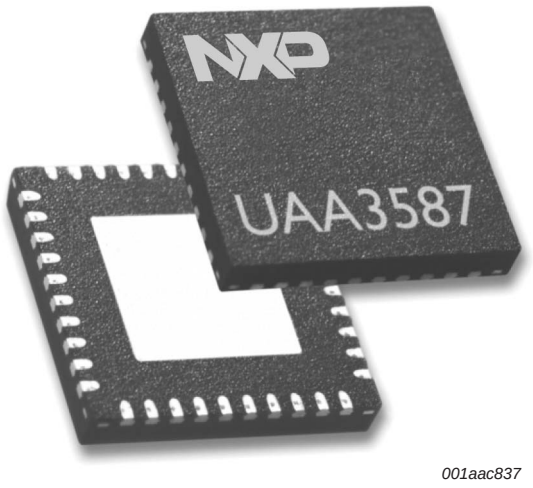

Fig 11. Example of leadless packages with solder lands: HVQFN

Semiconductor packages can have heat sinks at the top or the bottom of the package. The following remarks apply to those with heat sinks at the bottom, such as HVQFNs:

- Even if the exposed pad does not have to be soldered to the board for electrical or thermal purposes, the package reliability may improve if it is soldered to the board
- Voids in the solder joint connecting the heat sink pad to the board are allowed, provided that this does not conflict with demands made by the application

2.3 Solder paste

In line with European legislation, it is recommended to use Pb-free solder paste, although exemptions are granted for selected applications, such as automotive.

A wide variety of Pb-free solder pastes are available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes have a wide range of melting temperatures. Solders with a high melting point may be more suitable for the automotive industry, whereas solders with a low melting point can be used for soldering consumer semiconductor packages.

As a substitute for SnPb solder, the most common Pb-free paste is SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 3 % to 4 % of Ag and 0 % to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and it requires a reflow temperature of more than 235 °C.

Table 1. Typical solder paste characteristics

Solder	Melting temperature	Minimum peak reflow temperature[1]
SAC	217 °C	235 °C
SnPb	183 °C	215 °C

[1] Temperature is measured at solder joint.

Care should be taken when selecting a solder, and note that solder types are categorized by solder sphere size. For small packages or fine pitch applications solder paste type 3 or better is recommended.

A no-clean solder paste does not require cleaning after reflow soldering and is therefore preferred, provided that this is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflow.

For more information on the solder paste, please contact your solder paste supplier.

2.4 Specific items for HVQFN/HVSON packages

2.4.1 Pin 1 Keep out area

For the purpose of package orientation, a so called “pin 1” identification is included. This can either be as an additional small pin/pad as shown in design 1 (left) of Figure 12, or a notch in the diepad as shown in design 2 (right) of Figure 12.

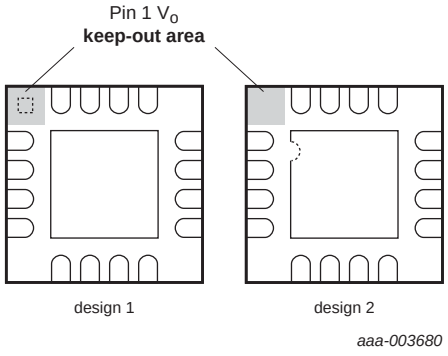

Fig 12. HVQFN/HVSON package ‘Keep out area’

This feature may not necessarily be defined in the package outline as published. However in the event of an open trace on the PC-board, there may be unintentional contact between this trace and the pin 1 pad, leading to a malfunction. In order to prevent this, NXP prescribes a so called “keep out” area for the HVQFN corner/pin 1 area of the PC-board, as indicated in Figure 12. This applies in general for all HVQFN/HVSON designs.

2.4.2 HVQFN wettable sides

In a standard HVQFN/HVSON package, the sides of the terminals consist of bare Cu. As a result, the sides of the terminals may not be wetted during reflow soldering. Non-wetting failures are difficult to detect in HVQFN/HVSON packages.

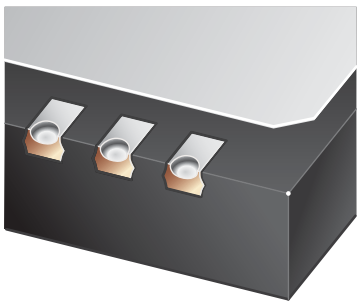

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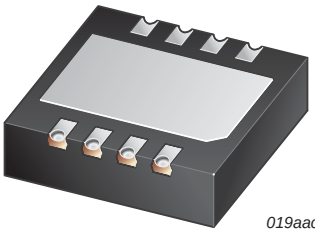
Fig 13. HVQFN/HVSON package with 'wettable flank'

A 'wettable flank' option may be requested for variants of these packages with a terminal pitch ≥ 0.65 mm. The exposed edge of each terminal contains a small cavity. The cavity is plated, ensuring the solder flows into it and adheres to the side of the terminal.
Non-wetting of the sides can be detected more easily with the wettable-flank option, simplifying the inspection process.



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3-d view showing cavities

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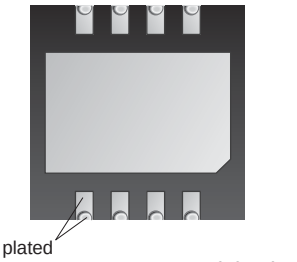
side view



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bottom view

Fig 14. 3-d, side and bottom views

3. Moisture sensitivity level and storage

If there is moisture trapped inside a package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may result in a cracked semiconductor package body (the popcorn effect). A package's sensitivity to moisture, or Moisture Sensitivity Level (MSL), depends on the package characteristics and on the temperature it is exposed to during reflow soldering.

The MSL of semiconductor packages can be determined through standardized tests in which the packages are moisturized to a predetermined level and then exposed to a temperature profile. Studies have shown that small and thin packages reach higher temperatures during reflow than larger packages. Therefore, small and thin packages must be classified at higher reflow temperatures.

The temperatures that packages are exposed to are always measured at the top of the package body.

Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package. For every product, this MSL is given on a packing label on the shipping box. Each package is rated at two temperatures, for SnPb and Pb-free soldering conditions. An example of a packing label is given in Figure 15.

Fig 15. Example of MSL information on packing label; note the two MSLs corresponding to the two reflow processes

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow, in order to remove any moisture that might have soaked into the package. MSLs and temperatures on the packing labels are to be respected at all times. Naturally, this also means that semiconductor packages with a critical MSL may not remain on the placement machine between assembly runs. Nor should partly-assembled boards, between two reflow steps, be stored longer than indicated by the MSL level.

The semiconductor package floor life, as a function of the MSL, can be found in Table 2.

Table 2. Floor life as a function of MSL[1]

MSL	Floor life	
	Time	Conditions
1	unlimited	≤ 30 °C/85 % RH
2	1 year	≤ 30 °C/60 % RH
2a	4 weeks	≤ 30 °C/60 % RH
3	168 hours	≤ 30 °C/60 % RH
4	72 hours	≤ 30 °C/60 % RH
5	48 hours	≤ 30 °C/60 % RH
5a	24 hours	≤ 30 °C/60 % RH
6	6 hours	≤ 30 °C/60 % RH

[1] Refer to *IEC 61760-2 Transportation and storage conditions of surface mounting devices* and/or *IPC/JEDEC J-STD-033B.1 Handling, packing, shipping and use of moisture/reflow sensitive surface mount devices*.

4. Surface mounting process

4.1 Solder paste printing

Solder paste printing requires a stencil aperture to be completely filled with paste. When the board is released from the stencil, the solder paste is supposed to adhere to the board so that all of the paste is released from the stencil aperture and a good solder paste deposit remains on the board. Ideally, the volume of solder paste on the board should equal the ‘volume’ of the stencil aperture.

In practice, however, not all of the solder paste is released from the stencil aperture. The percentage of paste released depends largely on the aperture dimensions, that is, the length and width and the depth (the stencil thickness). If a stencil aperture becomes very small, the paste will no longer release completely. Furthermore, stencil apertures must be larger if a thicker stencil is used.

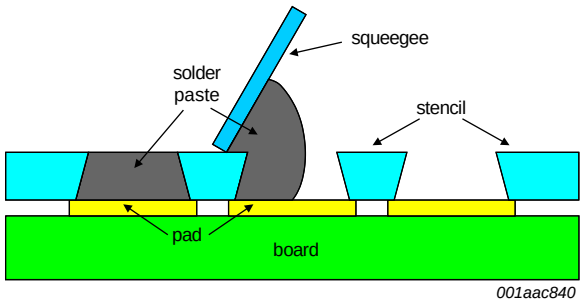


Fig 16. Stencil printing

Another important factor is the aperture shape, that is, whether the aperture is rectangular, trapezoidal, or otherwise. Paste release also depends - amongst others - on the loading and speed of the squeegee, the board separation speed, the printing direction, and the aperture orientation. In essence, all of these parameters must be adjusted so that all solder paste deposits on one board, from the smallest to the largest, are printed properly.

Consequences of insufficient solder paste printing are usually open contacts or bad joints. These may arise because:

- The solder paste deposit is not sufficiently high: components or their leads may not make proper contact with the paste, resulting in open circuits or bad joints,

or

- There is insufficient solder volume for a proper solder joint, also resulting in open circuits,

or

- The activator is used up rapidly in a small solder paste deposit, so that the paste no longer properly wets the component metallization, also resulting in open circuits

A second important aspect in solder paste printing is smearing. If some solder paste bleeds between the stencil and the board during one printing stroke, then the next board may not fit tightly to the stencil, allowing more paste to bleed onto the bottom of the stencil. Once this effect starts, it strengthens itself. As a result, the solder paste may eventually form bridges that stretch from one paste deposit to the next. If a bridge is narrow enough, it will snap open during reflow, as the volume of molten solder seeks to attain minimum surface area. A wider bridge, however, may remain stable, resulting in a short-circuit.

To achieve a difference in solder paste volumes on one board, it is possible to use a stencil that has a different thickness at different locations. An example of this is the step-stencil. This, however, is only recommended if there is no other solution.

Stencils are commonly made from Nickel; they may be either electro-formed or laser-cut (preferred). Typical stencil thicknesses are given in Table 3.

Table 3. Typical stencil thickness

Semiconductor package pitch	Stencil thickness
≥ 0.5 mm	150 μm
0.4 mm to 0.5 mm	100 μm to 125 μm

A general rule is that the stencil apertures must be 25 μm smaller than the solder lands, on all sides. In other words, the solder paste lies 25 μm inward from the solder land edge. This usually results in stencil aperture dimensions that are 50 μm smaller than the corresponding solder land dimensions; see Figure 17.

This rule does not apply for a BGA; for a BGA the solder paste deposit is shown explicitly in the PCB footprint specification. Although BGA balls and their solder pads are circular, square stencil apertures are sometimes preferred for a BGA.

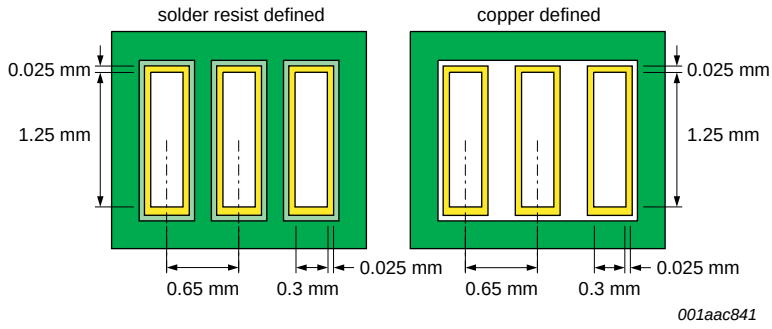


Fig 17. Solder paste printing on solder and capped resist defined layouts

Another exception lies with the very large solder lands, such as when printing solder paste on a heat sink land. In that case, it is advised to print an array of smaller solder paste deposits. The solder paste should cover approximately 20 % of the total land area. It is also advised to keep the solder paste away from the edges of this land: the solder paste pattern, including the spacing between the deposits, should have a coverage of 35 % of the land area; see Figure 18 and Figure 19.

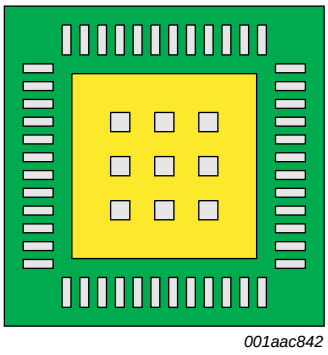


Fig 18. Paste coverage

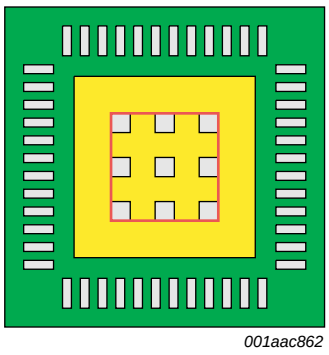


Fig 19. Pattern coverage

A paste printing pattern for exposed die pads is illustrated by the example shown in Figure 20. A HVQFN48 with an exposed pad of 5.1 mm × 5.1 mm, for example, should have nine solder paste deposits that are arranged in a three-by-three array. The solder paste deposits are 0.76 mm × 0.76 mm, and the distance between them is 0.37 mm.

This way, the solder paste area is 9 × (0.76 mm × 0.76 mm), and dividing this by the land area 5.1 mm × 5.1 mm yields a solder paste coverage of approximately 20 %.

Similarly, the solder paste pattern (the paste, plus the area between the deposits) has a length of 3.02 mm. The pattern area, 3.02 mm × 3.02 mm, divided by the land area, yields a paste pattern coverage of approximately 35 %.

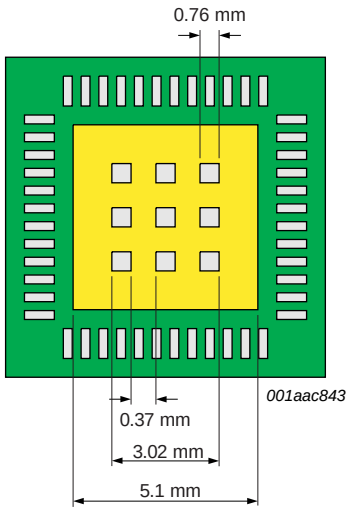


Fig 20. Solder paste dimensions on the land area for an exposed die pad of HVQFN48

Depending on the solder paste used, the solder paste deposits printed on a large land may not always coalesce completely. In some cases, individual solder joints can still be recognized between the exposed die pad and solder land on the board. It is possible that voids remain in the solder joints. Whether or not voids or incomplete coalescing of the solder are a problem, depends on the application. For low-power devices in which little heat is generated, up to 80 % of voids may still be acceptable.

Keep in mind that printing a smaller volume of solder paste could have adverse effects on the solder joint reliability. Also, if there are vias in pads, solder paste deposits should be arranged so that paste is never printed directly over a via.

4.2 Semiconductor package placement

The required placement accuracy of a package depends on a variety of factors, such as package size and the terminal pitch, but also the package type itself. During reflow, when the solder is molten, a package that has not been placed perfectly may center itself on the pads: this is referred to as self-alignment. Therefore, the required placement accuracy of a package may be less tight if this package is a trusted self-aligner. It is known, for example, that a BGA is good at self-alignment, as the package body essentially rests on a number of droplets of molten solder, resulting in minimal friction.

Remark: Self-alignment properties can be improved by performing the reflow process in an N2 environment.

Typical placement tolerances, as a function of the semiconductor package terminal pitch, are given in Table 4.

Table 4. Typical placement accuracy

Package terminal pitch	Placement tolerance (±3 sigma)
≥ 0.65 mm	100 μm
< 0.65 mm > 0.5 mm	50 μm
< 0.5 mm	30 μm

Semiconductor packages are usually placed with two types of machines. If the highest placement accuracy is required, the slower but more accurate machines must be used. These machines are also often more flexible when it comes to unusual package shapes, that may require dedicated nozzles and non-standard trays. If the highest placement accuracy is not necessary, and there are no special requirements, fast component mounters or chip shooters, can be used. These machines can process up to 100,000 components per hour.

The placement force may also be an important parameter for some packages. In theory, a semiconductor package is always pressed down into the solder paste until it rests on a single layer of solder paste powder particles - the rest of the solder paste is pressed aside. A consequence that is immediately apparent, is that the solder paste that is pushed aside, or that bulges outside the package, may cause bridges with neighboring solder paste deposits.

In extreme cases, solder paste may not only bulge outside the pads, but may actually be blasted further away from the pads, so that a small amount of solder paste is no longer connected to the paste deposit it originally came from. This must always be avoided as the splattered solder paste may cause a short circuit on the board, and the original solder paste deposit may then have insufficient solder. Incidentally, this effect is often caused in part by use of an improper nozzle shape, so that the paste is actually blown away by air from the nozzle.

If the placement force is too low, there is a chance that a semiconductor package terminal does not make sufficient contact with the solder paste. In that case, there is a risk that the solder paste tackiness will not be able to hold it in place up to the reflow zone in the oven, and the package may be displaced. In addition, even if the semiconductor package remains in place, there may be bad contact between the package terminals and the solder paste resulting in open contacts or bad joints.

Therefore, the placement force must always be adjusted so that there is no excessive paste bulging or even splattering and there is a proper contact between the semiconductor package and the solder paste. The necessary placement force to achieve this will depend on a number of factors, including the package dimensions. Typical forces are 1.5 N to 4 N. Note however, that some of the more modern machines have a sensor that detects the package’s proximity to the solder paste so that the placement speed is reduced as soon as the package comes near to, or touches, the solder paste. In this way, splattering can be minimized.

4.3 Reflow soldering

The most important step in reflow soldering is reflow itself when the solder paste deposits melt and soldered joints are formed. This is achieved by passing the boards through an oven and exposing them to a temperature profile that varies in time.

A temperature profile essentially consists of three phases:

1. Preheat: the board is warmed up to a temperature that is lower than the melting point of the solder alloy
2. Reflow: the board is heated to a peak temperature that is well above the melting point of the solder but below the temperature at which the components and boards are damaged

3. Cooling down: the board is cooled down rapidly so that soldered joints freeze before the board exits the oven

The peak temperature during reflow has an upper and a lower limit:

- Lower limit of peak temperature (measured at the solder joint): the minimum peak temperature must be at least high enough for the solder to make reliable solder joints, determined by solder paste characteristics; contact your paste supplier for details
- Upper limit of peak temperature (measured at the top of the component body); the maximum peak temperature must be lower than:
  a. The test temperature used for MSL assessment; see Section 3 “Moisture sensitivity level and storage”.
  b. The temperature at which the boards are damaged, a board characteristic; contact your board supplier for details.

A rough indication of the recommended minimum peak temperatures for SnPb and SAC alloys is given in Table 5. However, these values should be verified with your solder paste supplier.

Table 5. Typical solder paste characteristics

Solder	Melting temperature	Minimum peak reflow temperature
SAC	217 °C	235 °C
SnPb	183 °C	215 °C

When a board is exposed to the profile temperature, certain areas on the board will become hotter than others: a board has hot spots (the hottest areas) and cold spots (the coolest areas). Cold spots are usually found in sections of the board that hold a high density of large components, as these soak up a lot of heat. Large areas of Cu in a board will also reduce the local temperature. Hot spots, on the other hand, are found in areas with few components, or only the smallest components, and with little Cu. Finally, the board dimensions, and the board orientation in the oven, may also affect the location of hot and cold spots.

The temperature of the hot spot on a board must be lower than the upper limit of the peak temperature. Similarly, the temperature of the cold spot must be higher than the lower limit of the peak temperature.

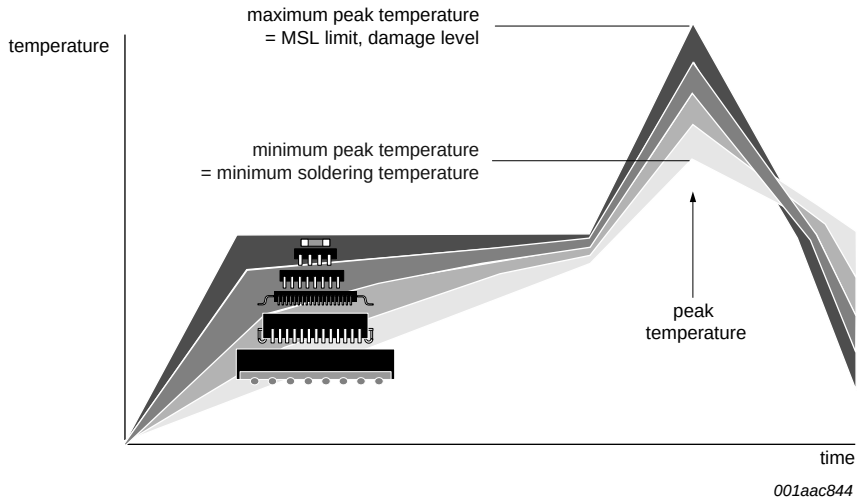


Fig 21. Temperature profiles for large and small components

In Figure 21, the grey band with the large component represents cold spots, and the dark band, at the top, with the smallest component, represents hot spots. In both cases, the graph first represents a component body temperature, measured at the top of the body. In the preheat phase, the hot spots will heat up rapidly to a temperature lower than the melting point of the solder alloy. They may remain at this temperature for a while. Note however, that small solder paste deposits should not remain at an intermediate temperature for so long that their activator runs out: for small solder paste deposits, a fast temperature profile is preferred. The cold spots on the board will warm up far more slowly. The oven settings should be planned so that the cold as well as the hot spots will have reached roughly the same temperature by the end of the preheat phase.

The second phase in the reflow profile is the reflow zone, in which the solder melts and forms soldered joints. The minimum peak temperature, which all solder joints in the cold as well as the hot spots must reach, depends on the solder alloy. However, no region on the board may surpass a maximum peak temperature as this would result in component and/or board damage. See Section 3 “Moisture sensitivity level and storage” for more information. Even if the cold and hot spots at the start of the reflow phase have roughly the same temperature, the hot spots will reach a higher peak temperature than the cold spots. Yet, both the hot spots and the cold spots must lie within the allowed peak temperature range. This may require some tweaking of the oven temperature settings and conveyor belt speeds. In some cases, the board layout may have to be optimized to limit the temperature difference between the cold and the hot spots.

When reflow soldering, the peak temperature should never exceed the temperature at which either the components or the board are damaged. The maximum peak temperature for components is partially determined by their moisture sensitivity. For reflow soldering with SnPb solder, the peak temperature should be higher than 215 °C; when soldering with SAC, the peak temperature should be higher than 235 °C, but should not exceed a temperature of 260 °C. Note that this usually implies a smaller process window for Pb-free soldering, thus requiring tighter process control.

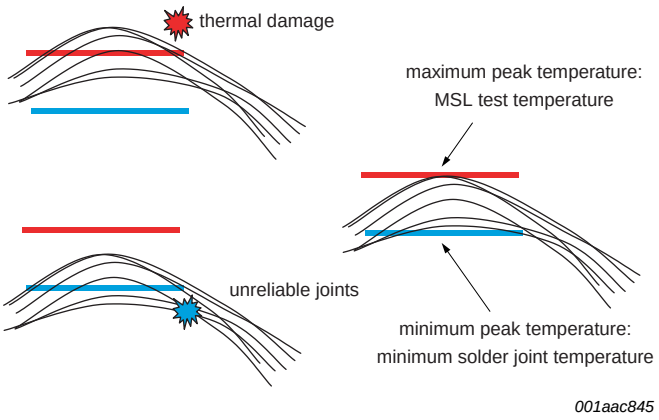


Fig 22. Fitting both the hot and cold spots into the required peak temperature range

The black lines in Figure 22 represent the actual temperature profiles for a number of different temperature spots on a board. The bottom black line represents the coldest spot, and the top black line represents the hottest spot. The blue line represents the minimum peak temperature, and the red line is the maximum peak temperature. At the top left, some regions on the board are exposed to temperatures that are too high, exceeding MSL qualification conditions. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all of the regions on the board have peak temperatures that fall within the upper and lower limits.

Reflow may be done either in air or in nitrogen. In general, nitrogen should not be necessary; in that case, air is preferred because of the lower cost. Reflow may be done in convection reflow ovens, some of which have additional infrared heating. Furthermore, using vapor phase reflow soldering can reduce temperature differences on a board.

Application boards are usually populated with components on both sides of the board. This means that the board will need to undergo a soldering process twice. It is important, therefore, that the following details are taken into consideration prior to a double-sided reflow process to prevent damage to, or malfunction of the components.

- Components should be able to withstand multiple reflow cycles. As components are MSL classified, they are guaranteed to withstand three reflow cycles.
- If the time between first and second reflow exceeds the floor life of the corresponding MSL classification, the application board needs to be dried before the second reflow. Storage between reflow steps in a nitrogen cabinet or sealed MBB is also an option.
- Heavy components mounted during the first reflow may drop off during the second reflow, either due to their weight or because of vibration during transport through the reflow oven. Heavy components may be fixed in place with glue before reflow soldering.

4.4 Solder and terminal finish or solder ball compatibility

When selecting a solder paste, care must be taken that the solder is compatible with both the board and the semiconductor package finishes. When soldering leaded or leadless packages, all package finishes can be combined freely with all solders; see Table 6.

Table 6. Compatibility of ball and solder paste alloys, for leaded or leadless packages

Terminal finish	SnPb solder	Pb-free solder
SnPb	mature technology	ok
Pb-free	ok	ok

This however, is not the case for packages with solder balls. If these packages are soldered, the semiconductor package solder balls and the solder paste both melt to form a single joint. Therefore, it is essential that the reflow temperature profile reaches a temperature that is high enough for both the solder paste and the solder ball to melt and to form proper solder joints.

SnPb needs a temperature of at least 215 °C, but at least 235 °C is required for most Pb-free solders. There are four options:

- SnPb balls are combined with a SnPb paste: the balls and paste form good joints at a temperature of 215 °C or more. This combination has been used for decades.
- SnPb balls are combined with a Pb-free paste: the paste requires a higher reflow temperature of at least 235 °C; the solder balls only need 215 °C so they will also melt properly: ok.
- Pb-free solder balls are combined with a SnPb paste: in this case only the Pb-free balls require a higher reflow temperature, whereas the rest of the process does not. Therefore this combination is not advised.
- Pb-free solder balls are combined with a Pb-free paste: now the paste requires the same reflow temperature and so do the solder balls: ok.

The text above is summarized in Table 7.

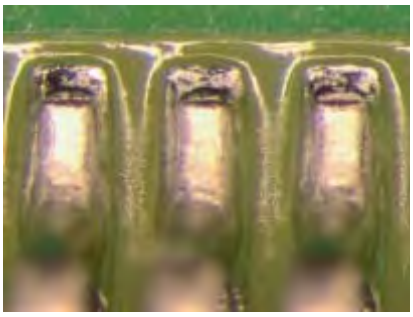
Table 7. Compatibility of ball and solder paste alloys, for packages with solder balls

Solder ball	SnPb solder	Pb-free solder
SnPb balls	mature technology	ok
Pb-free balls	not advised	ok

5. Inspection and repair

5.1 Inspection

In general, Pb-free solder is a little less successful at wetting than SnPb solders; SAC fillets will have a larger contact angle between the fillet and the wetted surface. When using Pb-free solder this contact angle may typically be 20° to 30°. Notice the difference between SnPb and Pb-free solder in Figure 23: the photograph on the left (SnPb) shows the solder lands have been wetted completely. The photograph on the right shows the solder has left part of the solder lands unwetted.



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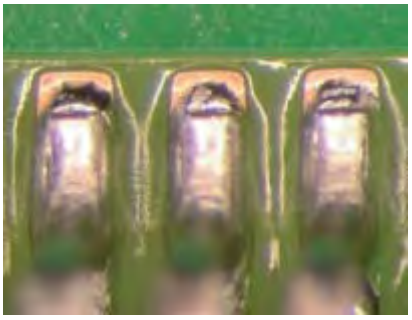
a. SnPb solder joints



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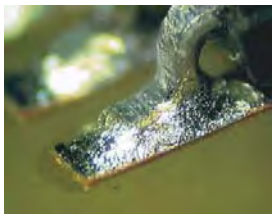
b. Pb-free solder joints

Fig 23. Difference in wetting between SnPb and Pb-free solder joints

Another visual aspect in Pb-free soldering is that Pb-free solder joints tend to be less shiny than SnPb solder joints and they may have striation marks. This is due to the different microstructure that is formed during solidification. Although SnPb solder joints should be rejected if they look this way, this is normal for Pb-free and no reason to reject Pb-free solder joints.

001aac847

a. SnPb solder joints



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b. Pb-free solder joints

Fig 24. Difference in appearance between SnPb and Pb-free solder joints

Non-wetting of lead frame parts as a result of punching or sawing is not a reason for rejection.

Other inspection methods besides optical inspection, such as, for design and process development purposes are:

- Automatic optical inspection (AOI)
- Examination by roentgen ray (X-ray)
- Cross-sectional analysis
- Dye penetration test

5.2 Repair

Sometimes, a package lead that has not been soldered properly may be repaired simply by heating this single lead with the tip of a soldering iron. In this case, it is sufficient to heat the lead until the solder melts completely; a new device should not be necessary.

In other situations however, there may be a need to replace a semiconductor package on the board. In that case, the rework process should comprise the following steps:

1. Device removal
2. Site preparation
3. Application of solder paste to the site
4. Device placement
5. Device attachment

It is advised to dry bake the board for 4 hours at 125 °C prior to steps 1 to 5.

5.2.1 Device removal

In order to remove a semiconductor package from the board, it must be heated; if possible, this must be done as locally as possible to avoid heating the surrounding board and components. Packages with leads at a relatively large pitch may first be removed from the board by cutting the leads, after which only the leads must be de-soldered. This can be done with a soldering iron.

Semiconductor packages without leads must be heated entirely for removal. Heat can be supplied using a hot air gun, a soldering iron, or focused infrared energy, depending on the package type and availability. If necessary, the bottom of the board can also be heated. The temperature to which the package solder joints should be heated depends on the solder that was originally used, and it is best to keep the temperature as low as possible, just above the melting point of the solder alloy used.

As soon as the solder has melted, the semiconductor package is lifted from the board using a vacuum wand or tweezers; note that package removal should not be initiated until the solder has melted entirely.

Re-use of removed semiconductor packages is not recommended.

5.2.2 Site preparation

After the device has been removed, the board area must be prepared for the new device. Prepare the site by removing any excess solder and/or flux remains from the board. Ideally this can be done on an appropriate de-soldering station, using solder wick or an alternative method.

After most of the solder has been removed from a solder land, a very thin layer of solder will be left on top of a few intermetallic layers. In the case of Cu boards for example, there will be layers of Cu_3Sn, Cu_6Sn_5 and finally solder, on top of the Cu. The top layer of solder is easily soldered.

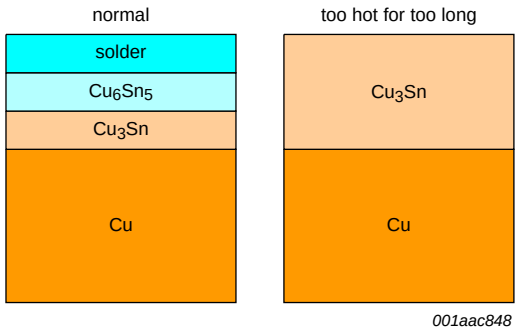

Fig 25. Overheating and Cu_3Sn formation

If however, the pad is heated too much during removal of the rejected semiconductor package and during site preparation, the top two layers will also be converted into Cu_3Sn. In this case there will only be the Cu_3Sn intermetallic layer on top of the Cu. Unfortunately, Cu_3Sn is hardly wettable, as a result, it will become very difficult to solder the replacement package at this location. Therefore, care must be taken during reject package removal and site redress that the solder lands are heated not more than necessary.

5.2.3 Solder paste printing

After the site redress is completed solder paste should be applied to either the site or the device. This can be done by using a miniature stencil or other in-house techniques. Preferably, the same type of solder paste should be used as was originally applied on the board.

If the new device that is to be soldered to the board has solder balls, solder paste printing is not necessary. In this case it suffices to apply a thin layer of tacky flux on the solder lands on the PCB.

5.2.4 Device placement

The last step of the repair process is to solder the new semiconductor package on the board. If necessary, the new package may be aligned under a microscope or split beam system, possibly in a special repair station. If this is not possible, try to align the device with board markers.

5.2.5 Soldering

To reflow the solder, apply a temperature profile that is as close as possible to the original reflow profile used for assembling the board. Take care that the board and/or semiconductor package are not moved or tilted until the solder has solidified completely. Note that if a board is exposed to reflow temperatures a second time, it may be necessary to dry bake the board for the sake of the components that have already been mounted.

6. Component handling

6.1 Electrostatic charges

Damage to semiconductors from ElectroStatic Discharge (ESD) is a major cause of rejects and poses an increased risk to miniaturized packages. Electrostatic charge can be stored in many things, for example, man-made fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. It is recommended that the following ESD precautions are complied with.

6.1.1 Workstations for handling ESD sensitive components

Figure 26 shows a working area suitable for safely handling electrostatic-sensitive devices. The following precautions should be observed.

- Workbench and floor surface should be lined with anti-static material
- Persons at a workbench should be earthed via a wrist strap and a resistor
- All mains-powered equipment should be connected to the mains via an earth leakage switch
- Equipment cases should be grounded
- Relative humidity should be maintained between 40 % and 50 %
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail
- Keep static materials, such as plastic envelopes and plastic trays away from the workbench. If there are any such static materials on the workbench remove them before handling the semiconductor devices.
- Refer to the current version of the handbook *EN 100015 (CECC 00015) "Protection of Electrostatic Sensitive Devices"*, which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices

6.1.2 Receipt and storage of components

Packing for electrostatic devices should be made of anti-static/conductive materials. Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge. The electronic components should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any electronic components that are stored temporarily should be re-packed in conductive or anti-static packing or carriers.

6.1.3 PCB assembly

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand tools should be of conductive or anti-static material and where possible should not be insulated. Standard precautions for manual handling of electrostatic-sensitive devices need to be taken into account.

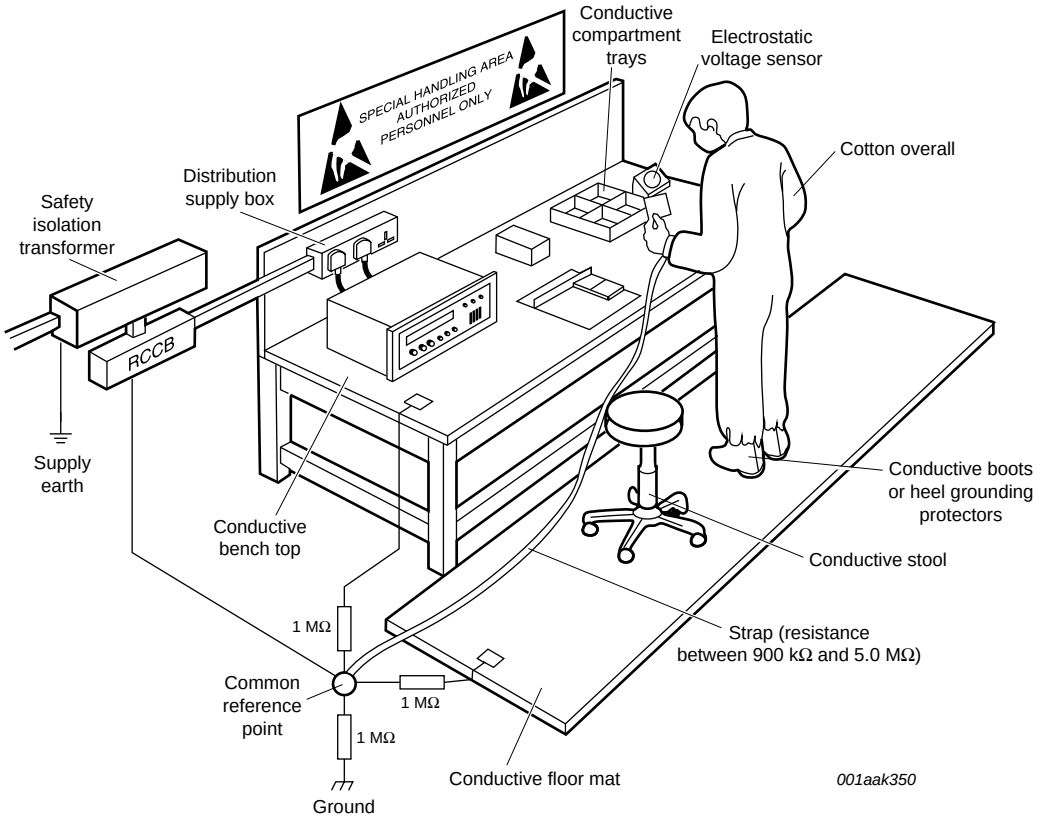

Fig 26. ESD protected workstation environment

6.1.4 Ultra small leadless packages (such as SOD882, SOT883)

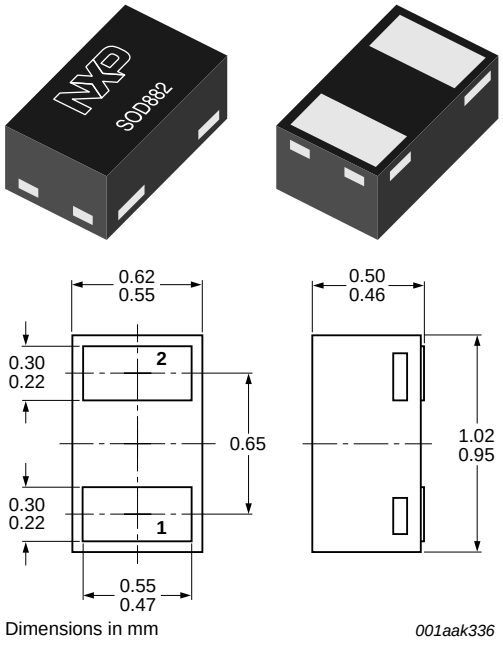

Fig 27. SOD882

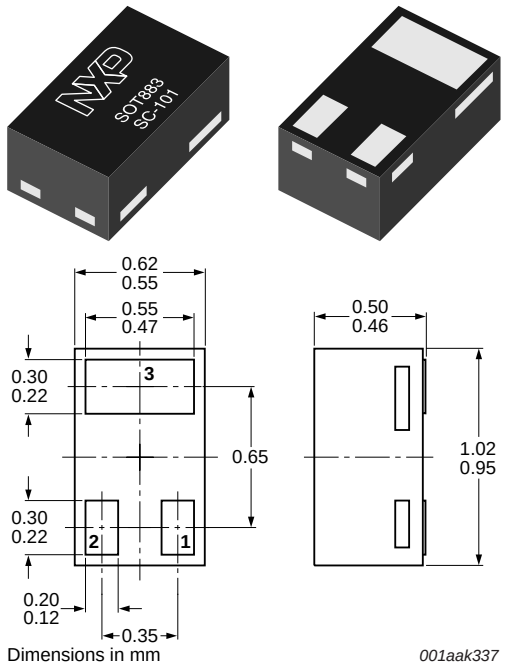

Fig 28. SOT883

The main advantage of ultra small leadless packages is that they need less board space for a given function of a semiconductor device than packages with leads. These packages however, are more susceptible to mechanical damage due to their size and construction than standard gullwing packages or packages with relatively large soldering areas. Any sheer forces acting on the side of the body of the device or excessive bending of the board can easily cause the device to be damaged or dislodged. Compliance with international board mounting standard IPC-A-610 is recommended when working with boards.

During manual processes such as physical inspection, the moving of boards to other locations and/or other manual handling processes, there is risk of damage to ultra-small leadless packages.

Special care is needed if flexible substrates (e.g. thickness in the range 0.1 mm - 0.2 mm) are used. They are designed to be folded but excessive bending, at positions where semiconductor packages are placed, needs to be excluded. During transportation in production, supporting with carrier tools (frames) is highly recommended.

The risk of damage is greater if the devices are mounted near the edge of the board rather than towards the center of the board where the small components can be surrounded by other components, thereby providing a form of protection.

Manual touching should be avoided. If manual handling is unavoidable, handle with care and avoid applying shear forces of more than 4 N to the sides of the devices. An assembled board should be held by the edges (see Figure 29), or handled while contained in a specially designed cassette or other dedicated carrier tool (frame).

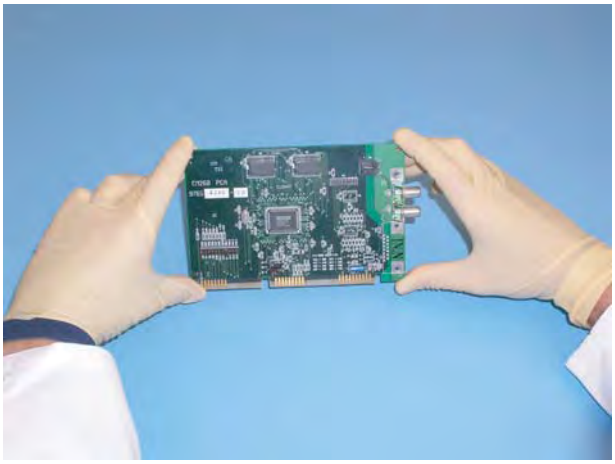

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Fig 29. Manual handling of an assembled board

7. Abbreviations

Table 8. Abbreviations

Acronym	Description
BT	Bismaleimide Triazine
FR	Flame Resistant
HVQFN	Heatsink Very thin Quad Flat-pack No leads
MBB	Moisture Barrier Bag
QFN	Quad Flat No leads
QFP	Quad Flat Package
RCCB	Residual Current Circuit Breaker
SON	Small Outline No Leads
SSOP	Shrink Small Outline Package
TFBGA	Thin and Fine-pitch Ball Grid Array
URL	Uniform Resource Locator

8. References

[1] **IPC/JEDEC J-STD-020D August 2007 —** Joint Industry Standard Moisture/Reflow, Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[2] **IPC-7351 —** Generic requirements for Surface Mount Design and Land Pattern Standard, IPC

[3] **EN 100015/CECC 00015 —** Protection of Electrostatic Sensitive Devices, European Standard

[4] **3997.750.04888 —** Quality reference handbook, NXP

[5] **IPC-A-610D —** Acceptability of Electronic Assemblies, IPC

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