### Abstract
This application note provides the guidelines for the use of Wafer-Level Packages (WLP) in fan-in and fan-out designs, using various bump attach processes with minimum bump pitches of 500 μm, 400 μm and 350 μm.
1 Introduction

This application note provides guidelines for the handling and board mounting of NXP’s Wafer Level Chip Scale Package (WLCSP) in both Fan-In Wafer-Level Packaging (FI-WLP) and Fan-Out Wafer-Level Packaging (FO-WLP) designs, including recommendations for Printed-Circuit Board (PCB) design, board mounting, and rework. Generic information of package properties such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical and thermal resistance data are also provided. Semiconductor components are Electrostatic Discharge (ESD) and mechanically sensitive devices. Proper precautions for handling, packing and processing are described.

The term WLP is used in this document to refer to both types of wafer-level packages. Information specific to fan-in or fan-out WLP is clearly marked.

2 Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>BGA</td>
<td>Ball-Grid Array</td>
</tr>
<tr>
<td>BLR</td>
<td>Board Level Reliability</td>
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<tr>
<td>CSP</td>
<td>Chip-Scale Package</td>
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<tr>
<td>ENIG</td>
<td>Electroless Nickel Immersion Gold</td>
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<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
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<td>ESDS</td>
<td>Electrostatic Discharge Sensitive</td>
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<tr>
<td>FI-WLP</td>
<td>Fan-In Wafer-Level Packaging</td>
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<tr>
<td>FO-WLP</td>
<td>Fan-Out Wafer-Level Packaging</td>
</tr>
<tr>
<td>HASL</td>
<td>Hot Air Solder Leveled</td>
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<tr>
<td>MBB</td>
<td>Moisture Barrier Bag</td>
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<tr>
<td>MSL</td>
<td>Moisture Sensitivity Level</td>
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<tr>
<td>NSMD</td>
<td>Non-Solder Mask Defined</td>
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<tr>
<td>OSP</td>
<td>Organic Solderability Preservative</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed-Circuit Board</td>
</tr>
<tr>
<td>POD</td>
<td>Package Outline Drawing</td>
</tr>
<tr>
<td>SJR</td>
<td>Solder Joint Reliability</td>
</tr>
<tr>
<td>SMD</td>
<td>Solder Mask Defined</td>
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<tr>
<td>SMT</td>
<td>Surface Mount Technology</td>
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<tr>
<td>UBM</td>
<td>Under-Bump-Metalization</td>
</tr>
<tr>
<td>WLCSP</td>
<td>Wafer Level Chip Scale Package</td>
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</tbody>
</table>

3 Scope

This application note contains generic information about various fan-in and fan-out WLPs assembled at NXP and NXP’s assembly and test vendors. For more details about NXP
products, visit http://www.nxp.com or contact the appropriate product application team. Development efforts are required to optimize the board assembly process and application design per individual product requirements. Additionally, industry standards (such as IPC and JEDEC), and prevalent practices in the board assembly environment are good references.

4 Package description

4.1 Fan-In Wafer-Level Package (FI-WLP)

Fan-In Wafer-Level Package (FI-WLP) refers to the technology of packaging an integrated circuit at the wafer level, instead of the traditional process of assembling individual dies into packages after dicing them from a wafer. This technology is an extension of the wafer fab process and uses the traditional fab processes and tools. A redistribution layer is used to connect device I/Os to bump (ball) locations on top of the die surface. The bumps are arranged in an array pattern that is compatible with traditional circuit board assembly processes. The bumps provide the interconnection to the application. FI-WLP is a true Chip-Scale Package (CSP) technology, because the resulting package is the same size as the die. Wafer-Level Package (WLP) technology differs from other Ball-Grid Array (BGA) and laminate-based CSPs in that no bond wires or interposer connections are required. Figure 1 shows typical FI-WLPs.

![Figure 1. Typical FI-WLPs](image)

4.2 Fan-Out Wafer-Level Package (FO-WLP)

The Fan-Out Wafer-Level Package (FO-WLP) is an enhancement of standard WLPs, enabling a greater number of I/O connections. This package involves dicing chips from a silicon wafer, precisely positioning the known-good-die on a “reconstituted” or “carrier” wafer/panel, which is then molded. This is followed by making a redistribution layer on top of the die and the molded area, and then connecting bumps on top. Redistribution of I/Os to the mold compound regions outside the periphery of the die allows a greater number of I/O connections compared to an FI-WLP. Figure 2 shows typical FO-WLPs.
WLPs can have three distinct constructions:

- Repassivation
- Redistribution
- Direct bumping

**Repassivation:** The I/Os on the die are designed in such a way that they are already at the bump position. A repassivation layer is added on the bond pad, followed by the Under-Bump-Metallization (UBM) and the bump. See Figure 3.

**Redistribution:** The I/Os on the die are relocated to the correct bump locations with a redistribution layer. Two repassivation layers are used. See Figure 4.
Direct bumping: The UBM is deposited directly on the wafer passivation without a compliant layer in between. See Figure 5. This construction has limited use.

Notes:

- FO-WLP uses only redistribution type of construction.
- Some FI-WLPs are over-molded or have a back-side protection coating.

NXP offers WLP package in various sizes, thicknesses, I/O layouts and standard minimum ball pitches of 0.35, 0.40 and 0.50 mm. The physical outlines of a WLP depend on the actual die size. Refer to the applicable NXP package outline drawing for detailed dimensions and tolerances, which comply with JEDEC Publication 95, Design Guide 4.18 [1].

5 PCB design guidelines and requirements

Proper PCB footprint and stencil designs are critical to ensure high surface mount assembly yields, electrical and mechanical performance and reliability. The design starts with obtaining the correct package outline drawing, which is available at http://www.nxp.com. Figure 6 shows an example of a 4.045 x 3.16 mm 43 I/O WLP POD.
5.1 PCB pad design

WLP typically follows BGA package guidelines for PCB design. To allow for better PCB routing, some WLP products do not have fully populated arrays. PCB footprint design must match the package footprint.

NXP follows the generic requirements for Surface Mount Design and Land Pattern standards from the Institute for Printed Circuits (IPC), IPC-7351B [2].
5.1.1 PCB pad dimensions

Typically, PCB pad diameter is equal to the WLP pad diameter. Contact the NXP sales team to obtain WLP pad diameters. Table 2 contains suggested dimensions for the commonly used WLP pad diameters.

<table>
<thead>
<tr>
<th>Description</th>
<th>Bump pitch (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Cu pad shape</td>
<td>0.50</td>
</tr>
<tr>
<td>Circular</td>
<td>0.250</td>
</tr>
<tr>
<td>Circular</td>
<td>0.240</td>
</tr>
<tr>
<td>Circular</td>
<td>0.205</td>
</tr>
<tr>
<td>WLP pad diameter (mm)</td>
<td>0.250</td>
</tr>
<tr>
<td>PCB Cu pad diameter (mm ±0.025)</td>
<td>0.250</td>
</tr>
<tr>
<td>PCB solder resist diameter (mm ±0.025)</td>
<td>0.400</td>
</tr>
</tbody>
</table>

5.1.2 Pad surface finish

Most commonly used PCB finishes are compatible with FI-WLP and FO-WLP, including:
- Organic Solderability Preservative (OSP)
- Electroless Nickel Immersion Gold (ENIG), Au < 0.5 µm to avoid solder joint embrittlement.
- Immersion Sn
- Immersion Ag

Hot Air Solder Leveled (HASL) finish might have an uneven surface. Extra caution is required.

The PCB surface finish shelf life should be monitored to ensure that it has not expired. Surfaces should always be free of contaminants before PCB assembly.

5.1.3 Stencil thickness

The thickness and apertures of a stencil determine the amount of solder paste deposited on the PCB land. For ultra-small apertures required by small pitch WLP, it is preferred that the stencil be laser-cut stainless steel, electroformed cobalt, or hardened nickel-chromium, for repeatable solder paste deposition. Stencil coatings may be used for a more consistent paste release. Inspect stencil openings for dimensional accuracy, burrs and other quality issues prior to use.

When these stencil design requirements conflict with other required Surface Mount Technology (SMT) components in a mixed technology PCB assembly, a step-down stencil process may be utilized in compliance with IPC-7525 [3] design standards. Table 3 shows typical stencil aperture openings as a function of WLP bump pitch.

<table>
<thead>
<tr>
<th>Description</th>
<th>Bump pitch (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB stencil shape</td>
<td>0.50</td>
</tr>
<tr>
<td>Circular</td>
<td>0.340 / 125</td>
</tr>
<tr>
<td>PCB stencil aperture diameter (mm) / thickness (µm)</td>
<td>0.300 / 100</td>
</tr>
</tbody>
</table>
5.1.4 Solder mask layer

There are two types of PCB pads:

- Solder Mask Defined (SMD)
- Non-Solder Mask Defined (NSMD)

There are many factors influencing whether the PCB designer uses SMD or NSMD pads. NSMD pads are most commonly used for thermo-mechanical fatigue performance and SMD pads are used for improved drop test performance. Fillets are recommended where the trace connects to the Cu pad, especially with NSMD pads.

**Solder Mask Defined (SMD):** The exposed area of the SMD pad is smaller than the underlying copper and is defined by the solder mask opening.

The Pad diameter for SMD is typically a minimum of 0.07 to 0.1 mm larger than solder mask opening.

A key factor in picking the Cu diameter and solder mask diameter is PCB vendor capabilities. Inspection of delivered PCBs for solder mask registration is encouraged.

![Solder mask defined](image)

**Non-Solder Mask Defined (NSMD):** An NSMD pad has a solder mask opening larger than the copper pad.

The NSMD solder mask opening diameter is typically 0.12 to 0.15 mm larger than the pad size resulting in a 0.060 to 0.075 mm clearance between the copper land and solder mask (IPC-7351).

![Non-solder mask defined](image)

5.2 Via-in-pad structures

The need for via-in-pad structures is generally determined by the PCB design. Via-in-pad designs with fully or partially open vias typically result in voids and inconsistent
solder joints after reflow, which can lead to early failures. For via-in-pad structures, it is recommended to use filled vias that can be plated over with copper, so the resulting pad is planar. As with any PCB, the quality and experience of the vendor is very important with via-in-pad designs.

5.3 Clearance to vias and adjacent components

Clearance around the WLP component should account for the pick-and-place equipment size, placement accuracy and dimensions of the surrounding components. When underfill is applied, room should be available for dispensing nozzles. Placing a WLP near features such as PCB mounting holes, connectors or clamps is not recommended. This distance restriction is due to the increased amount of bending stress on the bumps and to avoid hitting those components during product placement for board assembly. Placement of WLPs near separation lanes of PCB panels should be avoided to minimize mechanical stress during the panel singulation process. When placing a WLP near another large component, care must be taken to prevent overheating of the WLP during the board assembly process.

Figure 9. Example of clearance during placement of WLP on PCB

6 Board assembly

6.1 Assembly process flow

Figure 10 shows a typical Surface Mount Technology (SMT) process flow.

Figure 10. SMT process flow
6.2 Solder paste

Solder paste is a homogenous mixture of fine metal alloy particles, flux, and viscosity modifiers to adjust printing and reflow properties. The main ingredients of solder paste are:

- **Solder alloy**
  NXP preference is to use lead-free solder paste, in line with environmental legislation (RoHS, ELV) [4]. A variety of lead-free alloys are available for PCB assembly, with different physical properties and melting temperatures. Common solder alloys use combinations of tin, silver, and copper: SnAg3Cu0.5 (SAC305), SnAg4Cu0.5 (SAC405), or SnAg3.8Cu0.7 (SAC387). Melting range is between 217 – 220 °C. The peak reflow temperature for these alloys is >235 °C.

- **Solder particles**
  A main component of the paste is the spherical powder made from the solder alloy. The solder pastes are classified by sphere size according to IPC standard J-STD-005 [5]. Smaller spheres allow higher printing resolution and smaller pitches. Solder paste suppliers can recommend a suitable flux for the selected solder paste. Type 5 solder paste is preferred for 350 µm or smaller pitches.

- **Flux**
  Flux is needed to remove surface oxidation, prevent oxidation during reflow and improve the wetting of the solder alloy. IPC standard J-STD-004 [6] classifies fluxes into three types:
  - Rosin-based flux
  - Water-soluble flux
  - No-clean flux
  Rosin based, and water-soluble fluxes require cleaning of the PCB after the reflow process. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.
  No-clean flux does not require cleaning, but normally a little residue remains on the PCB after soldering. In general, it is recommended to use a no-clean solder paste, because cleaning of flux residues from underneath the package is not feasible for WLP.

6.3 Component placement

The WLPs are comparatively small and require automated fine-pitch pick-and-place tools with an optical recognition system for precise placement on a PCB. Local fiducial markers are required on the board to support the vision systems.

Pick-and-place systems need to use minimal force to avoid damage to the WLP device. All vertical compression forces must be controlled and monitored. NXP recommends the use of low-force nozzles with compliant tip material. Use only a vacuum pencil with a compliant tip material whenever manual handling is required. Do not handle parts using tweezers.

Component placement accuracy studies are recommended to provide factual knowledge about compensations needed for WLP. NXP cannot anticipate the range of placement equipment and settings for package placement and, therefore, is unable to make a generic recommendation on how to compensate for WLP interchangeability.
6.4 Soldering

The soldering oven temperature profile is the most important control in reflow soldering. This temperature must be fine-tuned to establish a robust process. The profile parameters depend upon the solder paste and alloy used. The actual reflow temperature settings need to be determined by the end user, based on thermal loading effects and the recommendations from solder paste manufacturers. While profiling, the temperature of the package top surface shall be monitored, to validate that the peak package body temperature \( T_P \) does not exceed the MSL classification of individual devices. See IPC/JEDEC J-STD020 [7].

![Typical reflow profile for lead-free SAC solder](aaa-014105)

Figure 11. Typical reflow profile for lead-free SAC solder

Figure 11 shows a typical time/temperature profile for reflow soldering with lead-free SAC solder alloys using a multizone reflow oven.

The reflow profile is divided into four stages:

1. **Ramp-up to Soak**
   The printed circuit board should be heated evenly to avoid overheating of components. Volatile solvents in the solder paste start to outgas during ramp-up. A temperature increase that is too fast could cause solder balling. The maximum ramp-up rate shall not exceed 3 °C/second, to avoid overstressing the package.

2. **Preheat and Soak**
   The PCB assembly is typically held at 150 to 180 °C for 60 to 120 seconds during thermal soak. The time and temperature of the thermal soak are recommended by the paste supplier, depending on the flux type. The volatiles in the solder paste are removed and the flux is activated during this process to reduce oxides from the pads and spheres.

3. **Ramp-up and reflow**
   The PCB assembly is uniformly heated above the liquidous temperature of the solder alloy. The maximum ramp-up rate shall not exceed 3 °C/second to avoid overstressing the package. The recommended peak reflow temperature for SAC alloys shall be >235 °C. The period above the liquidous temperature \( (T_L) \) shall be long enough to allow the liquid solder to uniformly wet the pad and land surfaces and to form an intermetallic phase. A reflow time that is too long might lead to brittle solder joints and could cause damage to the board and components. The peak package body temperature \( (T_P) \) must not exceed 260 °C and the time above 255 °C must not exceed 30 seconds, depending on IPC/JEDEC classification.

4. **Cool down**
   Fast cool down prevents excess intermetallic formation and creates a fine grain structure of the solder alloy. The ramp-down rate can be faster than the ramp-up but
shall not exceed 6 °C/second to avoid overstress. Check with your board material supplier for a recommendation on maximum ramp down rates.

6.5 Inspection

The solder joints of WLP parts are formed underneath the package. Nondestructive optical and x-ray inspections are recommended to verify that there are no open or short circuits (bridging) after reflow soldering. When using x-ray, check if the device is sensitive to x-ray process.

Microsectioning is another method of inspecting solder joint quality during process optimization, but it is less suitable to inspection. Figure 12 shows the expected x-ray image of a soldered component.

Figure 12. X-ray image of a wafer-level package

7 Repair and rework procedure

7.1 Repairing

Repairing a single solder joint of a WLP is not recommended. The solder joints of terminals cannot be soldered in a controlled way.

7.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. The rework process for WLP devices is similar to typical BGA packages. This rework can be performed using the method described in this section. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

When performing the rework:

- In any rework, the PCB is heated. The thermal limits of the PCB and components must be followed.
- During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can damage the component and PCB. To prevent moisture induced failures, it is recommended that the PCB assembly and components
have had strict storage control with a controlled environment such as dry air or nitrogen. In addition, a pre-bake can help to remove the moisture.

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent packages.
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers and mounted components used); thus, the conditions must be set to correspond to the actual product and its mounted components.
- NXP follows industry-standard component-level qualification requirements, which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass.
- The removed WLP should be properly disposed of, so that it is not accidentally mixed with new components.

A typical rework flow process:

1. Tooling preparation
2. Component removal
3. Site preparation
4. Solder paste printing
5. Component placement
6. Reflow soldering
7. Inspection

Individual process steps for reworking a WLP are described in subsequent sections.

**Note:** NXP product quality guarantee / warranty does not apply to products that have been removed; thus, component reuse should be avoided.

### 7.2.1 Tooling preparation

Various rework systems for SMD are available on the market. In general, the rework station should have a split-light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing WLPs, a system should meet the requirements described as follows.

**Heating system**

The hot-air temperature and the air flow must be controlled so that the component is heated in a targeted and controlled manner. The heating should be appropriate for the package size and thermal mass. PCB preheating from the bottom side is recommended. Infrared heating can be applied for preheating of the PCB, but it should only augment the hot-air flow to the component side. Nitrogen can be used instead of air.

**Vision system**

The bottom side of the package, as well as the site on the PCB, should be observable. For precise alignment of the package to PCB, a split-light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.

**Moving and additional tools**

Placement equipment should have good accuracy. In addition, special vacuum tools might be required to remove solder residue from PCB pads.
7.2.2 Component removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB, because this might interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal for rework. See Section 10.5 "Returning WLP components to NXP".

Moisture removal (for FO-WLP)

The entire assembly must be baked to remove moisture at the maximum temperature the module can stand, up to 125°C. The bake should be for a minimum of 3 to 6 hours, longer if a temperature lower than 125 °C is used. The bake out will also remove moisture from adjacent components.

Temperature profile

During desoldering, ensure that the package peak temperature is not higher and that the temperature ramps are not steeper than the standard assembly reflow process. The temperature setting for the top heater and the bottom heater depends on the component rating. An air nozzle of correct size should be used to conduct the heat to the WLP component balls, so that a vacuum pick-up tool can properly remove the component.

Mechanical

Do not to apply high mechanical forces for removal. High forces can damage the component and/or the PCB, which might limit failure analysis of the package. It is especially necessary to determine if the components can be electrically tested directly after desoldering, or if these components must be preconditioned prior to testing. If the PCB is large, it is important to avoid bending the printed circuit material due to thermal stress. A bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed to allow heating of the entire printed circuit board. This procedure will raise work efficiency.

Reuse of removed semiconductor packages is not recommended.

7.2.3 Site preparation

After the component is removed, the PCB pads must be cleaned to remove solder residue. This step is necessary before placement of the new component. After applying flux to the pads, cleaning can be completed by using any of the following:

- Desoldering vacuum
- Solder sucker

Figure 13. Component removal process
• Solder wick braid

Remaining solder residue and projections can cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred via suction to the through-hole during reflow, which might cause an improper connection. A solvent might be necessary to clean the PCB of flux residue. A desoldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed the rating of PCB material, which can contribute to the pad peeling from the PCB. This is typically a manual operation where success is directly attributed to experience and skill.

Nonabrasive or soft bristle brushes should be used, because abrasive brushes, such as steel brushes, can contribute to bad solder joints.

7.2.4 Solder paste printing

Before placing a new component on the site, solder paste should be applied to each PCB pad, by printing or dispensing. A no-clean solder paste is recommended.

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening and pattern as the normal stencil are placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See Figure 14. The printed pad should be inspected, to ensure even and sufficient solder paste coverage, before component placement.

If neighboring parts are so close to the WLP components that the mini-stencil method is not an option, then apply solder paste carefully on each component pad using a paste dispensing system. The volume of solder paste must be controlled, to prevent shorting on the component and/or neighboring components. Preferably, the same type of solder paste should be used as was originally applied on the board.

![Figure 14. Mini stencil and mini squeegee](Images/figure14.jpg)

7.2.5 Component placement

The next step of the repair process is to place the new WLP component on the board. When remounting the component, consider using rework equipment that has good optical or video vision capability. A split-light system displays images of both package leads and PCB pads by superimposing two images. See Figure 15. WLP exhibits self-alignment in any direction, including x-axis shift, y-axis shift, and rotational misplacement.
7.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process. See Section 6.4 "Soldering". During soldering, the package peak temperature and temperature ramps must not exceed those of the normal assembly reflow process. Note that it might be necessary to dry bake the board before it is exposed to reflow temperatures a second time.

The PCB might need to be cleaned if it did not get cleaned in the rework process, or if the rework was not done using "no clean" solder flux.

7.2.7 Inspection

Nondestructive optical and x-ray inspections are recommended to verify that there are no open or short circuits (bridging) after soldering. See Section 6.5 "Inspection".

8 Board level reliability

8.1 Board level reliability testing

Board Level Reliability (BLR) testing is performed to determine a measure of board-level reliability when exposed to thermal cycling. There are several different names for BLR, including:

- Second-level reliability (2nd-level reliability)
- Solder Joint Reliability (SJR)
- Temperature Cycling on Board (TCoB)

Information provided here is based on tests performed by NXP on WLP devices using a daisy chain ball grid array configuration. BLR temperature cycling conditions may vary widely, depending on the application and specific user. It is recommended that users run this test using production surface-mount process and board design to develop application specific information.

- Typically, board level temperature cycling tests are performed according to JEDEC condition G (−40 °C to 125 °C).
The board-level reliability test results are provided per product due to specific dependence on dimensions, such as array size and pitch.

Samples of WLP in daisy chain format are used to study the Board Level Reliability. BGA pairs were routed in the WLP RDL layer, with a complementary pattern designed on the test PCB to provide one electrical circuit (net) through the package.

8.2 Board level reliability results

To get results from NXP board level reliability tests, contact the NXP sales team.

8.3 Underfill

Underfilling a WLP can significantly increase board level reliability. However, care must be taken in selection of underfill material. Interaction of CTE values of an underfill and PCB materials can result in worse BLR performance than without underfill. Underfill might also influence electrical performance of the product. A careful assessment is advised. The storage and use conditions, as defined by the underfill supplier, should be followed.

9 Package thermal characteristics

9.1 General thermal performance

Thermal ratings of the individual products are usually given in the NXP product data sheets as appropriate. Product data sheets are available at http://www.nxp.com. More detailed thermal properties may be requested by customers.

Because the thermal performance of the package in the final application depends on many factors, such as board design, power dissipation of other components on the same board and ambient temperature, the thermal package properties provided by NXP are only for reference. In applications where the thermal performance is critical, NXP recommends running application-specific thermal calculations in the design phase to confirm the onboard thermal performance.

9.2 Package thermal characteristics

Die junction temperature (Tj) is a function of:

- Die size
- On-chip power dissipation
- Package design and materials
- Ambient temperature
- Air flow
- Power dissipation of other components on the board.

Additional factors to be considered in PCB design and thermal rating in the final application include:

- PCB design parameters
  - Metal density of PCB traces
  - Via size
  - Number of thermal vias
  - Wall thickness of thermal vias
– Quality and size of PCB solder joints
- Solder joint parameters
– Effective PCB pad size
– Potential solder voiding in the thermal path solder joints which might reduce the effective solder area

9.3 Package thermal properties - definition

The thermal performance of a WLP is typically specified on a four-layer board (2s2p) per JEDEC JESD51-7 [8] as $R_{\theta JA}$ and $\Psi_{JT}$ under natural convection (still air) conditions per JEDEC JESD51-2 [9].

9.3.1 $R_{\theta JA}$: Theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) [9] is a one-dimensional value measuring the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air condition. The heat generated on the die surface reaches the immediate environment along two paths:
- Convection and radiation off the exposed surface of the package
- Conduction into and through the test board followed by convection and radiation off the exposed board surfaces

9.3.2 $\Psi_{JT}$ (Psi JT): Junction-to-package top

Junction-to-Package top (Psi JT or $\Psi_{JT}$) indicates the temperature difference between package top and the junction temperature, optionally measured in still air condition (per JEDEC JESD51-2) [9] or forced convection environment (per JEDEC JESD51-6) [10]. Users can use the $\Psi_{JT}$ (Psi-junction-top) value to estimate the component junction temperature in their application by measuring temperature on top of the WLP in the application environment using a thermocouple or an infrared camera (per JEDEC JESD51-12) [11]. $\Psi_{JT}$ must not be confused with the parameter $R_{\theta JC}$, which is the thermal resistance from the device junction to the external surface of the package while the package surface is held at a constant temperature.

9.4 Package thermal properties

Table 4 shows an example of the thermal characteristics typically shown in an NXP product data sheet. The example applies to a 5.3 x 5.3 mm package with 120 I/Os in the WLP configurations.

<table>
<thead>
<tr>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to ambient, natural convection$^{[1][2][3]}$</td>
<td>Four-layer board (2s2p)</td>
<td>$R_{\theta JA}$</td>
</tr>
<tr>
<td>Junction to package top$^{[4]}$</td>
<td>Natural convection</td>
<td>$\Psi_{JT}$</td>
</tr>
</tbody>
</table>

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Per JEDEC JESD51-7 [8].


[4] Thermal correlation parameter from the die to the top of the package per JEDEC JESD51-2 [9].
10 Package handling

10.1 Handling of ESD sensitive devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic-Discharge-Sensitive devices (ESDS), so proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs and components. Comprehensive ESD controls to protect ESDS during handling and processing should be considered. The following industry standards describe detailed requirements of proper ESD controls. NXP recommends meeting the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

JEDEC JESD625: Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices [12]

IEC-61340-5-1: Protection of electronic devices from electrostatic phenomena - General requirements [13]

10.2 Handling of moisture-sensitive surface mount devices

Moisture from atmospheric humidity enters permeable plastic package materials by diffusion. When the package is exposed to rapid temperature rise and high temperature during reflow solder process, moisture expansion, materials mismatch, and material interface degradation can result in package delamination and/or cracking of critical interfaces. This is referred to as the popcorn effect.

IPC/JEDEC's J-STD-033 [14] defines the Moisture Sensitivity Level (MSL), which is a measure of the sensitivity of a component to ambient humidity. This parameter indicates permissible floor life of the component, its storage conditions, and handling precautions after the original container has been opened. Components must be mounted and reflowed within the allowable time (floor life out of the bag). Also, during the reflow process, the component temperature must not exceed the specified maximum peak body temperature.

**Note:** The default MSL for WLPs is 1. However, FO-WLPs are moisture-sensitive surface mount devices requiring proper precautions for handling, packing, shipping and use. Check the MSL rating of the component and follow precautions specified in this section for moisture-sensitive components.

Before shipping, moisture-sensitive components are dried, vacuum sealed and packed with a desiccant and a moisture indicator card in a Moisture Barrier Bag (MBB). Remove the moisture-sensitive components only immediately prior to assembly onto the PCB. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of bag opening. If components have been exposed to ambient air for longer than the specified time, or if the humidity indicator card indicates too much moisture after opening an MBB, then the components are required to be rebaked prior to the assembly process. Refer to IPC/JEDEC J-STD-033 [14] for the baking procedure.

A label on the moisture barrier bag indicates that it contains moisture-sensitive components. See Figure 16. The moisture sensitivity caution label contains information about the moisture sensitivity level (MSL) and maximum allowed peak body temperature of the products. The same information is shown on the barcode labels of the shipping box and reels. See Figure 17.
10.3 Handling of WLPs

The small, near-chip-scale size of WLPs enables higher integration on board level compared to leaded-type packages. Care must be taken with WLPs to avoid overstressing the parts during handling, such as pick-and-place processes or testing. Mechanical properties of the individual products strongly depend on product configuration. To get detailed information on a specific product, contact the NXP sales team.
10.4 Packing of devices

WLP devices are packed in tape-and-reel configurations and are dry packed for transportation and storage. Packing media are designed to protect devices from electrical, mechanical and chemical damages, as well as moisture absorption.

Proper handling and storage of dry packs are recommended. Improper handling and storage of dry packs will increase quality and reliability risks. Refrain from the following:

- Dropping dry packs
- Storage exceeding 40 °C/90 %RH environment
- Excessive stacking of dry packs

Detailed packing information can be found on NXP’s website. Follow the steps described in Section 10.3 "Handling of WLPs”.

NXP complies with the following Environmental Standards Conformance guidelines/directives:

- ISPM 15, Guidelines for Regulating Wood Packaging Material in International Trade [15].

10.4.1 Tape-and-reel

Tape-and-reel specifications can be found in application note AN4613 Analog and Power Management Tape and Reel Specification [17].

10.5 Returning WLP components to NXP

If WLPs are sent back to NXP for analysis purposes, return the entire assembly. Removing the WLPs from the PCB damages the solder balls and, most probably, the component. In case the entire assembly cannot be sent, cut the part around the device as large as possible. During sawing, the PCB-clamps should not be placed on top of the WLP. Excessive clamping force should be avoided, because it can cause the PCB to warp and damage the device. Follow the rework guidelines for WLP removal. See Section 7.2 "Reworking”.

For shipment of devices on PCBs, pack between two electrostatic discharge hard foam materials and tape along all edges. Demounted WLPs are best packed in a gel pack. Both WLPs on PCB and demounted WLPs should be packed in ESD bags and, preferably, in dry pack for shipping.

11 References

[1] JEDEC PUBLICATION 95 DESIGN GUIDE 4.18, Wafer Level Ball Grid Arrays, (WLBGA)
[5] IPC, J-STD-005, Requirements for Soldering Pastes
Wafer-level chip-scale package (fan-in WLP and fan-out WLP)

12 Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>v.8</td>
<td>20180710</td>
<td>Combined AN3846 and AN10439 and obsoleted AN3846. Added fan-out WLP.</td>
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<tr>
<td>v.7</td>
<td>20161031</td>
<td>adapted Section 4 (Table 2 modified, Table 2 removed)</td>
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<td>v.6</td>
<td>20150824</td>
<td>modified Table 2</td>
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<td>v.5</td>
<td>20150528</td>
<td>revision</td>
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<tr>
<td>v.4</td>
<td>20140825</td>
<td>revision</td>
</tr>
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<td>v.3</td>
<td>20071017</td>
<td>internal release; adapted to NXP house style</td>
</tr>
<tr>
<td>v.2</td>
<td>20060713</td>
<td>internal release; minor changes</td>
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<tr>
<td>v.1</td>
<td>20060310</td>
<td>initial version (internal release)</td>
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