AN10608

XTAL1 clock and $\overline{IOW}$ pulse synchronization issue

Rev. 01 — 23 April 2007 **Application note**

Document information

Info	Content
Keywords	non-B, 16C UART, transmitter error
Abstract	Non-B 16C UARTs might occasionally send an extra character from the transmit FIFO. This application note discusses the root cause, impact to customer and offers a work-around solution.

Revision history

Rev	Date	Description
01	20070423	application note; initial version

Contact information

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1. Introduction

Occasionally, the non-B revision UART transmitter sends an extra incorrect character that consists of part of the previous transmitted character. All subsequent characters from the transmit FIFO will also be transmitted wrongly.

2. Explanation of root cause

There is an internal signal that indicates the availability of a new character in the transmitter FIFO, and that signal is clocked by the processor $\overline{IOW}$ pulse. In the non-B UART design, that signal is not synchronized to the XTAL1 clock before it is being used in the transmitter state machine; there exists a race condition between the XTAL1 clock and the $\overline{IOW}$ pulse. If the $\overline{IOW}$ pulse happens during the time the state machine's input flip-flops are being switched, then the state machine will get into the wrong state. The state machine should be in the start state, but it wrongly jumps to the transmit bit 4^{th} state. The transmitter then wrongly sends out the last four bits of the old character without a start bit, and the rest of the characters in the transmit FIFO.

3. Impact to customer

Once the transmitter gets into the condition described above, transmitted characters will be erroneously received by the receiver.

4. Work-around

1. Replace the non-B revision with the B revision devices.
2. The hardware work-around for this issue requires an external flip-flop to synchronize the $\overline{IOW}$ pulse to the XTAL1 clock. XTAL1 is used to clock the D flip-flop. The $\overline{IOW}$ signal from the processor is connected to the D input of the flip-flop, and the Q output of the D flip-flop is connected to the $\overline{IOW}$ input of the UART. See Figure 1 for the circuit hook-up example.

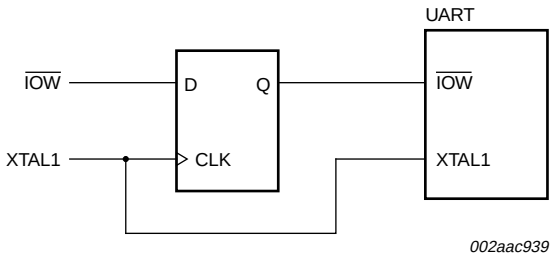

Fig 1. Circuit hook-up

We are not aware of any software work-around for this particular issue.

5. Conclusion

All 16C UART non-B versions are effected by this issue, and the issue has been fixed on the revision B. We advise that customers to switch from the non-B revision to revision B as soon as possible when the design allowed. Please see application notes *AN10257* and *AN10312* for the detailed explanation of the differences between the non-B and the B revisions.

6. Abbreviations

Table 1. Abbreviations

Acronym	Description
FIFO	First In, First Out
UART	Universal Asynchronous Receiver/Transmitter

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