AN10631

Possibility of erroneous transmitter interrupt in 16C 4-channel UARTs

Rev. 01 — 18 June 2007

Application note

Document information

Info	Content
Keywords	SC16C654B, SC16C654DB, SC16C754B
Abstract	The SC16C654B/654D/754 might occasionally generate an erroneous transmitter interrupt. This application note discusses the root cause, impact to customer and offers a work-around solution.



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Revision history

Rev	Date	Description
01	20070618	Application note; initial version.

Contact information

For additional information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

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Application note

1. Introduction

There is the possibility of erroneous transmitter interrupt in 16C 4-channel UARTs. The issue described below affects all SC16C654B/654DB/754B parts.

2. Description of the issue

In FIFO mode, the transmit ready (TxRDY) interrupt is asserted when the transmit FIFO (TxFIFO) is below the trigger level and while a batch of data is being loaded to the TxFIFO, an erroneous TxRDY interrupt might occur. This erroneous interrupt causes the interrupt service routine to reload another batch of data to the TxFIFO.

3. Detailed description

In FIFO mode, the TxRDY interrupt is set based on the Tx trigger level, so when the Tx FIFO level is below its trigger level, the TxRDY interrupt will be asserted and the TxRDY interrupt will be de-asserted when the Tx FIFO level is above its trigger level. If these randomized conditions (set and reset TxRDY interrupt) collide within one clock cycle, an erroneous TxRDY interrupt might occur.

4. Impact to customer

This erroneous TxRDY interrupt causes the interrupt service routine to reload another batch of data to the TxFIFO.

5. Work-around

Using hardware/software flow control will avoid this erroneous TxRDY interrupt.

6. Conclusion

It is recommended to use a hardware/software flow control to avoid the TxFIFO being reloaded due to this erroneous TxRDY interrupt.

7. Abbreviations

Table 1.	Abbreviations	
Acronym	Description	
FIFO	First In, First Out	
UART	Universal Asynchronous Receiver Transmitter	

8. Legal information

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Document identifier: AN10631_1