

# AN10777

## LPC32x0 power supply design examples

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Application note

### Document information

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<b>Abstract</b>	Provide an LPC32X0 power supply examples for the system designer, which takes advantage of the power saving features built in to the LPC32X0 microcontroller.

**Revision history**

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## 1. Introduction

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### 1.1 Purpose

Provide a power supply example for the system designer, which takes advantage of the power saving features built in to the LPC32X0 microcontroller.

### 1.2 LPC32X0 Microcontroller Description

The LPC32X0 family of embedded microcontrollers is targeted for low power, high performance applications. It has an ARM ARM926EJ-S CPU with a large set of standard peripherals including USB On-The-Go, NAND Flash interface, Ethernet MAC, LCD controller that supports STN and TFT panels, seven UARTs, two I<sup>2</sup>C interfaces, two SPI/SSP ports, two I<sup>2</sup>S interfaces, two single output PWMs, a motor control PWM, four general purpose timers with capture inputs and compare outputs, a Secure Digital (SD) interface, a 10-bit A/D converter with a touch screen sense option, and an external bus interface that supports SDR and DDR SDRAM as well as static devices.

### 1.3 LPC32X0 Power Domain Flexibility

In today's complex embedded microcontroller designs not all peripheral interfaces and memories operate over the same power supply voltage range. For this reason and for overall system power savings, there is a need to provide system designers with the flexibility to support a wide range of IO voltage levels. For example, a low power application may use mobile SDR or DDR synchronous dynamic memories requiring 1.8V power while many other peripheral interfaces may require 2.8 - 3.3 volts, while a battery backed RTC may require yet another voltage. The LPC32X0 provides flexible power domains for these situations in the following ways:

1. The LPC32X0 IO buffers operate over the voltage range between 1.7 to 3.6 volts.
2. The External Memory Controller pins are on an independent IO power domain.
3. Peripheral, RTC and Analog pins are distributed across independent power domains.

## 2. LPC32X0 Power Domains

The LPC32X0 has several power domains to provide the flexibility discussed in the previous section. A description of the power domains is covered in this section and [Fig 1](#) shows the LPC32X0 power domains in one schematic symbol.

### 2.1 CORE power domains

#### 2.1.1 VDD\_CORE

This is the LPC32X0 core power domain. It may be operated between 0.9 to 1.39 volts. The LPC32x0 maximum Run mode ARM\_CLK and HCLK frequency have been specified by three classes of operation, defined by the minimum required VDD\_CORE voltage, as shown in [Table 1](#).

**Table 1. LPC32x0 maximum clock rate over VDD\_CORE voltage**

Operation Class	Max ARM_CLK	Max HCLK	Min VDD_Core	Nom VDD_Core
Full performance	266MHz	133MHz	1.31V	1.35V
Normal performance	208MHz	104MHz	1.1V	1.2V
Reduced power	14MHz	14MHz	0.9V	0.9V

#### 2.1.2 VDD\_COREFXD

The VDD\_COREFXD pins provide the Core Supply to digital side of the analog blocks and must be 1.2 volts nominal regardless of the VDD\_CORE voltage.

#### 2.1.3 Other Core power domains

The VDD\_PLL397, VDD\_PLLHCLK, VDD\_PLUSB and VDD\_FUSE power domains shall all be connected to 1.2 volts nominal, the same as VDD\_COREFXD.

### 2.2 RTC power domain

The VDD\_RTC, VDD\_RTCCORE and VDD\_RTCOSC may be operated between 0.9 to 1.39V. For the lowest possible power down mode where the RTC must remain active while all other LPC32X0 power domains are shut down, this supply domain should be connected to a battery backed up power source.

### 2.3 Analog to Digital Converter power domain

The VDD\_AD power domain may be operated between 2.7 and 3.6V. Typically, this would be sourced by the power supply sourcing the highest voltage to the peripheral IO power domain(s). An LC filter is recommended to minimize noise from the digital IO from being applied to the VDD\_AD power domain.

### 2.4 External Memory Controller interface power domain

The VDD EMC power domain controls all the IO pins associated with the external memory interface, including SDR or DDR SDRAM, static memories and other board level peripherals that are treated as memory mapped static memory devices. This power domain operates over two distinct voltage ranges, either 1.7 - 1.95V or 2.3 – 3.6V. The voltage range used is dependent on the SDR or DDR SDRAM memory chosen for the

system. Mobile SDR or DDR memories, with 1.8V VDD power supply, are well suited for lowest power systems.

### 2.4.1 Supply voltage Impact on performance

The slew rate of the EMC IO pins can be set fast or slow by register settings. The slew rate can be set independent of the VDD\_EMC voltage, however the intent is the IO buffer performance with a VDD\_EMC of 1.8 volts and slew rate set to fast is similar to the buffer performance with a VDD\_EMC of 2.8V and slew rate set to slow. For additional details see the User Manual for SDRAM Clock Control Register bits SDRAM\_PIN\_SPEEDx (where x = 1,2 or 3).

## 2.5 Peripheral Interface power domains

The peripheral interface power domains VDD\_IOA, VDD\_IOB and VDD\_IOD may be operated in the voltage range of 1.7 to 3.6V. The VDD\_IOC power domain operates over two distinct voltage ranges, either 1.7 - 1.95V or 2.3 – 3.6V. Each peripheral domain may be operated at a voltage independent of the other domains with a few exceptions, as listed in Section 2.5.1. However in doing so it is extremely important for the system designer to be aware of which LPC32X0 pins are associated with each peripheral power domain to ensure that all LPC32X0 pins going to the same external board level device share the same IO voltage level. This can be especially important when GPIO pins go to a standard interface device like an Audio Codec or IO port such as SD/MMC, or the I2C interface goes to multiple devices. The datasheet chapter on Pinning Information provides details of which peripheral IO power domain is associated with each LPC32X0 signal pin.

### 2.5.1 Peripheral interface Power Domain limitation

There are two design considerations to mixing voltages on the peripheral power domains. They are as follows:

1. Ethernet Interface - The VDD\_IOD and VDD\_IOB power domains must be powered by the same voltage when the LPC32X0 Ethernet MAC is configured to operate in the MII mode. This is due to MII Ethernet interface having signal pins powered from a mix of VDD\_IOD and VDD\_IOB power domains. Most Ethernet PHY chips operate with a 3.3V IO voltage, requiring VDD\_IOD and VDD\_IOB to also be 3.3V. When the Ethernet MAC is operated in the reduced interface pin mode (RMII), the subset of Ethernet signal pins used are all powered by VDD\_IOD, thereby making it acceptable to have VDD\_IOD and VDD\_IOB powered from different voltages.
2. UART3 – The VDD\_IOA and VDD\_IOD must be powered by the same voltage source whenever UART3 TX and RX are used with DTR, CTS, DSR hardware flow control or they share an RS-232 transceiver with any other UART. This is due to U3\_RX and U3\_TX pins being powered by VDD\_IOD, while all other UART pins are powered by VDD\_IOA.

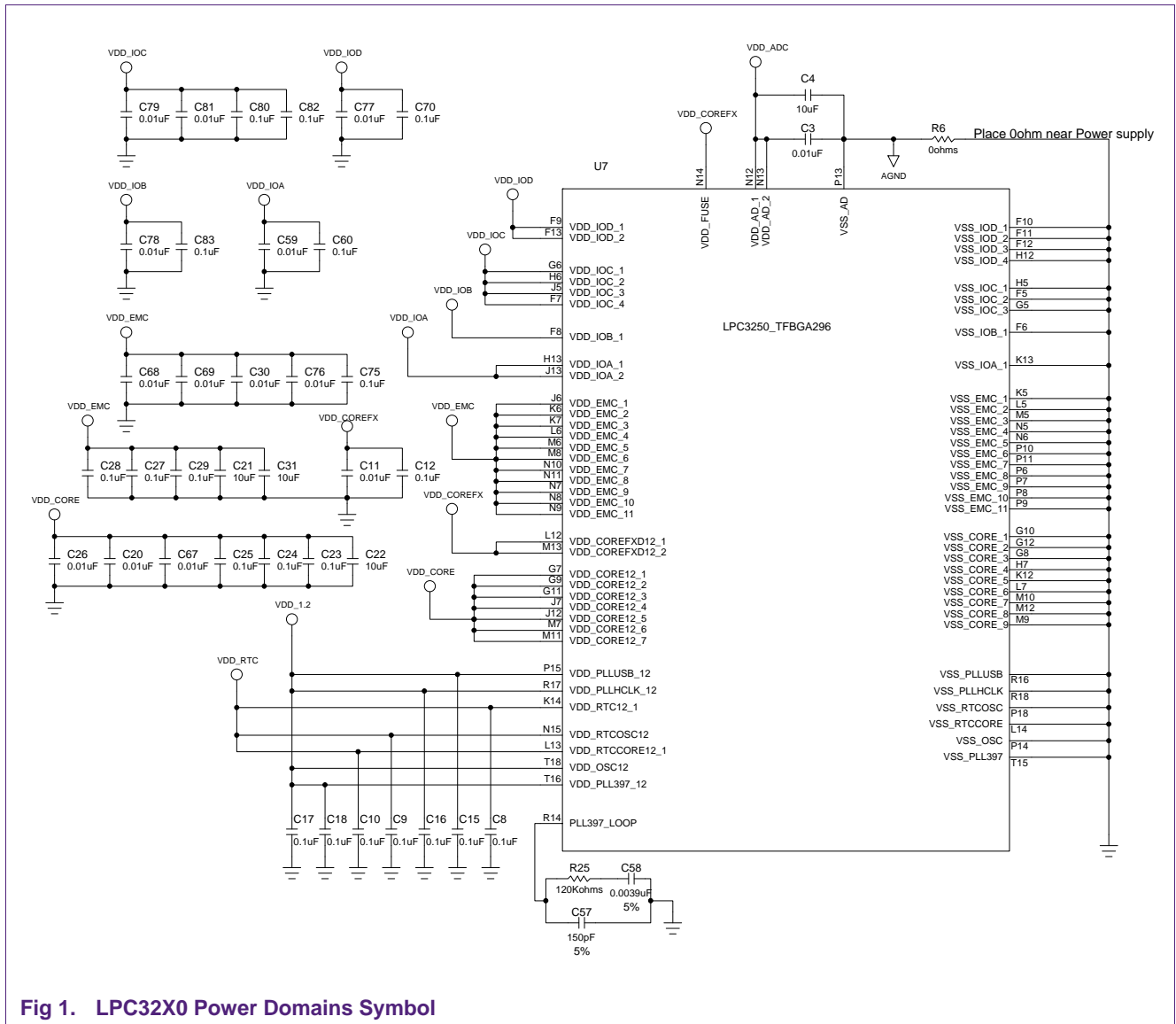


Fig 1. LPC32X0 Power Domains Symbol

### 3. LPC32X0 Minimal power supply design

It is possible to design a LPC32X0 board with as few as two power supply voltages; a 1.2 volt supply for the LPC32X0 core and RTC power domains, and a 3.3 volt supply for the EMC, peripheral IO, and ADC power domains. This would not be the most power efficient design but would reduce the number of items on the bill of material. The example in Fig 2 uses a MP2109DQ which has two switching regulators in a single package.

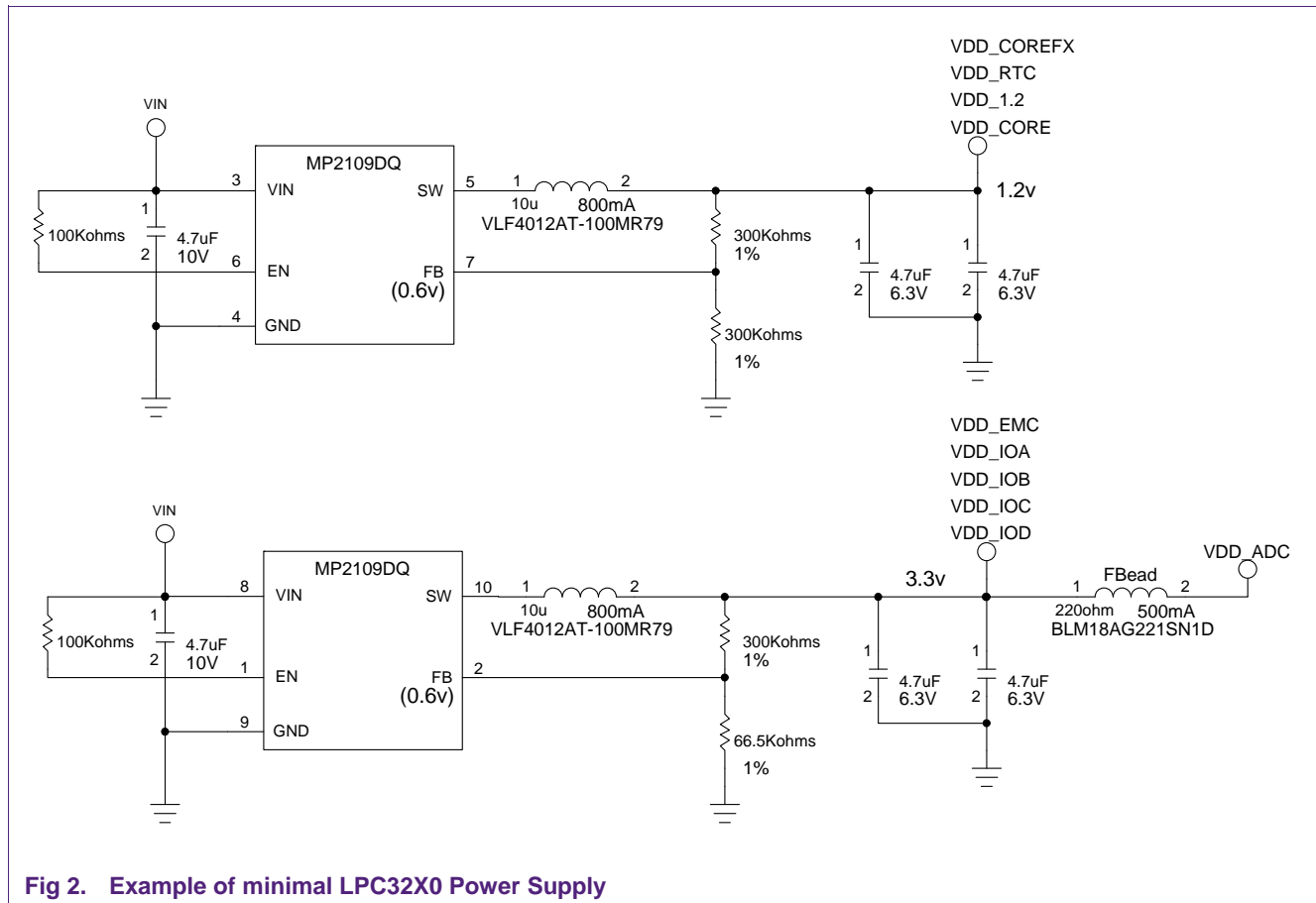


Fig 2. Example of minimal LPC32X0 Power Supply

### 4. LPC32X0 power supply designs for power savings

Dynamic power is calculated by the product of the frequency x capacitance x voltage<sup>2</sup>. Notice that a doubling of voltage causes a four fold increase in power. For IO power domains reducing power is a function of keeping the IO signal trace lengths short (minimize capacitance), setting clocks for the AHB and peripheral clocks as slow as possible for the desired performance, and using external components that operate with 1.8 VDD power. Since reducing capacitance in the LPC32X0 CORE is not possible at the board level, reducing dynamic power in the VDD\_CORE is done by reducing the CPU and AHB clock speed and reducing the VDD\_CORE voltage. A more typical power supply design for an LPC32X0 embedded application would employ several power saving approaches. Powering the RTC from a battery allows all other core and IO power

to be powered off when the product is shut down while still keeping accurate time with the RTC. Other power saving techniques include using 1.8v mobile SDRAMs and FLASH memories, and dynamically adjusting the LPC32X0 VDD\_CORE voltage between 0.9 to 1.39 volts depending on the required ARM processor speed and AHB bus speed required by the application. Details of using an I2C controlled switching regulator for the purpose of varying the VDD\_CORE supply will be shown later in this section.

#### 4.1 LPC32X0 Software Power Control Modes

The LPC32x0 family supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct Run mode, and Stop mode.

Run mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the 13MHz main oscillator frequency. In Run mode, the CPU is typically operated from a high frequency clock supplied by an on-chip PLL and can run at up to 266 MHz and the AHB bus can run at up to 133 MHz.

At times when the application does not require the performance of Run mode the PLL may be bypassed and the CPU clocked at the main oscillator rate. This is called Direct Run mode and saves power by reducing the CPU and AHB bus rates. Direct Run mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct Run mode is the default mode following chip reset.

Stop mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block, while allowing many peripheral functions to restart CPU activity.

#### 4.2 Using the LPC32X0 Highcore pin to control VDD\_CORE voltage

The HIGHCORE output pin may be used as a low cost method to save additional power during STOP Mode or low frequency operation by signaling external circuitry to lower the core supply voltage. If any on-chip clocks are running above 14 MHz, nominal core supply voltage must be supplied. If all on-chip clocks are running at or below 14 MHz (DIRECT RUN Mode), or during STOP Mode, the core supply voltage may be lowered to 0.9 volts. This can be controlled automatically in hardware if the pin HIGHCORE/LCD[17] is not being used for the alternate function LCD[17]. The HIGHCORE output pin is driven low after reset. A low indicates to an external power supply controller that nominal core voltage (1.2V) is needed. If software writes a 0 to the PWR\_CTRL[1] bit, the HIGHCORE pin will drive high during STOP mode. The external power supply controller may then cause the core voltage be lowered to 0.9 volts. After exit from STOP mode, the core voltage needs to stabilize to the nominal voltage before the ARM can change to higher frequency operation, if needed. The power supply must ensure that any over/under swing on the core voltage is within the operating limits. The USB clock cannot be operated in the low core voltage mode. It is important that software reads PWR\_CTRL[0] after exiting from STOP mode. If this bit is 1, it needs to be written to a 0 by software in order to guarantee the correct level on the HIGHCORE pin. In order to lower the operating voltage at low frequencies when not entering STOP Mode, software must control the value of the HIGHCORE pin. This is accomplished by writing a 1 to the PWR\_CTRL[1] bit, causing the value of the PWR\_CTRL[5] bit to appear on the HIGHCORE pin. When changing power supply voltages, all operating clocks must be at 14 MHz or lower prior to reducing the core supply voltage and remain there until the core



supply voltage has stabilized at the nominal voltage. Only then can clock speeds exceed 14 MHz.

#### 4.2.1 Example Power Supply using HIGHCORE pin

By using a voltage regulator with a voltage feedback pin together with the LPC32x0 HIGHCORE pin the regulator's output can be automatically switched bi-modal between nominal voltage and 0.9 volts. The example in Fig 3 uses an MP2109DQ dc to dc switching regulator, which has a feedback pin input voltage threshold of 0.6V, and configured to supply a nominal VDD\_CORE voltage of 1.2V. When the HIGHCORE pin is low, Q1 will be in the off state resulting in R5 pulling the gate of Q2 to VIN, turning on Q2 which now shunts R3 to GND. The regulator output voltage is set by the equation  $Regulator\_out = 0.6 / (R2 / R1 + R2)$ ;  $Regulator\_out = 0.6 / (300k / 600k) = 1.2$ . When the LPC32X0 is placed in Stop mode the HIGHCORE pin goes high, causing Q1 to switch on and pull the gate of Q2 to GND. With Q2 in off state the regulator feedback voltage of 0.6V is developed across the combined series resistance of R2 and R3 and the regulator output voltage is set by the equation  $Regulator\_out = 0.6 / (R2 + R3 / R1 + R2 + R3)$ ; in this example is 0.9 volts. VIN is dependent on the input voltage requirement of the voltage regulator device used. In this example VIN must be in the range of 2.5 – 5V. This circuit works with other low cost voltage regulators, and N-Channel FETs with 1.5 volt Gate Threshold Voltage. Two 4.7uF capacitors are shown connected to the output voltage. These could be replaced with a single 10uF capacitor, but in the 0402 and 0603 package size two ceramic 4.7uF XR5 type can cost less than a single 10uF, and in parallel have lower ESR than a single capacitor.

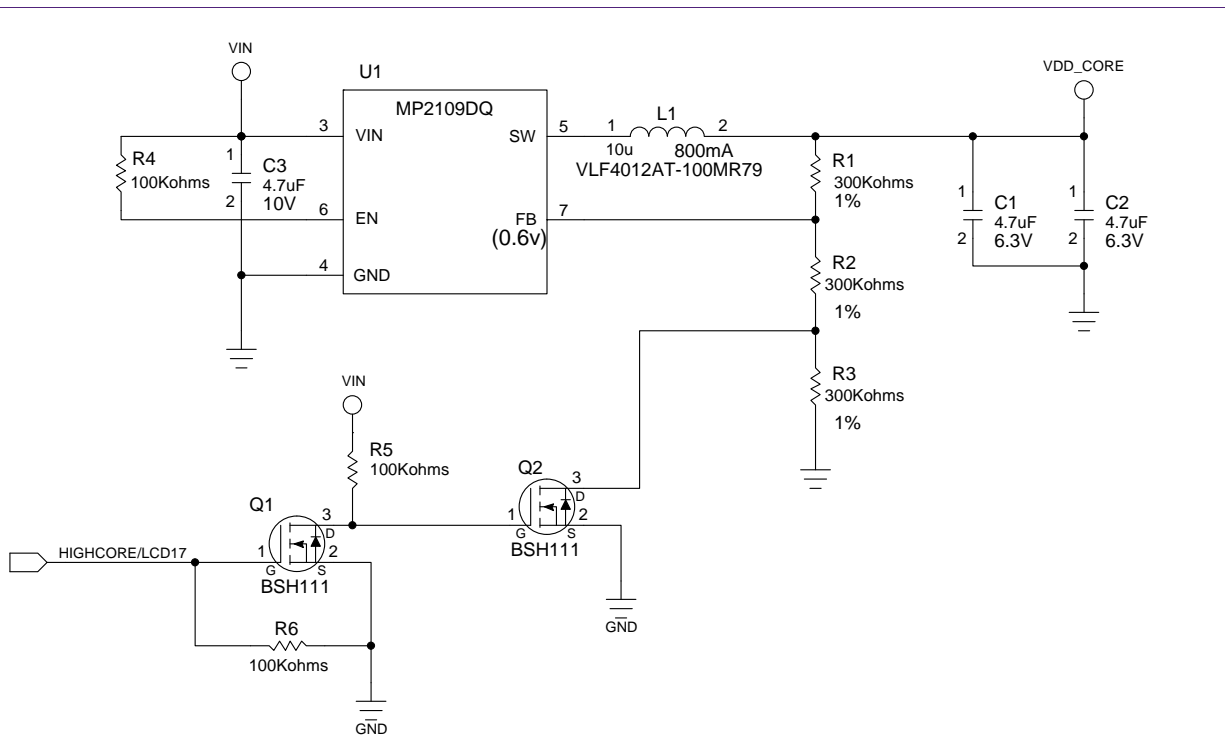


Fig 3. Example using HIGHCORE pin to switch VDD\_CORE bi-modal

### 4.3 I2C controlled variable VDD\_CORE Power Supply

Another power supply design with the potential for more power savings than using the HIGHCORE pin is to use a programmable output voltage regulator for the VDD\_CORE. For applications that do not require the maximum CPU / AHB clock rate of 266/133MHz at all times, additional power can be saved during Run mode by lowering the CPU clock rate and lowering the VDD\_CORE voltage to the 0.9V (clocks <= 14MHz) or 1.2V (208/104MHz) under software control.

The example shown in Fig 4 uses an LTC3447 I2C controlled voltage regulator for the VDD\_CORE power domain. The regulator uses external resistors to set the initial startup voltage. The LTC3447 feedback pin voltage threshold for this start-up option is 0.6V. In the example the resistors R1 and R2 are used to set the initial startup voltage of 1.2 on VDD\_CORE. After the regulator's voltage DAC is updated via the I2C, the buck regulator switches from external to internal feedback resistors. When there are no external resistors, the default start-up voltage is 1.38V. Using this type of power supply the software would be responsible for lowering the VDD\_CORE voltage to 0.9 as part of the routine entering Stop mode and to increase the voltage to the required nominal value after exiting the Stop mode.

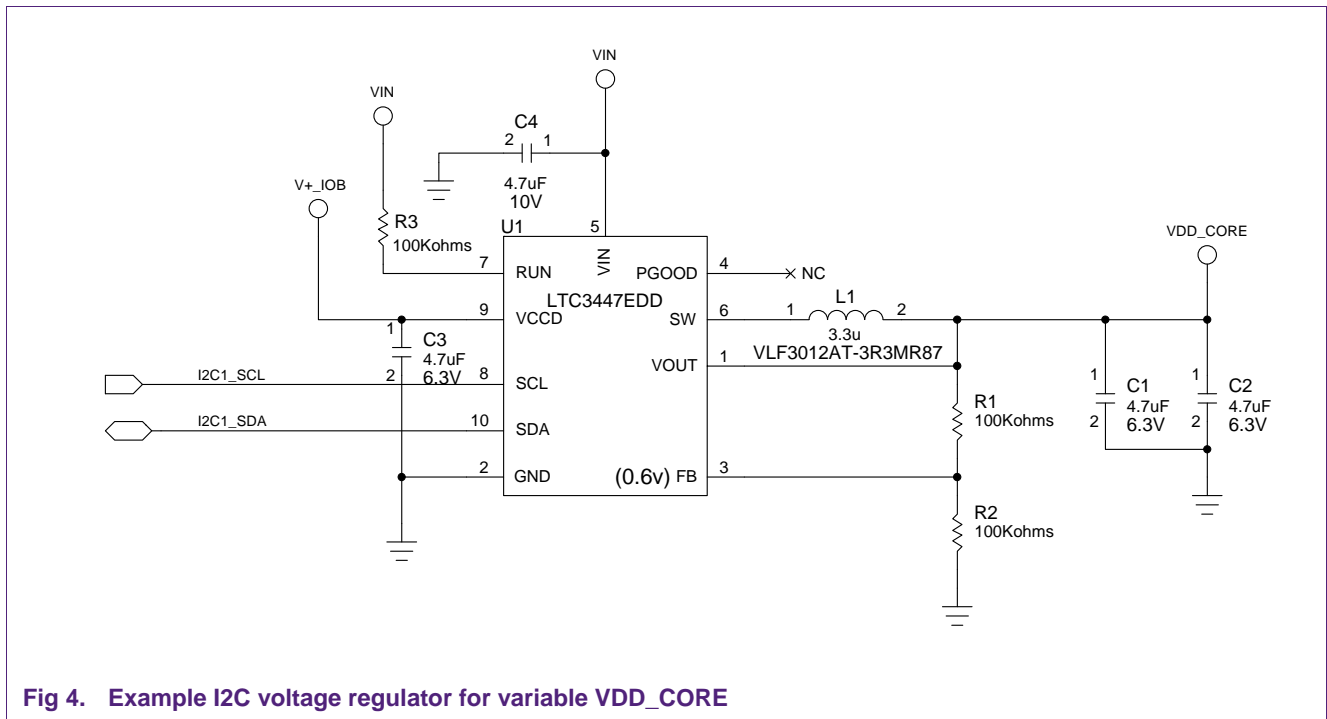


Fig 4. Example I2C voltage regulator for variable VDD\_CORE

## 4.4 Save power using the ONSW pin

For applications that do not require the ARM processor and other LPC32x0 peripheral functions for long periods of time, the biggest power savings come by using a battery backed power supply for the LPC32x0 Real-Time Clock (RTC), then under software control shutting off the LPC32x0 core and IO power supplies. The power supplies can be powered back on by using the RTC alarm to trigger the ONSW pin.

### 4.4.1 LPC32x0 RTC

The RTC has a special power domain independent of the rest of the chip and is designed both to be very low power and operate down to 0.9V (following a discharging battery). The RTC continues to operate even when all other LPC32x0 power domains have been powered off. The RTC generates a one-second tick from a dedicated 32 kHz crystal oscillator and uses 32-bit registers which should never need resetting because it takes 136 years to reach the maximum register count. The RTC has 32 words of SRAM that can be used to hold data between microcontroller power cycles. The RTC has two 32-bit match registers for setting alarms, either of which can generate an interrupt to the ARM processor or trigger the ONSW output pin. Before the ONSW pin can go active one of the Match ONSW control bits in the RTC Control register (RTC\_CTRL) must be written to 1 and the Key register (RTC\_KEY) must be written with the value 0xB5C13F27. The ONSW pin will go active (high level) for only one second, while the source RTC Match register equals the RTC Up Counter value.

### 4.4.2 Example hardware circuit using ONSW pin and on / off switch

An example circuit using the ONSW pin to turn on all of the LPC32x0 operating voltages, as a way to startup after power has been removed is shown in [Fig 5](#).

Features of the example circuit include:

- Circuit is disabled when main power source is initially applied
- Uses mechanical switch or ONSW pin to enable power supplies
- Software control to disable power supplies
- Both active high and active low power supply enable signals generated

In [Fig 5](#) example circuit, capacitor C2 ensures the flip-flop U1 comes up in a reset state after VIN is initially applied, keeping the power supplies disabled. The RC time constant of R2 x C2 needs to be at least as long as the ramp time of VIN to be effective. The power supplies are initially enabled when the mechanical on / off switch (S1) is moved from the off to on position clocking the flip-flop to the set state and enabling the power supplies. The flip-flop reset is driven by an LPC32x0 GPO pin, so that the power supplies are disabled by software control. This allows the software to perform whatever house keeping is necessary prior to shutting power off, including saving system specific state data in the RTC SRAM. The capacitor C1 acts as a filter to ensure the flip-flop is not reset by noise on the GPO while the LPC32x0 VDD\_CORE and VDD\_IO power supplies are ramping up. Once the RTC registers have been configured for a match alarm and the ONSW pin enabled, a subsequent RTC match event will drive the ONSW output high (for a maximum of 1 second), setting U1-Q output and enabling the power supplies. The NPN bipolar transistor Q3 is used to invert the ONSW output and voltage translate ONSW from the VDD\_RTC voltage level to the VIN level. A bipolar transistor is needed here because the logic high voltage level of 0.9 – 1.39V at the ONSW pin is not large enough to turn on most field effect transistors. VIN represents the main voltage source to the on-board power supplies, which could be from a battery or other DC power

source. For this example, VIN is limited to 5.5V by the flip-flop U1 VDD maximum specification.

Since the example circuit disables the power supplies under software control, Q2 is used to generate an interrupt to the LPC32x0 when the power switch is moved to the off state to request a power down. The software can also read the state of the power on / off switch to determine the source of the GPI interrupt.

By moving C2 to the U1 preset input, the flip-flop will come up set when VIN power is initially applied, enabling the other power supplies too.

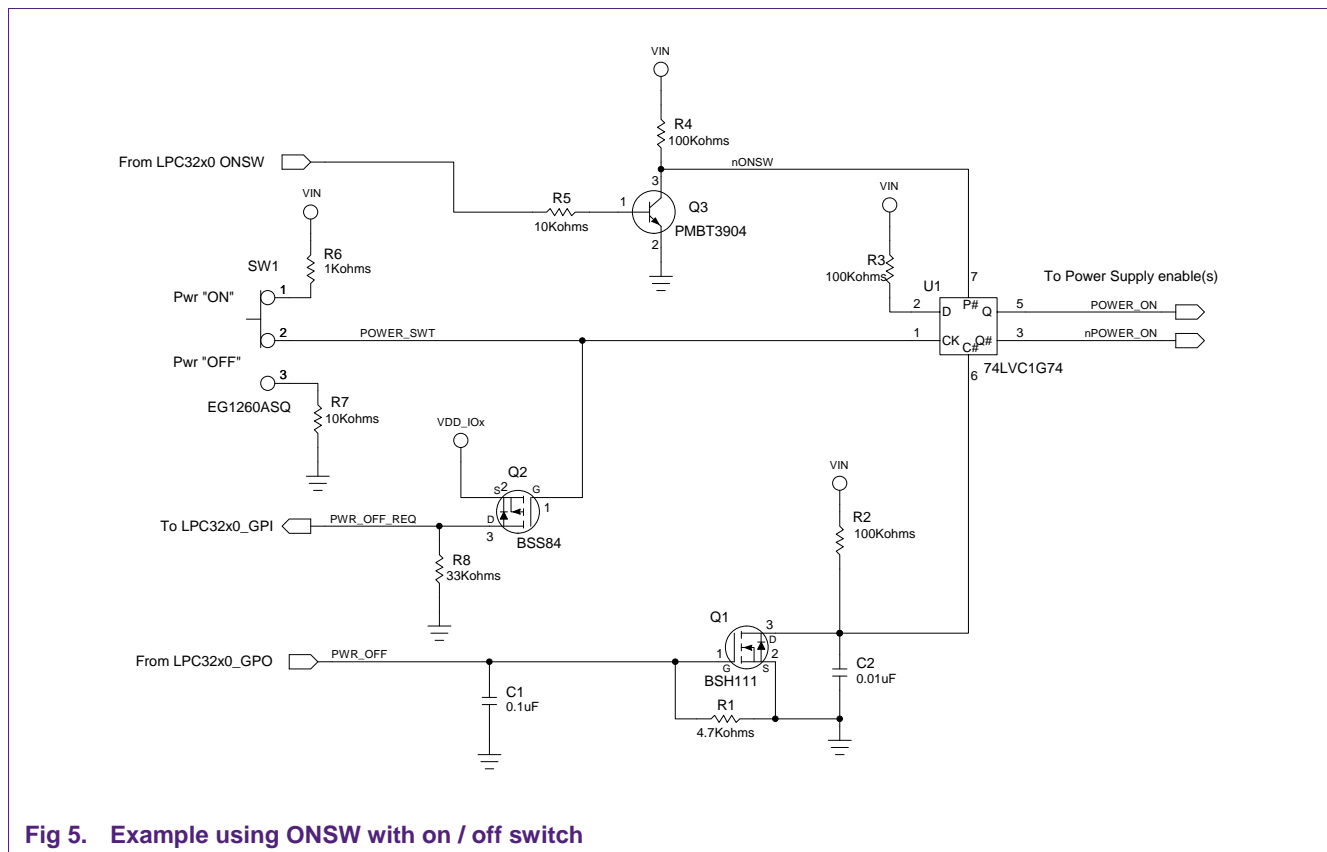


Fig 5. Example using ONSW with on / off switch

## 5. Notes on LPC32X0 Power supply design

### 5.1 LPC32X0 Power Supply Sequencing

There is no specific requirement for sequencing the LPC3230 power domains. The LPC32X0 core and IO voltages may come up together or either may come up first. However, the LPC32X0 RESET\_N pin must be held low for a minimum of 11mSec after all VDD power domains are at required minimum voltage levels to provide enough time for the main oscillator to start before the reset is released and code execution begins from the internal Boot ROM.

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## 7. Contents

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<b>1.</b>	<b>Introduction .....</b>	<b>3</b>
1.1	Purpose .....	3
1.2	LPC32X0 Microcontroller Description .....	3
1.3	LPC32X0 Power Domain Flexibility.....	3
<b>2.</b>	<b>LPC32X0 Power Domains .....</b>	<b>4</b>
2.1	CORE power domains .....	4
2.1.1	VDD_CORE .....	4
2.1.2	VDD_COREFXD .....	4
2.1.3	Other Core power domains .....	4
2.2	RTC power domain .....	4
2.3	Analog to Digital Converter power domain.....	4
2.4	External Memory Controller interface power domain .....	4
2.4.1	Supply voltage Impact on performance.....	5
2.5	Peripheral Interface power domains.....	5
2.5.1	Peripheral interface Power Domain limitation.....	5
<b>3.</b>	<b>LPC32X0 Minimal power supply design.....</b>	<b>7</b>
<b>4.</b>	<b>LPC32X0 power supply designs for power savings.....</b>	<b>7</b>
4.1	LPC32X0 Software Power Control Modes .....	8
4.2	Using the LPC32X0 Highcore pin to control VDD_CORE voltage.....	8
4.2.1	Example Power Supply using HIGHCORE pin...9	
4.3	I2C controlled variable VDD_CORE Power Supply .....	10
4.4	Save power using the ONSW pin.....	11
4.4.1	LPC32x0 RTC .....	11
4.4.2	Example hardware circuit using ONSW pin and on / off switch .....	11
<b>5.</b>	<b>Notes on LPC32X0 Power supply design.....</b>	<b>12</b>
5.1	LPC32X0 Power Supply Sequencing.....	12
<b>6.</b>	<b>Legal information .....</b>	<b>13</b>
6.1	Definitions .....	13
6.2	Disclaimers.....	13
6.3	Trademarks .....	13
<b>7.</b>	<b>Contents.....</b>	<b>14</b>

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