AN10833

MIFARE Type Identification Procedure

Rev. 3.6 — 11 July 2016
018436

Application note
COMPANY PUBLIC

Document information

Info	Content
Keywords	MIFARE, ISO/IEC 14443
Abstract	This document describes how to differentiate between the members of the MIFARE card IC family. ISO/IEC 14443-3 describes the initialization and anti-collision procedure, and ISO/IEC 14443-4 describes the protocol activation procedure. This document shows how to use these procedures to deliver the chip type information for all MIFARE ICs.

Revision history

Rev	Date	Description
3.6	20160711	Update for MIFARE Plus EV1
3.5	20140327	Update for multi-MIFARE implementation and implementation in UICC
3.4	20121029	Update for MIFARE Implementation in a device
3.3	20110928	Update for TNP3xxx
3.2	20110829	Update for the new MIFARE Classic with 7 byte UID option
3.1	20090707	Correction of Table 12
3	20090518	Third release (supersedes AN MIFARE Interface Platform, Type Identification Procedure, Rev. 1.3, Nov. 2004)

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

1.1 Terms and Abbreviations

Table 1 shows the terms and abbreviation used in this document. All the “Type A” related definitions are used and described in the ISO/IEC 14443 documents.

Table 1. Abbreviations

Abbreviation	
ATQA	Answer To Request acc. to ISO/IEC 14443-4
ATS	Answer To Select acc. to ISO/IEC 14443-4
DIF	Dual Interface (cards)
COS	Card Operating System
CL	Cascade Level acc. to ISO/IEC 14443-3
CT	Cascade Tag, Type A
n.a.	not applicable
NFC	Near Field Communication
PCD	Proximity Coupling Device (“Contactless Reader”)
PICC	Proximity Integrated Circuit (“Contactless Card”)
PKE	Public Key Encryption (like RSA or ECC)
REQA	Request Command, Type A
SAK	Select Acknowledge, Type A
Select	Select Command, Type A
RID	Random ID, typically dynamically generated at Power-on Reset (UID0 = “0x08”, Random number in UID1… UID3)
RFU	Reserved for future use
UID	Unique Identifier, Type A
NUID	Non-Unique Identifier

1.2 Scope

This document describes how to differentiate between the members of the MIFARE interface card IC family. The ISO/IEC 14443-3 describes the initialization and anti-collision procedure for type A, which delivers the card type information for all MIFARE cards.

The MIFARE cards are ISO/IEC 14443-3 compatible. Therefore already existing applications can easily be extended to operate with newer MIFARE chips respectively all other ISO/IEC 14443-3 compatible PICCs.

This document provides an easy guideline how the ISO/IEC 14443 compatible PCD should handle the MIFARE cards and how it can distinguish between the different available types of MIFARE cards.

1.3 MIFARE and ISO/IEC 14443

1.3.1 MIFARE

All MIFARE ICs are compliant to the ISO/IEC 14443 part 2 and part 3. The T=CL protocol as defined in the ISO/IEC 14443-4 is supported by MIFARE DESFire, the NXP Dual or Triple Interface Card ICs (like SmartMX), and the MIFARE Plus.

The MIFARE Classic 1K, the MIFARE Mini, the MIFARE Classic 4K, the MIFARE Ultralight, the MIFARE Ultralight C and the MIFARE Plus in the security level 1 and 2 use the MIFARE Protocol.

The MIFARE Classic 1K, the MIFARE Mini, and the MIFARE Classic 4K use the proprietary MIFARE Crypto 1.

1.3.2 ISO/IEC 14443

The ISO/IEC 14443 consists of 4 parts.

1.3.2.1 Part 1: Physical characteristics

The ISO/IEC 14443-1 defines the physical size of the ISO/IEC 14443 PICC and its antenna.

1.3.2.2 Part 2: RF signal & power interface

The ISO/IEC 14443-2 defines the carrier frequency of 13.56 MHz, the modulation and coding, and the minimum and maximum field-strength. It is split up into type A (= MIFARE) and type B.

1.3.2.3 Part 3: Initialization & anti-collision

The ISO/IEC 14443-3 defines the start of communication and how to select the PICC. Sometimes this is called “Card Activation Sequence”. It is split up into type A (= MIFARE) and type B.

1.3.2.4 Part 4: Transmission protocol

The ISO/IEC 14443-4 defines the protocol for a data exchange between PCD and PICC. This protocol often is called “T=CL” protocol.

Please refer to the ISO/IEC 14443 documents for details.

2. MIFARE IC types

The Table 2 shows the NXP MIFARE ICs and their features, Table 3 shows the supported ISO layers.

Table 2. NXP Contactless Card IC Feature Overview

	MIFARE Ultralight	MIFARE Ultralight C	MIFARE Classic	MIFARE Plus	MIFARE Plus EV1	MIFARE DESFire	DIF (like SmartMX)
HW Crypto	-	3DES	Crypto1	Crypto1, AES	Crypto1, AES	3DES, AES	3DES, AES, PKE
EEPROM	512 bit	1536 bit	320 Bytes, 1k Bytes, 4k Bytes	2k Bytes, 4k Bytes	2k Bytes, 4k Bytes	2k Bytes, 4k Bytes, 8k Bytes	4k Bytes – 144k Bytes
Special Features	-	-	-	MIFARE Classic compatible	MIFARE Classic compatible	-	MIFARE Classic compatible
Certification	-	-	-	CC EAL 4+	CC EAL 5+	CC EAL 4+	CC EAL 5+
Contactless interface	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A

Table 3. NXP Contactless Card IC compliance overview

ISO layer	MIFARE Ultralight	MIFARE Ultralight C	MIFARE Classic	MIFARE Plus	MIFARE Plus EV1	MIFARE DESFire	SmartMX platform
ISO/IEC 14443 -4				✓	✓	✓	✓
ISO/IEC 14443 -3	✓	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 -2	✓	✓	✓	✓	✓	✓	✓

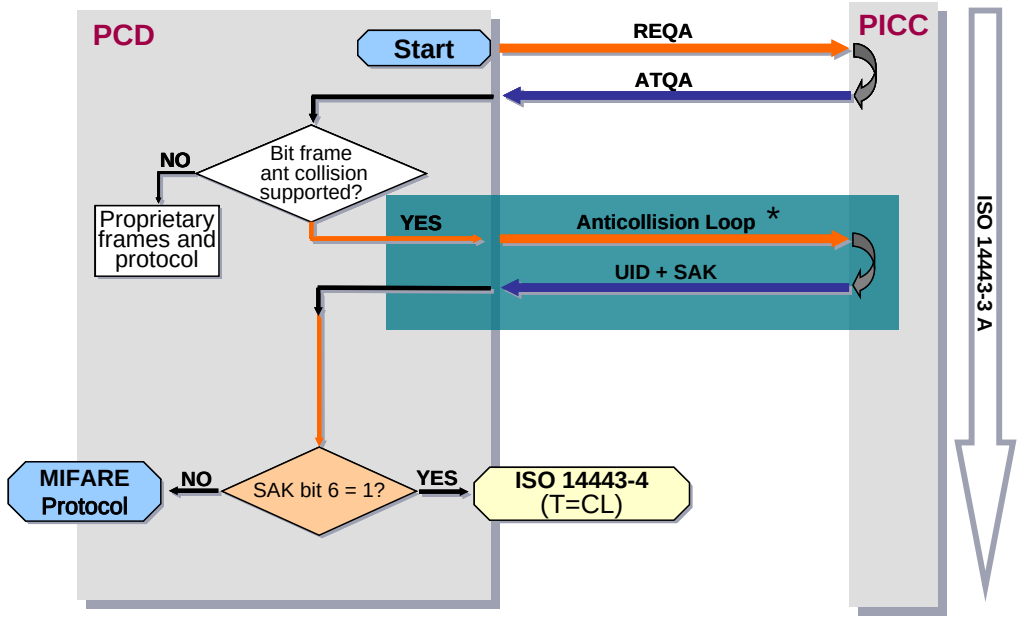
3. Chip Type Identification Procedure

The PCD typically polls for PICCs in the field. This is done with the REQA. When a PICC is within the operating range of the PCD and receives the REQA, any MIFARE PICC returns the ATQA.

The content of the ATQA should be ignored in a real application, even though according to the ISO/IEC 14443 it indicates that the PICC supports the anticollision scheme.

Note: In the case two or more MIFARE PICCs are in the operating field of the PCD at the same time, the received (combined) ATQA might contain “collisions”. That means there might be no unambiguous content anyway.

The complete card activation sequence is shown in the Fig 1 and Fig 2. The bit 6[1] in the SAK indicates, whether the PICC is compliant to the ISO/IEC14443-4 or not. However, it does not necessarily indicate, whether the PICC supports the MIFARE Protocol or not. For more details about selecting the different type of MIFARE cards refer to the AN “MIFARE ISO/IEC 14443 PICC Selection”.

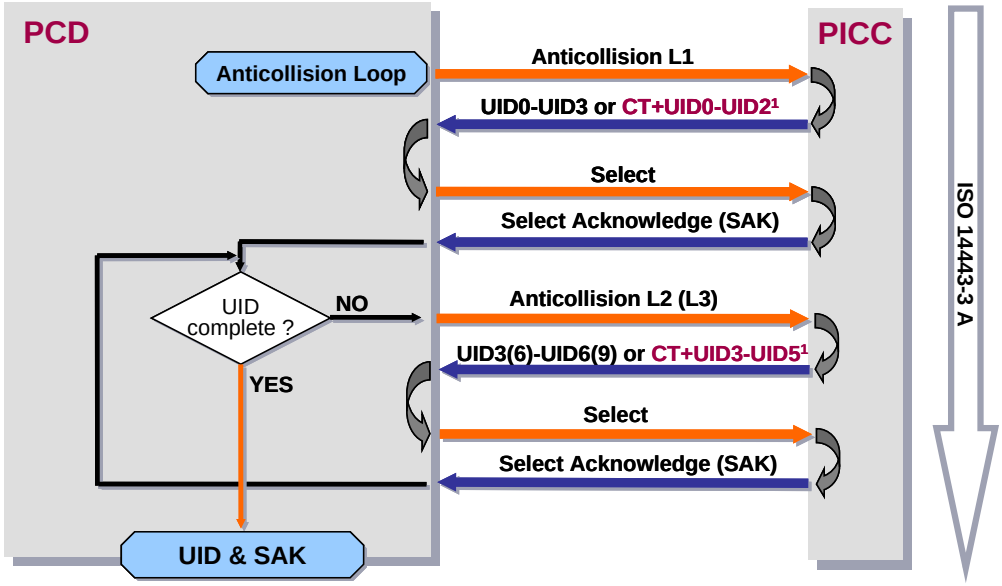


(1) Details of the Anticollision Loop see Fig 2.

Fig 1. Principle of the Card Activation Sequence

Note: For more details regarding the selection of one of the different types of MIFARE cards based on the SAK refer to AN 130830 “MIFARE ISO/IEC 14443 PICC Selection”.

1. Attention: The bit numbering in the ISO/IEC 14443 document starts with bit 1 … 8, but not bit 0…7.



(1) The CT (= Cascade Tag, Type A) byte indicates that the UID is not received completely yet. It indicates that another anticollision loop on the next higher cascade level is required to get the complete UID.

Fig 2. Anticollision Loop as part of the Card Activation Sequence

3.1 Coding of Answer to Request Type A (ATQA)

Table 4 shows the coding of the ATQA as described in the ISO/IEC 14443-3. The RFU marked bits must be set to “0”, the proprietary bits might be used for proprietary codings. In real application the content details of the ATQA are recommended to be ignored anyway.

Table 5 shows the ATQA coding of the NXP card ICs.

Note 1: The bit numbering in the ISO/IEC 14443 starts with LSBit = bit 1, but not LSBit = bit 0. So one byte counts bit 1…8 instead of bit 0…7.

Note 2: The ISO/IEC 14443 transfers LSByte first. So e.g. 0x 00 44 (ATQA of the MF UL) is often received as 0x 44 00.

Table 4. ATQA Coding according to the ISO/IEC 14443-3

Bit number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ISO/IEC 14443-3	RFU				Proprietary				UIDsize		RFU	Bit Frame Anticollision				
Proprietary	0	0	0	0				1			0					
	0	0	0	0			1				0					
	0	0	0	0		1					0					
Single Size UID	0	0	0	0					0	0	0					
Double Size UID	0	0	0	0					0	1	0					
Triple Size UID	0	0	0	0					1	0	0					
RFU	0	0	0	0					1	1	0					
Anticollision supported	0	0	0	0							0	1	0	0	0	0
	0	0	0	0							0	0	1	0	0	0
	0	0	0	0							0	0	0	1	0	0
	0	0	0	0							0	0	0	0	1	0
	0	0	0	0							0	0	0	0	0	1

Table 5. ATQA Coding of NXP Contactless Card ICs

X: depends on the COS

Bit number	Hex Value	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ISO/IEC 14443-3		RFU				Proprietary				UID size		RFU	Bit Frame Anti-collision				
MIFARE Ultralight	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Ultralight EV1	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Ultralight C	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Mini	00 x4	0	0	0	0	0	0	0	0	0	x[2]	0	0	0	1	0	0
MIFARE Classic 1K	00 x4	0	0	0	0	0	0	0	0	0	x[3]	0	0	0	1	0	0
MIFARE Classic 4K	00 x2	0	0	0	0	0	0	0	0	0	x[4]	0	0	0	0	1	0
MIFARE Plus 2K (4 Byte UID or 4 Byte RID)	00 04	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MIFARE Plus EV1 2K (4 Byte UID or 4 Byte RID)	00 04	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MIFARE Plus 4K (4 Byte UID or 4 Byte RID)	00 02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
MIFARE Plus EV1 4K (4 Byte UID or 4 Byte RID)	00 02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
MIFARE Plus 2K (7 Byte UID)	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Plus EV1 2K (7 Byte UID)	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Plus 4K (7 Byte UID)	00 42	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
MIFARE Plus EV1 4K (7 Byte UID)	00 42	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
MIFARE DESFire	03 44	0	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0
MIFARE DESFire EV1	03 44	0	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0
P3SR008	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

2. [2] The 7 byte UID MIFARE Mini has bit 7 = 1, even if the 4 byte NUID mapping is enabled.
3. [3] The 7 byte UID MIFARE Classic 1K has bit 7 = 1, even if the 4 byte NUID mapping is enabled.
4. [4] The 7 byte UID MIFARE Classic 4K has bit 7 = 1, even if the 4 byte NUID mapping is enabled.

Bit number	Hex Value	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
SmartMX with MIFARE 1K emulation	0X 04	0	0	0	0	x	x	x	x	0	0	0	0	0	1	0	0
SmartMX with MIFARE 4K emulation	0X 02	0	0	0	0	x	x	x	x	0	0	0	0	0	0	1	0
SmartMX with 7 Byte UID	0X 48	0	0	0	0	x	x	x	x	0	1	0	0	1	0	0	0
TNP3xxx	0F 01	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1

Never use ATQA to identify a chip or to extract UID size. Follow the ISO/IEC 14443-3 card activation sequence (fig 1 & 2 of this document) based on SAK. ATQA can be collided and misleading.

3.1.1 Coding of ATQA for MIFARE Implementation

In case of MIFARE Implementation, ATQA bits shall be set according to ISO14443-3, mentioning the UID size and if anti-collision is supported or not, all other RFU and propriety bits shall be set to 0.

Note: If the MIFARE implementation is going to be used in a running infrastructure where the existing infrastructure makes use of ATQA for PICC identification and or selection (although always recommended NOT to use), then there shall be an option in the implemented device for configuring the ATQA as required for this legacy application.

3.2 Coding of Select Acknowledge (SAK)

Table 6 shows the coding of the SAK of the NXP card ICs as described in the ISO/IEC 14443-3. It indicates the ISO/IEC 18092 protocol compliance, too. The RFU marked bits must be set to “0”, the proprietary bits might be used for proprietary coding.

In case of double size UIDs or triple size UIDs always **only** the last SAK shall be used to distinguish the chip type.

Note: RIDs always use the size of single size

Table 6. UIDs (4 Bytes) SAK coding of NXP Contactless Card ICs

Coding according to the ISO/IEC 14443-3 and ISO/IEC 18092, X = do not care

Bit number	UID size	Memory	Sec. Level	Hex Value	8	7	6	5	4	3	2	1
UID not complete				04	0	0	0	0	0	1	0	0
UID complete, PICC compliant with ISO/IEC 14443-4					X	X	1	X	X	0	X	X
UID complete, PICC not compliant with ISO/IEC 14443-4					X	X	0	X	X	0	X	X
UID complete, PICC compliant with ISO/IEC 18092 (NFC)					X	1	X	X	X	0	X	X

Bit number	UID size	Memory	Sec. Level	Hex Value	8	7	6	5	4	3	2	1
UID complete, PICC not compliant with ISO/IEC 18092					X	0	X	X	X	0	X	X
Any MIFARE CL1[5]	double			04	0	0	0	0	0	1	0	0
MIFARE DESFire CL1	double	-	-	24	0	0	1	0	0	1	0	0
MIFARE DESFire EV1 CL1	double	-	-	24	0	0	1	0	0	1	0	0
MIFARE Ultralight CL2	double			00	0	0	0	0	0	0	0	0
MIFARE Ultralight C CL2	double			00	0	0	0	0	0	0	0	0
MIFARE Mini	single	0.3K	-	09	0	0	0	0	1	0	0	1
MIFARE Classic 1K	single	1K	-	08	0	0	0	0	1	0	0	0
MIFARE Classic 4K	single	4K	-	18	0	0	0	1	1	0	0	0
MIFARE Mini CL2	double	0.3K	-	09	0	0	0	0	1	0	0	1
MIFARE Classic 1K CL2	double	1K	-	08	0	0	0	0	1	0	0	0
MIFARE Classic 4K CL2	double	4K	-	18	0	0	0	1	1	0	0	0
MIFARE Plus	single	2K	1	08	0	0	0	0	1	0	0	0
MIFARE Plus EV1	single	2K	1	08	0	0	0	0	1	0	0	0
MIFARE Plus	single	4K	1	18	0	0	0	1	1	0	0	0
MIFARE Plus EV1	single	4K	1	18	0	0	0	1	1	0	0	0
MIFARE Plus CL2	double	2K	1	08	0	0	0	0	1	0	0	0
MIFARE Plus EV1 CL2	double	2K	1	08	0	0	0	0	1	0	0	0
MIFARE Plus CL2	double	4K	1	18	0	0	0	1	1	0	0	0
MIFARE Plus EV1 CL2	double	4K	1	18	0	0	0	1	1	0	0	0
MIFARE Plus	single	2K	2	10	0	0	0	1	0	0	0	0
MIFARE Plus	single	4K	2	11	0	0	0	1	0	0	0	1
MIFARE Plus CL2	double	2K	2	10	0	0	0	1	0	0	0	0
MIFARE Plus CL2	double	4K	2	11	0	0	0	1	0	0	0	1
MIFARE Plus	single	2K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus EV1	single	2K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus	single	4K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus EV1	single	4K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus CL2	double	2K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus EV1 CL2	double	2K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus CL2	double	4K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus EV1 CL2	double	4K	3	20	0	0	1	0	0	0	0	0
MIFARE DESFire CL2	double	4K	-	20	0	0	1	0	0	0	0	0
MIFARE DESFire EV1 CL2	double	2K	-	20	0	0	1	0	0	0	0	0
MIFARE DESFire EV1 CL2	double	4K	-	20	0	0	1	0	0	0	0	0
MIFARE DESFire EV1 CL2	double	8K	-	20	0	0	1	0	0	0	0	0
Smart MX	single	-	-	xx[6]	x	x	x	x	x	x	x	x
Smart MX CL2	double	-	-	xx[7]	x	x	x	x	x	x	x	x
TNP3xxx	single	-	-	01	0	0	0	0	0	0	0	1

5. 5. Except the MIFARE DESFire and MIFARE DESFire EV1.
6. 6. Depends on the COS.
7. 7. Depends on the COS.

Note: The bit numbering in the ISO/IEC 14443 starts with LSBit = bit 1, but not LSBit = bit 0. So one byte counts bit 1…8 instead of bit 0…7.

Note: NXP MIFARE Plus ICs might use a **generic SAK** (in the near future), which does not (exclusively) indicate the chip type during the anti-collision procedure for privacy reasons. In such case the way to distinguish between different MIFARE Plus types is the read of Block 0, to use the ATS, if available, or the card capabilities of the Virtual Card Selection.

Note: The MIFARE Classic 1K, MIFARE Classic 4K and MIFARE Mini with 7 byte UID (Double Size UID) with NUID mapping enabled does not support Cascade Level 2, and therefore uses the indicated SAK in Cascade Level 1.

3.2.1 Coding of SAK for MIFARE Implementation

In case of MIFARE Implementation, final SAK shall be set according to ISO14443-3 and MIFARE SAKs. In case of multi-MIFARE implementation all supported SAKs can be ORed to generate a SAK to be presented. In case of UICC, sometimes the CLF itself can set some bits showing activated applications. Following table (table 7) shows some examples.

Table 7. SAK example for multiple MIFARE implementation

Example	Final SAK values					
	MIFARE Classic 1KB SAK = 0x08 (b4 is set)	MIFARE Classic 4KB SAK = 0x18 (b5,b4 are set)	MIFARE DESFire SAK = 0x20 (b6 is set)	P2P support from Android SAK = 0x40 (b7 is to be set)	Standard ISO1443-4 (b6 is set)	Resultant SAK
Example 1	X	-	X	-	-	0x28
Example 2	-	X	X	-	-	0x38
Example 3	-	X	-	-	X	0x38
Example 4	X	-	X	X	X	0x68
Example 5	-	-	-	X	X	0x60
Example 6	-	X	X	X	X	0x78
Example 7	X	-	-	-	X	0x28

Note: SAK is a bit mapping and is recommended to use the bit to check the MIFARE type, the full value of SAK shall not be used to detect a MIFARE type. For detail check in the application note AN10834 - MIFARE ISO/IEC 14443 PICC Selection.

In future, NXP recommends to use “Virtual Card Architecture (VCA)” for PICC selection and type identification. If installations do not depend on the actual content of ATQA, SAK and/or ATS for card selection and identification, this allows for more than one MIFARE product being enabled for activation in a single device at the same time. In this case, the VCA allows for efficient and privacy friendly selection of the targeted MIFARE product. This is described in a separate application note.

3.3 Coding of Answer To Select (ATS)

As the ATS of different MIFARE ICs can be customized, it is certainly not advisable to rely on the ATS to differentiate the IC type. NXP advises to keep the default value of the ATS to avoid any privacy attack based on the information in ATS.

3.4 Using GET_VERSION command to exactly identify the ICs

The MIFARE Ultralight EV1, MIFARE Plus EV1 and MIFARE DESFire EV2 support the command “GET_VERSION” to exactly identify the IC.

4. Legal information

4.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

4.3 Licenses

ICs with DPA Countermeasures functionality

NXP ICs containing functionality implementing countermeasures to Differential Power Analysis and Simple Power Analysis are produced and sold under applicable license from Cryptography Research, Inc.

4.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

MIFARE — is a trademark of NXP Semiconductors N.V.

MIFARE Plus — is a trademark of NXP Semiconductors N.V.

MIFARE Ultralight — is a trademark of NXP Semiconductors N.V.

MIFARE DESFire — is a trademark of NXP Semiconductors N.V.

5. Contents

For more information, visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 July 2016
018436
Document identifier: AN10833