### Document information

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<th>Info</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keywords</td>
<td>LPC1700, LPC1300, DSP library</td>
</tr>
<tr>
<td>Abstract</td>
<td>This application note describes how to use the DSP library with the LPC1700 and LPC1300 products</td>
</tr>
</tbody>
</table>
Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>3</td>
<td>20100611</td>
<td>Updated Section 3.</td>
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<tr>
<td>2</td>
<td>20100401</td>
<td>Added performance tables throughout.</td>
</tr>
<tr>
<td>1</td>
<td>20100210</td>
<td>Initial version.</td>
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</table>

Contact information

For additional information, please visit: [http://www.nxp.com](http://www.nxp.com)

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1. Introduction

The DSP library has been developed as a commonly used set of DSP functions optimized for the NXP Cortex-M3 LPC1700 and LPC1300 family products. Most functions have been implemented in Thumb-2 assembler unless there was little or no performance benefit in doing so.

The library is supplied as a static library project with source code in LPCXpresso (Code Red), Keil and IAR versions, and can also be linked into any ARM-EABI tool chain as a binary library.

1.1 DSP library functions

- Biquad filter
- Fast Fourier transform
- Dot product
- Vector manipulation
- FIR filter
- Resonator
- PID controller
- Random number generator

1.2 Convention used in function names and variable names

Each variable and function is prefixed with letters giving hints to the types. Some examples are shown below:

- vF: void Function
- iF: integer Function
- pi_x: a pointer to integer
- psi_x: a pointer to a signed integer
- si_x: a signed integer
- i_x: an integer
- pS_x: a pointer to a structure

1.3 Cortex-M3 for DSP

The Cortex-M3 has several attributes that make it deliver excellent DSP performance:

- 1-cycle 32x32 -> 32 signed multiplication
- 2-cycle (32x32)+32 -> 32 signed multiply accumulate
- Cortex-M3 is Harvard in having a separate data port to memory and instruction port to memory

Notes:

- Any load with base register update such as LDR <rt>,[<rn>],#<imm8> takes 2-cycles due to register bank write port conflict with the register write in the following instruction. The few exceptions are when it is followed by instructions that do not write results back to the register bank.
In the library there are 16- and 32-bit variants of many algorithms. Because the Cortex-M3 is fundamentally a 32-bit architecture, there is often little or no performance improvement in the 16-bit implementation. Some other ARM cores have the 'E' DSP extensions or the V6 SIMD extensions that effectively allow the 32-bit registers to be used as a pair of 16-bit registers.

One performance benefit from the 16-bit implementations could be the reduced data memory footprint of the coefficients and data for the algorithm and also the reduced memory system bandwidth which at the very least should save some power.

The algorithms are all implemented using the native C types of 'int' and 'short int'. A 32x32 multiply will overflow the 32-bit result if the inputs are not scaled appropriately by the user of the library.
2. Biquad filter

The biquad is a commonly used 2\textsuperscript{nd} order filter section that can be cascaded to build any order of filter.

Biquad discrete-time function:

\[ y(n) = b_0 \cdot x(n) + b_1 \cdot x(n-1) + b_2 \cdot x(n-2) + a_1 \cdot y(n-1) + a_2 \cdot y(n-2) \]

The Z-domain transfer function is:

\[ H(z) = \frac{(b_0 + b_1 \cdot Z^{-1} + b_2 \cdot Z^{-2})}{(1 - a_1 \cdot Z^{-1} - a_2 \cdot Z^{-2})} \]

The implementation is a Direct Form II (see Ref. [3]) which uses a shared 2-element state vector.

2.1 Function calling details

```c
void vF_dspl_biquad32(int *pi_Output, int *pi_Input, tS_biquad32_StateCoeff *pS_StateCoeff, int i_NSamples);
```

typedef struct
{
    short int psi_Coeff[5];
    short int psi_State[2];
}tS_biquad32_StateCoeff;

psi_Coeff are ‘2.14’ format fractional values.

psi_State are ‘2.14’ format fractional values that can be zero initialized for the first call but are updated by the routine to allow repeated calling of the filter with a stream of data.

pi_x and pi_y are ‘4.28’ format fractional values.

2.2 Biquad filter performance

<table>
<thead>
<tr>
<th>Biquad</th>
<th>Flash access (20 MHz max)</th>
<th>Flash access (40 MHz max)</th>
<th>Flash access (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time ((\mu)s)</td>
<td>Cycles</td>
</tr>
<tr>
<td>32 samples</td>
<td>626</td>
<td>31.300</td>
<td>631</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Biquad</th>
<th>Flash access (80 MHz max)</th>
<th>Flash access (100 MHz max)</th>
<th>Flash access (120 MHz max)[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time ((\mu)s)</td>
<td>Cycles</td>
</tr>
<tr>
<td>32 samples</td>
<td>641</td>
<td>8.013</td>
<td>648</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
3. Fast Fourier transform

The Discrete Time Fourier Transform (DFT) is a commonly used transform in communications, audio signal processing, speech signal processing, instrumentation signal processing and image processing.

There are many algorithms to implement the DFT efficiently, but often the reality is that certain algorithms suit certain machine architectures. The ARM architecture in general, due to the register bank of 16, delivers the best FFT performance by using a Radix-4 transform and this is what has been implemented in this library.

3.1 DFT formula

\[ X(k) = \sum_{n=0}^{N-1} x(n) \cdot W_N^{kn} \]

where:

\[ W_N = e^{-\frac{2\pi j}{N}} \]

3.2 DFT function prototype

```c
void vF_dspl_fftR4b16N64(short int *psi_Y, short int *psi_x);
void vF_dspl_fftR4b16N256(short int *psi_Y, short int *psi_x);
void vF_dspl_fftR4b16N1024(short int *psi_Y, short int *psi_x);
void vF_dspl_fftR4b16N4096(short int *psi_Y, short int *psi_x);
```

3.3 FFT performance

<table>
<thead>
<tr>
<th>FFT (coefficients in flash memory)</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 points</td>
<td>Cycles 3895 Time (ms) 0.195</td>
<td>Cycles 4035 Time (ms) 0.101</td>
<td>Cycles 4202 Time (ms) 0.070</td>
<td>Cycles 4384 Time (ms) 0.055</td>
<td>Cycles 4616 Time (ms) 0.046</td>
<td>Cycles 4616 Time (ms) 0.038</td>
</tr>
<tr>
<td>256 points</td>
<td>Cycles 21107 Time (ms) 1.055</td>
<td>Cycles 21719 Time (ms) 0.543</td>
<td>Cycles 22339 Time (ms) 0.372</td>
<td>Cycles 22961 Time (ms) 0.287</td>
<td>Cycles 23884 Time (ms) 0.239</td>
<td>Cycles 23884 Time (ms) 0.199</td>
</tr>
<tr>
<td>1024 points</td>
<td>Cycles 107007 Time (ms) 5.350</td>
<td>Cycles 110161 Time (ms) 2.754</td>
<td>Cycles 113326 Time (ms) 1.889</td>
<td>Cycles 116749 Time (ms) 1.459</td>
<td>Cycles 121657 Time (ms) 1.217</td>
<td>Cycles 121657 Time (ms) 1.014</td>
</tr>
<tr>
<td>4096 points</td>
<td>Cycles 518926 Time (ms) 25.946</td>
<td>Cycles 538209 Time (ms) 13.455</td>
<td>Cycles 557494 Time (ms) 9.292</td>
<td>Cycles 578059 Time (ms) 7.226</td>
<td>Cycles 600694 Time (ms) 6.007</td>
<td>Cycles 600694 Time (ms) 5.006</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
4. Dot product

This function implements a 32-bit dot-product (otherwise known as the scalar product) in assembler. The loop does one multiply per loop iteration for maximum vector length flexibility, but could be simply unrolled further for fixed lengths of vectors.

4.1 Dot product formula

\[ z = \sum_{i=0}^{N-1} x(i) \cdot y(i) \]

4.2 Dot product function prototype

```c
int iF_dspl_dotproduct32(int *pi_x, int *pi_y, int i_VectorLen);
```

4.3 Dot product performance

- N = Number of cycles
- \( N = (8 \times i_{\text{VectorLen}}) + 8 \)

Assumes all instruction fetches are single cycle.
5. Vector add

5.1 VectAdd16

```c
void vF_dspl_vectadd16(int *psi_z, int *psi_x, int *psi_y, int i_VectorLen);
```

5.2 VectAdd32

```c
void vF_dspl_vectadd32(int *pi_z, int *pi_x, int *pi_y, int i_VectorLen);
```

5.3 Vector add performance

<table>
<thead>
<tr>
<th>Vector addition</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit 32 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 bit</td>
<td>340</td>
<td>17.000</td>
<td>343</td>
</tr>
<tr>
<td>32 bit</td>
<td>341</td>
<td>17.050</td>
<td>346</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vector addition</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit 32 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 bit</td>
<td>349</td>
<td>4.363</td>
<td>352</td>
</tr>
<tr>
<td>32 bit</td>
<td>357</td>
<td>4.463</td>
<td>363</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
6. Vector subtract

6.1 VectSub16

```c
void vF_dspl_vectsub16(int *psi_z, int *psi_x, int *psi_y, int i_VectorLen);
```

6.2 VectSub32

```c
void vF_dspl_vectsub32(int *pi_z, int *pi_x, int *pi_y, int i_VectorLen);
```

6.3 Vector Sub Performance

### Table 4. Vector subtraction

<table>
<thead>
<tr>
<th>Vector subtraction</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>309</td>
<td>15.450</td>
<td></td>
<td>313</td>
</tr>
<tr>
<td>341</td>
<td>17.050</td>
<td></td>
<td>346</td>
</tr>
<tr>
<td>32 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>321</td>
<td>4.013</td>
<td></td>
<td>326</td>
</tr>
<tr>
<td>358</td>
<td>4.475</td>
<td></td>
<td>365</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
7. Vector add constant

7.1 VectAddConst16

void vF_dspl_vectaddconst16(int *psi_y, int *psi_x, int si_c, int i_VectorLen);

7.2 VectAddConst32

void vF_dspl_vectaddconst32(int *pi_y, int *pi_x, int i_c, int i_VectorLen);

7.3 Vector Add Constant Performance

<table>
<thead>
<tr>
<th>Vector add constant</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td>274</td>
<td>13.700</td>
<td>278</td>
</tr>
<tr>
<td>32 bit</td>
<td>274</td>
<td>13.700</td>
<td>280</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vector add constant</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td>287</td>
<td>3.588</td>
<td>292</td>
</tr>
<tr>
<td>32 bit</td>
<td>295</td>
<td>3.688</td>
<td>303</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
8. Vector element-by-element multiply

8.1 VectMulElement16

```c
void vF_dspl_vectmulelement16(int *psi_z, int *psi_x, int *psi_y, int i_VectorLen);
```

8.2 VectMulElement32

```c
void vF_dspl_vectmulelement32(int *pi_z, int *pi_x, int *pi_y, int i_VectorLen);
```

8.3 Vector Element-by-Element Multiply Performance

<table>
<thead>
<tr>
<th>Vector multiply</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 bit</td>
<td>277</td>
<td>13.850</td>
<td>280</td>
</tr>
<tr>
<td>32 bit</td>
<td>309</td>
<td>15.450</td>
<td>312</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vector multiply</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 bit</td>
<td>286</td>
<td>3.575</td>
<td>290</td>
</tr>
<tr>
<td>32 bit</td>
<td>320</td>
<td>4.000</td>
<td>325</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
9. Vector multiply by constant

Multiply each vector element by a constant.

9.1 Vector Multiply by Constant formula

\[ y = x \cdot c \]

9.2 VectMulConst16 function prototype

```c
void vF_dspl_vectmulconst16(short int *psi_y, short int *psi_x, short int si_c, int i_VectorLen);
```

9.3 VectMulConst32 function prototype

```c
void vF_dspl_vectmulconst32(int *pi_y, int *pi_x, int i_c, int i_VectorLen);
```

9.4 Vector Multiply by Constant Performance

<table>
<thead>
<tr>
<th>Vector multiply constant</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time ((\mu)s)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td>243</td>
<td>12.150</td>
<td>247</td>
</tr>
<tr>
<td>32 bit</td>
<td>274</td>
<td>13.700</td>
<td>277</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vector multiply constant</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time ((\mu)s)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td>257</td>
<td>3.213</td>
<td>264</td>
</tr>
<tr>
<td>32 bit</td>
<td>283</td>
<td>3.538</td>
<td>286</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
10. Vector sum of squares

10.1 Vector sum of squares formula
\[ y = \sum_{i=0}^{N-1} x_i^2 \]

10.2 VectSumSquares16 function prototype

```c
int iF_dspl_vectsumofsquares16(short int *psi_x, int i_VectorLen);
```

10.3 VectSumSquares32 function prototype

```c
int iF_dspl_vectsumofsquares32(int *pi_x, int i_VectorLen);
```

10.4 Vector Sum of Squares Performance

<table>
<thead>
<tr>
<th>Vector sum of squares</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td>242</td>
<td>12.100</td>
<td>244</td>
</tr>
<tr>
<td>32 bit</td>
<td>242</td>
<td>12.100</td>
<td>245</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vector sum of squares</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>16 bit</td>
<td>250</td>
<td>3.125</td>
<td>254</td>
</tr>
<tr>
<td>32 bit</td>
<td>254</td>
<td>3.175</td>
<td>259</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
11. FIR filter

Unlike DSP processors, the Cortex-M3 cannot perform load operations in parallel with ALU operations, so each data load cycle is a cycle that cannot be used for performing filter arithmetic. FIR filters are basically a long sequence of multiply-accumulate operations with the output sample being produced by the accumulation of many coefficient by input-sample multiplies.

To maximize FIR filter performance on the Cortex-M3, we utilize what is known as a ‘block-FIR’ algorithm. The algorithm reduces the number of memory accesses by computing several output samples in each loop iteration. In this way, the input data and the coefficients can be re-used multiple times before reading some more from memory.

11.1 FIR filter formula

\[ y(n) = \sum_{i=0}^{N-1} x(n-i) \cdot h(i) \]

11.2 FIR32 calling details

```c
typedef struct
{
    int *pi_Coeff;
    int NTaps;
}tS_blockfir32_Coeff;

void vF_dspl_blockfir32(int *pi_y, int *pi_x, tS_blockfir32_Coeff *pS_Coeff, int i_nsamples);
```

Note that the number of sample 'i_nsamples' must be a multiple of 4.

11.3 FIR filter performance

<table>
<thead>
<tr>
<th>Table 9. FIR filter</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>32 samples and taps</td>
<td>3433</td>
<td>171.650</td>
<td>3445</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th></th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
</tr>
<tr>
<td>32 samples and taps</td>
<td>3495</td>
<td>43.688</td>
<td>3520</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
12. Resonator (oscillator)

The resonator function is used to very efficiently generate sinusoidal signal—i.e., no look up table or use of trigonometric approximations. Note that this algorithm is just a special case of the biquad filter section but with the numerator coefficients equal to zero and the two poles on the unit-circle so that it oscillates.

12.1 Resonator formula

12.1.1 Discrete time representation

\[ y(n) = a_1 \cdot y(n-1) + a_2 \cdot y(n-2) \]

12.1.2 Z-domain representation

\[ H(z) = \frac{1}{(1-a_1 \cdot z^{-1} - a_2 \cdot z^{-2})} \]

12.2 Resonator calling details

typedef struct
{
    int i_Coeff_a1;
    int i_yn_1;
    int i_yn_2;
} tS_ResonatorStateCoeff;

void vF_dspl_resonator(int *psi_Output, void *pS_ResonatorStateCoeff, int i_NSamples);

Since the resonator is a recursive algorithm, care needs to be taken with the parameter scaling that is used. The coefficients and state of the resonator needs setting up as follows:

\[ i_{Coeff\_a1} = 2.0 \cdot \cos(Omega) \cdot \text{pow}(2.0,14) \]

To start the oscillation, the initial state should be set as follows:

\[ i_{yn\_1} = 0; \]
\[ i_{yn\_2} = -\text{Amplitude} \cdot \sin(Omega) \cdot \text{pow}(2.0,14) \]

where:

Omega = frequency as a fraction of the sample rate
Amplitude = required amplitude of the wave – must be <2.0 due to the ‘2.14’ arithmetic

A numerical format of ‘2.14’ has been used because the a1 coefficient is larger than 1 and the single cycle multiply of the CM3 can only be guaranteed not to overflow if the multiplier and multiplicand inputs to the multiplier are 16-bits.
### 12.3 Resonator performance

<table>
<thead>
<tr>
<th>Resonator</th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
<td>Time (μs)</td>
</tr>
<tr>
<td>512 samples</td>
<td>5153</td>
<td>257.650</td>
<td>5157</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Resonator</th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycles</td>
<td>Time (μs)</td>
<td>Cycles</td>
<td>Time (μs)</td>
</tr>
<tr>
<td>512 samples</td>
<td>5166</td>
<td>64.575</td>
<td>5172</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
13. PID controller

The ‘Proportional, Integral, Differential’ is a commonly used feedback control algorithm with very modest CPU usage.

13.1 PID controller discrete time formula

\[ u(n) = K_p \cdot e(n) + K_i \cdot \sum_{k=0}^{n} e(k) + K_d \cdot (e(n) - e(n-1)) \]

13.2 PID controller function calling details

```c
typedef struct {
    short int Kp;
    short int Ki;
    short int Kd;
    short int IntegratedError;
    short int LastError;
} tS_pid_Coeff;

short int vF_dspl_pid(short int si_Error, tS_pid_Coeff *pS_Coeff);
```

13.3 PID controller performance

Table 11. PID controller

<table>
<thead>
<tr>
<th></th>
<th>Flash access 1 CPU clocks (20 MHz max)</th>
<th>Flash access 2 CPU clocks (40 MHz max)</th>
<th>Flash access 3 CPU clocks (60 MHz max)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time ((\mu s))</td>
<td>Cycles</td>
</tr>
<tr>
<td>PID</td>
<td>47</td>
<td>2.350</td>
<td>49</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Flash access 4 CPU clocks (80 MHz max)</th>
<th>Flash access 5 CPU clocks (100 MHz max)</th>
<th>Flash access 5 CPU clocks (120 MHz max)[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cycles</td>
<td>Time ((\mu s))</td>
<td>Cycles</td>
</tr>
<tr>
<td>PID</td>
<td>56</td>
<td>0.700</td>
<td>60</td>
</tr>
</tbody>
</table>

[1] 120 MHz only available on LPC1759 and LPC1769.
14. Random number generator

The library implements an assembler version of a Linear Congruential random sequence generator best described in Ref. [1].

Note that if you only want less bits than the 32-bits returned by this function it is better to choose the upper bits of the word returned as these are 'more random' than the lower bits.

14.1 Random number formula

\[ Y_n = (a \cdot X_n + c) \mod m \]

Where:
- \( Y_n \) is the new number in the output sequence
- \( X_n \) is a seed value (or the previous value in a sequence)
- \( c \) is a well chosen constant – see Ref. [1]
- \( a \) is a well chosen multiplier constant – Ref. [1]
- \( m \) is a carefully chosen modulus for the arithmetic – Ref. [1]

In our implementation \( m=2^{32} \) so that we simply use the native arithmetic.

\[ c = 32767 \]
\[ a = 16644525 \]

14.2 Random number function prototype

\[ \text{int iF_RandomNumber(int i_Seed);} \]

Note: To produce a sequence of random numbers, use the previous result as the seed for the next call.

14.3 Random number performance

<table>
<thead>
<tr>
<th>Table 12. Random number generator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash access 1 CPU clocks (20 MHz max)</td>
</tr>
<tr>
<td>Cycles</td>
</tr>
<tr>
<td>Random number</td>
</tr>
</tbody>
</table>

| Flash access 4 CPU clocks (80 MHz max) | Flash access 5 CPU clocks (100 MHz max) | Flash access 5 CPU clocks (120 MHz max) |
| Cycles | Time (\( \mu \)s) | Cycles | Time (\( \mu \)s) | Cycles | Time (\( \mu \)s) |
| Random number | 34 | 0.425 | 38 | 0.380 | 38 | 0.317 |

[1] 120 MHz only available on LPC1759 and LPC1769.
15. References


16. Legal information

16.1 Definitions

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