AN10928

Enhanced BOD function of LPC98x/97x

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Document information

Info	Content
Keywords	LPC98x, LPC97x, enhanced BOD, brownout detect
Abstract	This application note describes how to use enhanced BOD function in LPC98x/97x. Demo code is also provided.

Revision history

Rev	Date	Description
01	20100409	Initial version.

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1. Introduction

The brownout detect function determines if the power supply voltage drops below a certain level. The Enhanced BOD feature of the P89LPC98x/97x has three independent functions: BOD reset, BOD interrupt and BOD flash.

2. BOD flash

BOD flash is used for flash program/erase protection. BOD flash is always on, except in power-down or total power-down mode (PCON.1 = 1). It can not be disabled in software. BOD flash has only one trip voltage level at 2.4 V.

For the 2K/4K/8K bytes of on-chip flash, the BOD flash is tripped and flash erase/program is blocked when V_{DD} is lower than 2.4 V. The HVA bit in the FMCON register indicates the BOD flash occurred.

3. BOD reset and BOD interrupt

A BOD reset will cause a processor reset and it is always enabled, except in power-down or total power-down mode. It can not be disabled in software. The BOD interrupt will generate an interrupt and can be enabled or disabled in software.

The BOD reset and BOD interrupt each has six trip voltage levels. BOE0 to BOE2 (UCFG1[3:5]) are used as the trip point configuration bits of BOD reset. BOICFG0 to BOICFG2 in the BODCFG register are used as trip point configuration bits for the BOD interrupt. The BOD reset voltage should be lower than the BOD interrupt trip point. Table 1 and Table 2 give BOD trip point configuration.

Table 1. BOD reset trip points configuration

BOE2 (UCFG1.5)	BOE1 (UCFG1.4)	BOE0 (UCFG1.3)	BOD reset	
			Fall	Rise
0	0	0	Reserved	Reserved
0	0	1	Reserved	Reserved
0	1	0	2.25 V	2.4 V
0	1	1	2.55 V	2.7 V
1	0	0	2.85 V	3.0 V
1	0	1	3.15 V	3.3 V
1	1	0	3.85 V	4 V
1	1	1	4.05 V	4.2 V

Table 2. BOD interrupt trip points configuration

BOICFG2 (BODCFG.2)	BOICFG1 (BODCFG.1)	BOICFG0 (BODCFG.0)	BOD interrupt	
			Fall	Rise
0	0	0	Reserved	Reserved
0	0	1	Reserved	Reserved
0	1	0	2.55 V	2.7 V
0	1	1	2.85 V	3.0 V
1	0	0	3.0 V	3.15 V
1	0	1	3.45 V	3.6 V
1	1	0	4.15 V	4.3 V
1	1	1	4.35 V	4.5 V

After power-on reset, the value of BOICFG 2 to BOICFG 0 bits will be copied from UCFG1.5 to UCFG1.3. The factory preprogrammed value of the UCFG1 register is 0x53 as shown in Table 3. In this case, the trip voltage level is 2.25 V (fall) and 2.4 V (rise) for the BOD reset and 2.55 V (fall) and 2.7 V (rise) for the BOD interrupt. Of course, it is possible to change the trip point of the BOD interrupt in software. When configuring the trip voltage of the BOD reset, make sure the operational supply voltage is high enough. Otherwise it will cause the processor to be reset continuously.

In power-down mode (PMOD1/PMOD0 = ‘10’) or total power-down mode (PMOD1/PMOD0 = '11'), the circuitry for the Brownout Detection is disabled for lowest power consumption. When the PMOD1/PMOD0 bits are not equal to ‘10’ or '11', BOD reset is always enabled and the BOD interrupt is enabled by setting BOI (PCON.4) bit. Please refer to Table 4 for BOD reset and BOD interrupt configuration. For the BOF bit (RSTSRC.5), the BOD reset flag has a default value of '0' and is set when a BOD reset is tripped. For the BOIF bit (RSTSRC.6), the BOD interrupt flag default state is '0'; this bit is set when the BOD interrupt is tripped.

Table 3. Flash user configuration byte 1 (UCFG1) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CLKDBL	RPE	BOE2	BOE1	BOE0	FOSC2	FOSC1	FOSC0
Unprogrammed value	0	1	0	1	0	0	1	1

Table 4. BOD reset and BOD interrupt configuration

PMOD1/PMOD0 (PCON[1:0])	BOI (PCON.4)	EBO (IEN0.5)	EA (IEN0.7)	BOD reset	BOD interrupt
'10' (power-down) or '11' (total power-down)	X	X	X	N	N
'00' or '01' (normal or idle mode)	0	X	X	Y	N
	1	0	X	Y	N
		1	0	Y	N
		1	1	Y	Y

4. BOD demo

4.1 Demo introduction

This demo gives an example on how to use the enhanced BOD feature. The Keil MCB900 board with a LPC982 is used for this application note.

In the demo, the trip voltage is set to 2.25 V (fall) and 2.4 V (rise) for BOD reset and 2.55 V (fall) and 2.7 V (rise) for a BOD interrupt. While the LPC982 is running, the power supply is adjusted to lower than 2.55 V to trigger BOD interrupt. The ISR of the BOD interrupt will set the BOD_flag and blink the LEDs. In the main function, BOD_flag is polled. When it is set, the information of "BOD interrupt" will be output through UART0. The UART interface is configured as 9600 Hz baud rate, 8 bit data, no parity, and 1 stop bit.

The BOE2 to BOE0 bits (UCFG1.5 to1.3) are set to '010'. The subroutine BOD_Int_Config() implements BOD interrupt initialization.

```
1          BODCFG = 0x02;    // set BODCFG = 0000 0010 bin: the BOD int voltage is
     2.55V fall and 2.7V rise
2          EA = 1;           // set Enable all interrupts
3          EBO = 1;          // set BOD enable
4          PCON |=0x10;      // set BOD interrupt enable
```

The BOD interrupt ISR is implemented as below. BOD_flag is used to indicate the BOD interrupt occurs.

```
5     void BOD_ISR(void) interrupt 5
6     {
7          RSTSRC &= ~0x40; // clr BOIF at RSTSRC.6
8
9          BOD_flag = 1;         // make flag active
10
11         P2^=0xff;         // Blinky LEDs
12    }
13
```

4.2 Demo setup

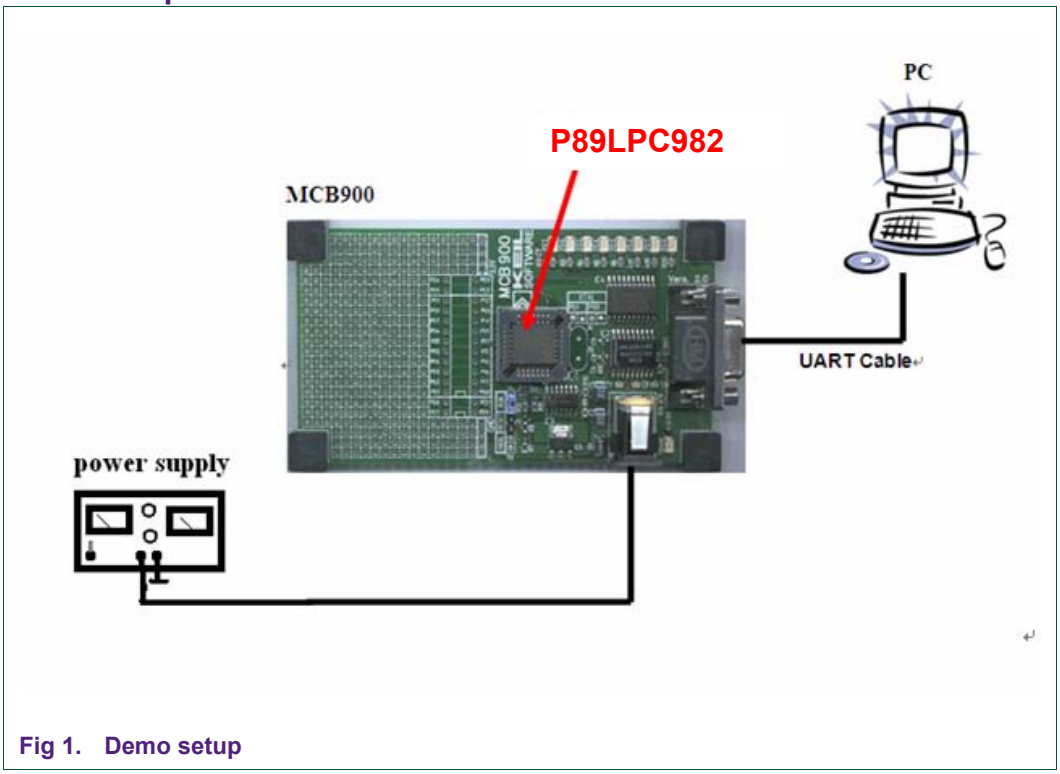

Fig 1. Demo setup

4.3 Output information

When the power supply falls to lower than about 2.55 V, the BOD interrupt is triggered and debug information “BOD interrupt” will be sent to UART0. If the power supply is raised higher than 2.7 V, there will be no serial debug information.

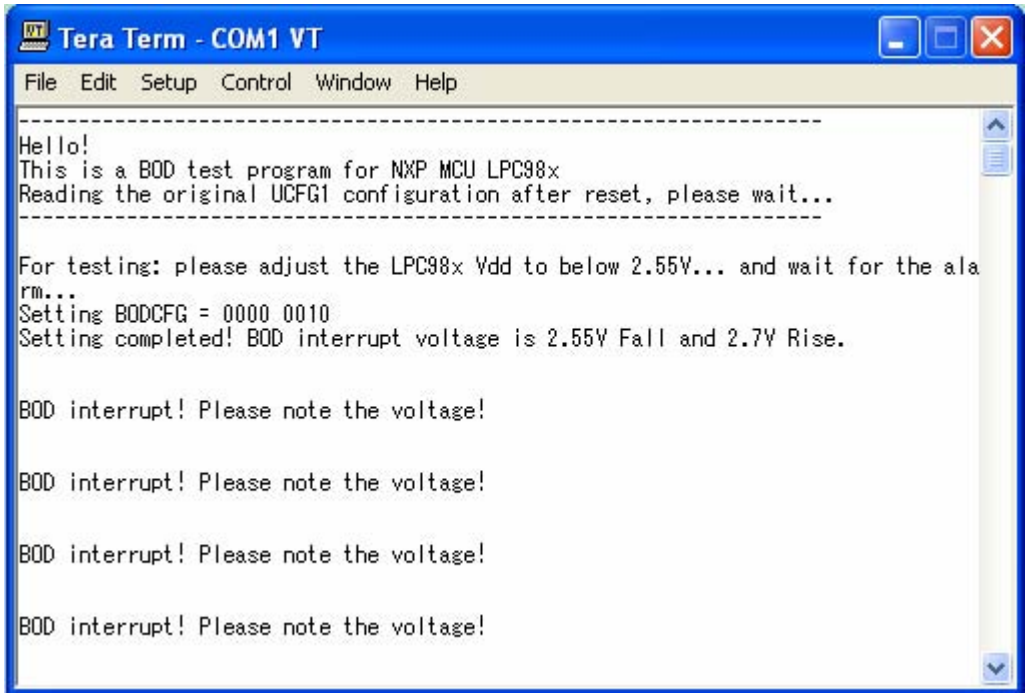

Fig 2. Output information

5. Reference

[1] LPC98x User Manual（UM10346）– Rev. 02

[2] LPC98x Data Sheet – Rev. 01

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