AN11013

GreenChip III TEA1753 integrated PFC and flyback controller

Rev. 1 — 21 March 2011 Application note

Document information

Info	Content
Keywords	GreenChip III, TEA1753, PFC, flyback, high efficiency, adaptor, notebook, PC power
Abstract	The TEA1753 is a member of the new generation of PFC and flyback combination controller ICs, used for efficient switched mode power supplies. Using the TEA1753 and TEA1703 provides a solution for applications needing an extremely low Standby power mode. It has a high level of integration which allows the design of a cost-effective power supply using the minimum number of external components. The TEA1753 is fabricated in a Silicon On Insulator (SOI) process, enabling it to operate at a wide voltage range.

Revision history

Rev	Date	Description
v.1	20110321	first issue

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1. Introduction

The TEA1753 is a combination controller with a PFC and flyback controller integrated into an SO16 package. Both controllers operate in Quasi-Resonance (QR) mode and in Discontinuous Conduction Mode (DCM) with valley detection. Both controllers are switched independently.

The PFC output power is on-time controlled for simplicity. It is not necessary to sense the phase of the mains voltage. The flyback output power is current mode controlled for good suppression of the input voltage ripple.

The communication circuitry between the controllers is integrated and no adjustment is needed.

The voltage and current levels mentioned in this application note are typical values. A detailed description of the pin level spreading can be found in the *TEA1753T and TEA1753LT data sheets*.

1.1 Scope

This application note describes the functionality of the TEA1753 and the adjustments needed within the power converter application.

The large signal parts of the PFC and the flyback power stages, the design and the data for the coil and the transformer are dealt with in a separate application note.

1.2 The TEA1753 GreenChip III controller

The features of the GreenChip III allow a power supply engineer to design a reliable, cost-effective and efficient switched mode power supply using the minimum number of external components.

1.2.1 Key features

- PFC and flyback controller integrated in one SO16 package
- Switching frequencies of PFC and flyback are independent of each other
- No external hardware required for the communication between both controllers
- High level of integration, resulting in minimal external component count
- Integrated mains voltage enable and brownout protection
- Fast latch reset function implemented
- Power-down functionality for very low Standby mode power requirements

1.2.2 System features

- Safe restart mode for system fault conditions
- High voltage start-up current source (5.4 mA)
- Reduction of HV current source (1 mA) in Safe restart mode
- Wide V_{CC} range (38 V)
- MOSFET driver voltage limited
- Easy control of start-up behavior and V_{CC} circuit

- General purpose input for latched protection
- Internal IC overtemperature protection
- One high-voltage spacer between the HV pin and the next active pin
- Open pin protection on the VINSENSE, VOSENSE, PFCAUX, FBCTRL and FBAUX pins

1.2.3 PFC features

- Dual output voltage boost converter
- QR/DCM operation with valley switching
- Frequency limitation (250 kHz) to reduce switching losses and ElectroMagnetic Interference (EMI)
- t_{on} controlled
- Mains input voltage compensation for control loop for good transient response
- OverCurrent Protection (OCP)
- Soft-start and soft-stop
- Open/short detection for PFC feedback loop: no external Overvoltage Protection (OVP) circuit necessary
- Adjustable delay for turning off the PFC

1.2.4 Flyback features

- QR/DCM operation with valley switching
- Frequency Reduction (FR) with fixed minimum peak current and valley switching to maintain high efficiency at low output power levels without audible noise
- Frequency limitation (125 kHz) to reduce switching losses and EMI
- Current mode controlled
- Overcurrent protection
- Soft-start
- Accurate OVP through auxiliary winding
- Time-out protection for output overloads and open flyback feedback loop, available as safe restart (TEA1753T) or latched (TEA1753LT) protection

1.3 Application schematic

Refer to Figure 1 for an overview of a typical application.

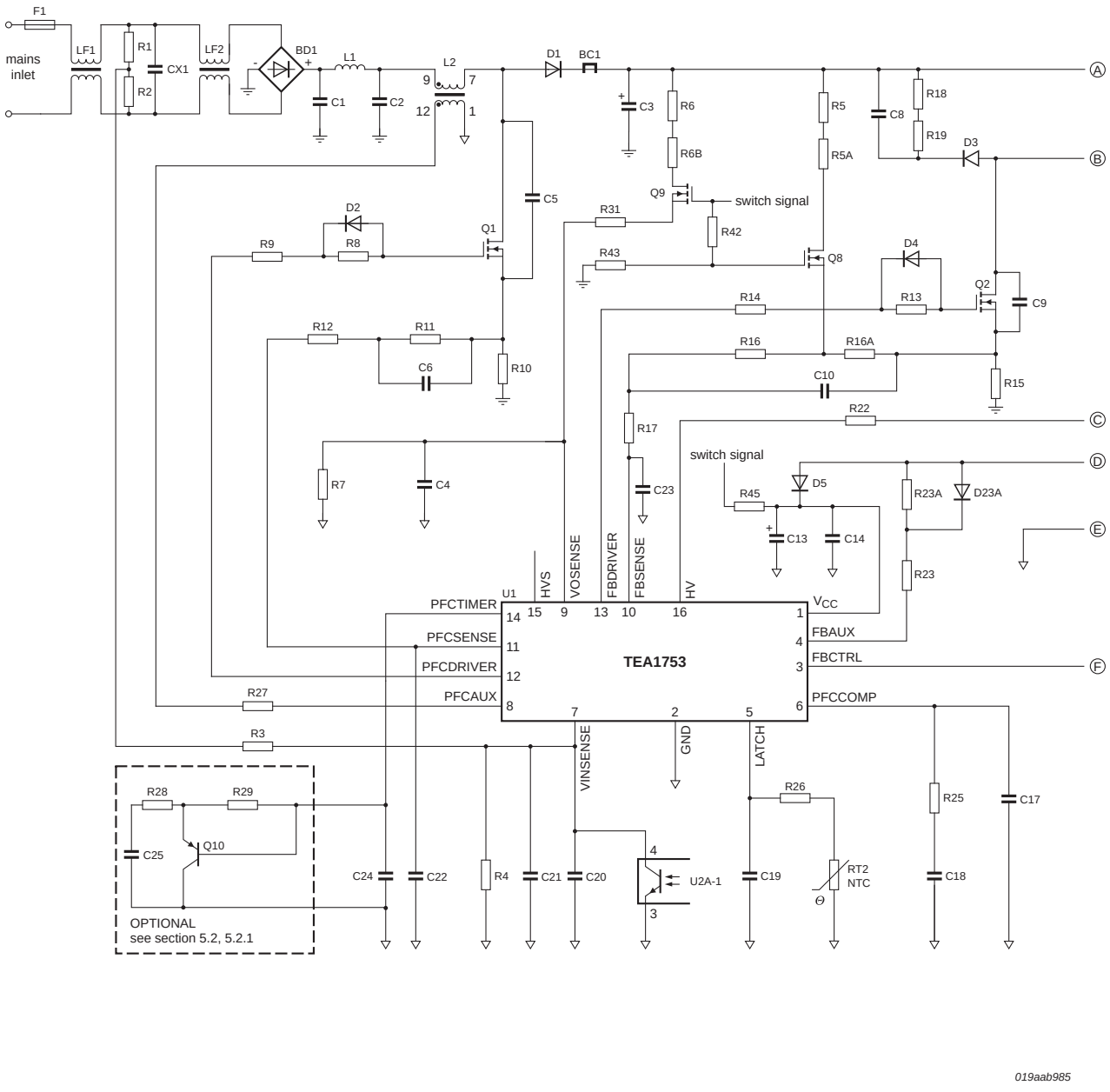


Fig 1. Application schematic (part1)

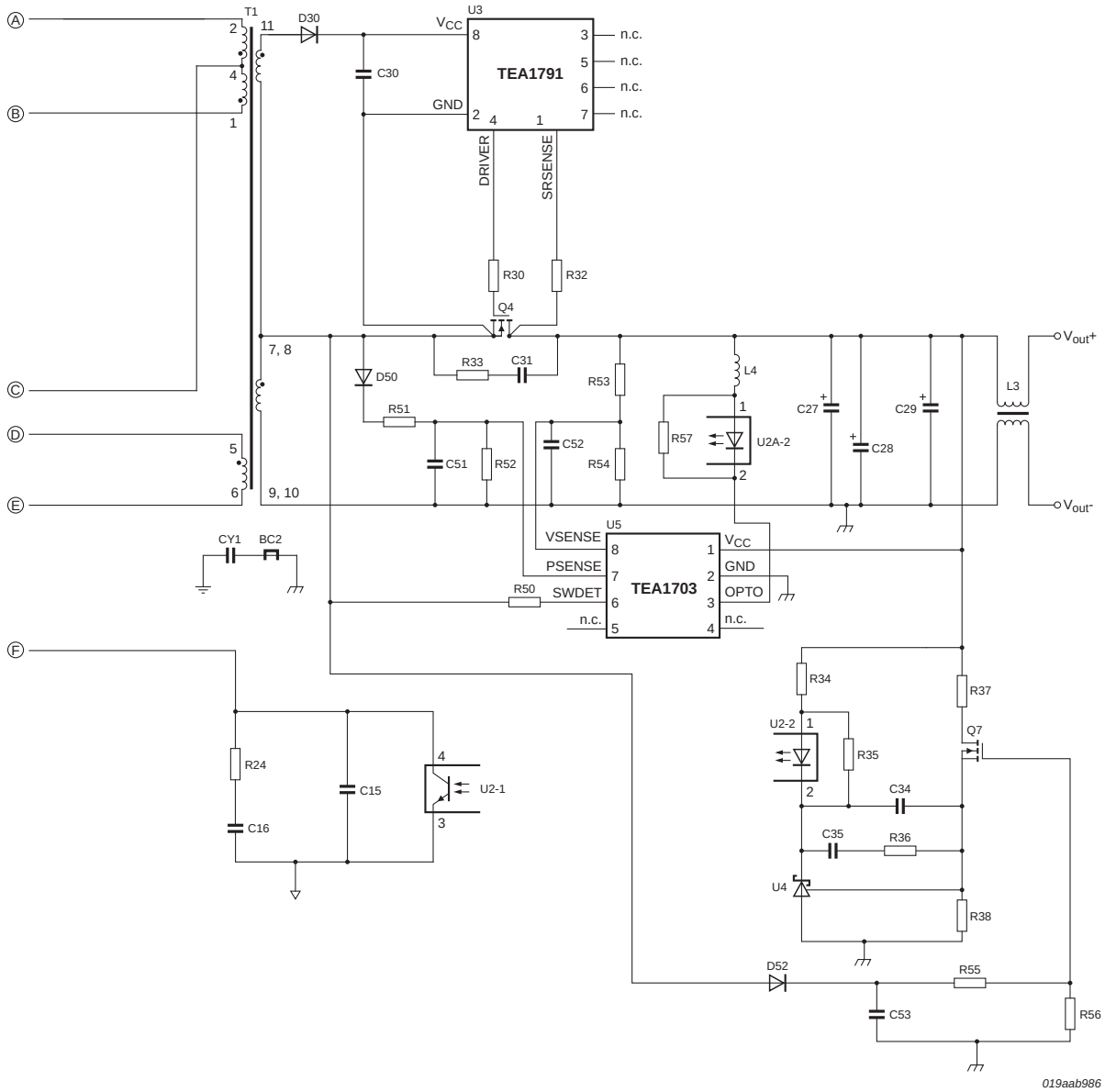


Fig 2. Application schematic (part2)

2. Pin description

Table 1. Pin description

Pin	Name	Functional description
1	V_{CC}	Supply voltage: $V_{startup}$ = 22 V, $V_{th(UVLO)}$ = 15 V. At mains switch-on, the capacitor connected to this pin is charged to $V_{startup}$ by the internal HV current source. When the pin voltage is lower than 0.65 V, the charge current is limited to 1 mA to prevent overheating of the IC if the V_{CC} pin is short-circuited. When the pin voltage is between 0.65 V and $V_{th(UVLO)}$, the charge current is 5.4 mA to enable a fast start-up. When it is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current is limited to 1 mA again to reduce the safe restart duty cycle. This results in a reduction of the input power during fault conditions. When $V_{startup}$ is reached, the HV current source is pinched off and V_{CC} is regulated to $V_{startup}$ until the flyback starts. See Section 3.2 for a complete description of the start-up sequence.
2	GND	Ground connection.
3	FBCTRL	Control input for flyback for direct connection of the optocoupler. At a control voltage of 2 V the flyback delivers maximum power. At a control voltage of 1.5 V the flyback enters the Frequency reduction mode. At 1.3 V the flyback stops switching. There is an internal 30 μA current source connected to the pin, which is controlled by the internal logic. This current source can be used to implement a time-out function to detect an open control loop or a short circuit of the output voltage. The time-out function is disabled by connecting a resistor of 100 kΩ between this pin and ground.
4	FBAUX	Input from auxiliary winding for transformer demagnetization detection, mains dependent OverPower Protection (OPP) and OverVoltage Protection (OVP) of the flyback. The combination of the demagnetization detection and the valley detection at pin HV determines the switch-on moment of the flyback in the valley. A flyback OVP is detected at a current higher than 300 μA to the FBAUX pin. Internal filtering prevents false detection of an OVP. The flyback OPP starts at a current lower than −100 μA from the FBAUX pin.
5	LATCH	General purpose latched protection input. When $V_{startup}$ (on pin 1) is reached, this pin is charged to 1.35 V before the PFC and the flyback can be enabled. The latched protection is triggered when the pin is pulled below 1.25 V and the PFC and the flyback are disabled. An internal 80 μA current source is connected to the pin, which is controlled by the internal logic. Using this current source, an optional Negative Temperature Coefficient (NTC) resistor can be directly connected to this pin for temperature protection.
6	PFCCOMP	Frequency compensation pin for the PFC control loop.

Table 1. Pin description *...continued*

Pin	Name	Functional description
7	VINSENSE	Sense input for mains voltage. This pin has six functions: • mains enable level: $V_{start(VINSENSE)}$ = 1.15 V; • mains stop level (brownout): $V_{stop(VINSENSE)}$ = 0.89 V; • mains voltage compensation for the PFC control loop gain bandwidth; • fast latch reset: V_{flr} = 0.75 V; • dual boost switchover point: $V_{bst(dual)}$ = 2.2 V. • Standby mode: $V_{th(pd)}$ = 350 mV The voltage on pin VINSENSE must be an averaged DC value, representing the AC line voltage. The pin is not used for sensing the phase of the mains voltage.
8	PFCAUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control PFC switching. The auxiliary winding needs to be connected via a 5 kΩ series resistor to prevent damage to the input because of lightning surges.
9	VOSENSE	Sense input for the output voltage of the PFC. VOSENSE pin, open-loop and short circuit detection: $V_{th(ol)(VOSENSE)}$ = 1.15 V; Regulation of the PFC output voltage: $V_{reg(VOSENSE)}$ = 2.5 V; PFC soft OVP (cycle-by-cycle): $V_{ovp(VOSENSE)}$ = 2.63 V; Control output for the output voltage of the PFC: - dual boost current: $I_{bst(dual)}$ = −8 μA.
10	FBSENSE	Current sense input for flyback. At this pin the sum of three voltages across three resistors is measured. Selecting the proper resistor values: • Prevents or minimizes the risk of saturation of the flyback transformer; • Allows some adjustment for enabling or disabling the PFC; • Allows a system that operates line voltage independently. The maximum setting level for $V_{sense(fb)max}$ is 0.63 V at dV/dt = 0 mV/μs. The level of $V_{sense(fb)min}$ is 0.30 V at dv/dt = 0 mV/μs and is related to the fixed peak current through the flyback transformer when the flyback is running in Frequency reduction mode. There are two internal current sources connected to this pin, $I_{start(soft)fb}$ and $I_{adj(FBSENSE)}$. $I_{start(soft)fb}$ is an internal current source of 60 μA, which is controlled by the internal logic. The current source is used to implement a soft-start function for the flyback. The flyback only starts when the internal current source can charge the soft-start capacitor to a voltage of more than 0.63 V. Therefore a minimum soft-start resistor of 16 kΩ is required to guarantee the enabling of the flyback. The current source $I_{adj(FBSENSE)}$ is 3 μA. It is intended to support the adjustment for enabling and disabling the PFC.
11	PFCSENSE	Overcurrent protection input for PFC. This input is used to limit the maximum peak current in the PFC core. The PFCSENSE is a switching-cycle-by-switching-cycle protection. When it reaches 0.52 V at dV/dt = 50 mV/μs the PFC MOSFET is switched off. An internal 60 μA current source is connected to this pin, which is controlled by the internal logic. This current source is used to implement a soft-start and soft-stop function for the PFC to prevent audible noise. The PFC only starts when the internal current source can charge the soft-start capacitor to a voltage of more than 0.5 V. A soft-start resistor of at least 12 kΩ is required to guarantee the enabling of the PFC.

Table 1. Pin description *...continued*

Pin	Name	Functional description
12	PFCDRIVER	Gate driver output for PFC MOSFET.
13	FBDRIVER	Gate driver output for flyback MOSFET.
14	PFCTIMER	Timer pin to delay the turning off of the PFC when the load of the flyback is removed or minimized. The PFC is enabled when the voltage across this pin is low (≤ 1.27 V). It is disabled when the voltage is high (≥ 3.6 V).
15	HVS	High-voltage safety spacer, not connected.
16	HV	High-voltage input for the internal start-up current source (output at pin 1) and valley sensing of the flyback. The combination of the demagnetization detection at the FBAUX pin and the valley detection at the HV pin determine the switch-on moment of the flyback in the valley.

3. System description and calculation

3.1 PFC and flyback start conditions

Figure 3 and Figure 4 show the conditions for enabling the PFC and the flyback. If start-up problems occur these conditions can be checked to find the cause of the problem. Some of the conditions are dynamic signals (see Figure 5) and should be checked using an oscilloscope.

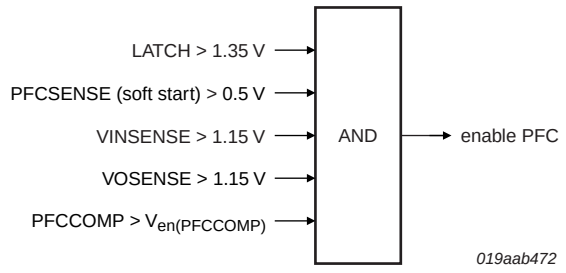


Fig 3. Enabling the PFC

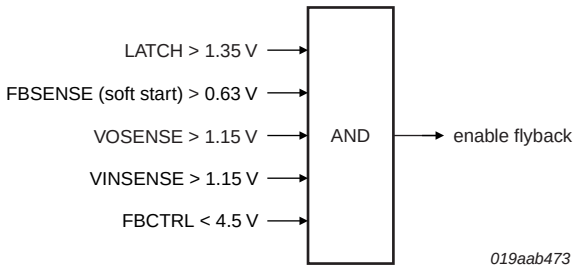


Fig 4. Enabling the Flyback

3.2 Start-up sequence

At switch-on with a low mains voltage the TEA1753 power supply has the following start-up sequence (see Figure 5):

1. The HV current source is set to 1.0 mA and the V_{CC} elcap is charged to 0.65 V to detect a possible short circuit on pin V_{CC}.
2. At V_{CC} = 0.65 V, the HV current source is set to 5.4 mA and the V_{CC} elcap is quickly charged to $V_{th(UVLO)}$.
3. At $V_{CC} = V_{th(UVLO)}$, the HV current source is set to 1.0 mA again and the V_{CC} elcap is charged to $V_{startup}$.
4. At $V_{startup}$, the HV current source is switched off and the 80 μA LATCH pin current source is switched on to charge the LATCH pin capacitor. At the same time the PFCSENSE and FBSENSE soft-start current sources are switched on.
5. When the LATCH pin is charged to 1.35 V, the PFC starts switching, but only when the VOSENSE and VINSENSE pins has reached 1.15 V.
6. Two extra conditions have to be met for enabling the PFC: The soft-start capacitor on pin PFCSENSE must be charged to 0.5 V, and the capacitors connected to the PFCCOMP pin are charged to either 2.5 V or 3.5 V depending on the required conditions needed for the $V_{en(PFCCOMP)}$ level.
7. Three conditions have to be met in order to enable the flyback: The PFC must be enabled, the soft-start capacitor on pin FBSENSE must be charged to 0.63 V and the voltage on pin FBCTRL must be lower than 4.5 V. Normally, the voltage on pin FBCTRL is lower than 4.5 V at the first flyback switching cycle, unless the FBCTRL pin is open. When the flyback starts, the FBCTRL time-out current source is switched on.

8. When the flyback has reached its nominal output voltage, the V_{CC} supply of the IC is taken over by the auxiliary winding. If the flyback feedback loop signal is missing, the time-out protection at the FBCTRL pin is triggered, both converters are switched off, V_{CC} drops to $V_{th(UVLO)}$ and the IC restarts at step 3 of the start-up cycle. This is the safe restart cycle.

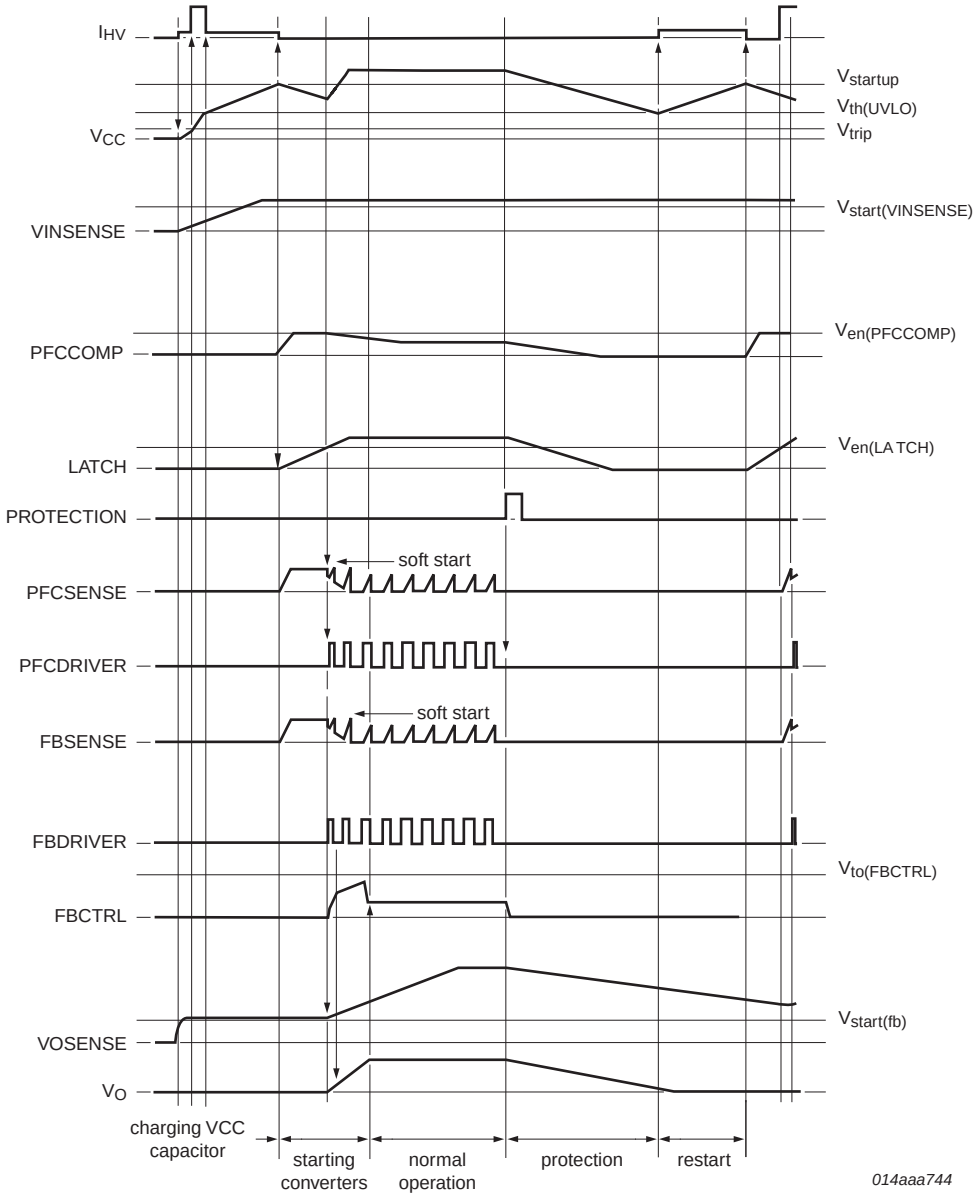


Fig 5. Start-up sequence at low mains voltage

The charge time of the soft-start capacitors can be chosen independently for the PFC and the flyback, based on their values.

3.3 V_{CC} cycle in safe restart protection mode

In Safe restart mode the controller goes through the steps 3 to 8 as described in Section 3.2.

3.4 Mains voltage sensing and brownout

The mains input voltage is measured through the VINSENSE pin. When the VINSENSE pin has reached $V_{start(VINSENSE)}$ (1.15 V) the PFC starts switching, but only if the other start conditions are met as well, see Section 3.1. As soon as the voltage on pin VINSENSE drops below $V_{stop(VINSENSE)}$ (0.89 V), the PFC stops switching. The flyback however, continues switching until its maximum on-time protection, $t_{on(fb)max}$ (40 μs) is triggered. When this protection is triggered, the IC stops switching and enters Safe restart mode.

The voltage on pin VINSENSE must be an average DC value, representing the mains input voltage. The system works optimally using a time constant of approximately 150 ms at the VINSENSE pin.

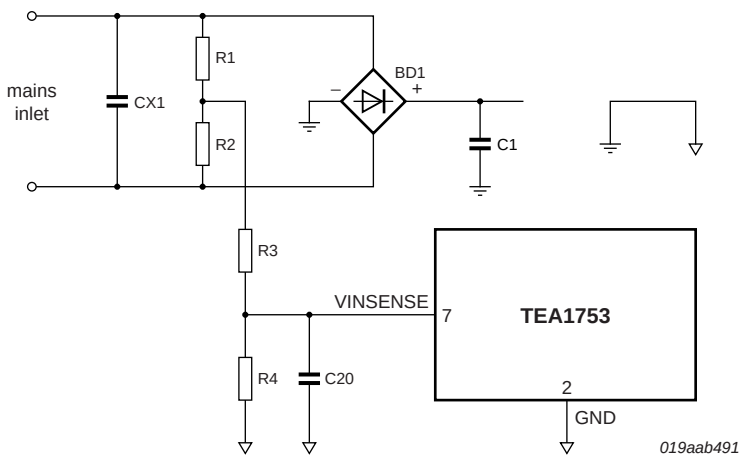


Fig 6. VINSENSE circuitry

3.4.1 Discharge of mains input capacitor

The X-capacitors in the ElectroMagnetic Compatibility (EMC) input filtering must be discharged using a time constant of $\tau < 1$ second for safety reasons (see Ref. 1).

In a typical 90 W adapter application with CX1 = 220 nF, the replacement value resistor value R_V is determined by:

$$R_V = R + \frac{R \times (R_3 + R_4)}{R + R_3 + R_4} \quad (1)$$

Where:

- $R = R_1 = R_2$

The value of R_V must be lower than or equal to the following:

$$R_V \leq \frac{\tau}{CX1} = \frac{1}{220\ nF} = 4.55\ M\Omega$$

3.4.2 Brownout voltage adjustment

The rectified AC input voltage is measured via R1 and R2. Each resistor alternately senses half the sine wave, so both resistors must have the same value. The average voltage sensed at the connection of R1 and R2 is calculated using Equation 2:

$$V_{avg} = \frac{2 \times \sqrt{2}}{\pi} \cdot V_{acrms} \quad (2)$$

The V (AC) brownout RMS level is calculated using Equation 3:

$$V_{brownout}\ (AC) = \frac{\pi}{2 \times \sqrt{2}} \times V_{stop(VINSENSE)} \times \frac{(R_V + R_3 + R_4)}{R_4} \quad (3)$$

Where: $V_{stop(VINSENSE)}$ = 0.89 V

At a brownout threshold of 68 V (AC) and in compliance to *IEC-60950 chapter 2.1.1.7 "discharge of capacitors in equipment"* (Ref. 1). Example values are shown in Table 2.

Table 2. VINSENSE component values

CX1	R1	R2	R3	R4
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

A value of 3.3 μF for capacitor C20, with 47 kΩ at R4, gives the recommended time constant of ~150 ms at the VINSENSE pin.

3.4.3 Minimizing the influence of the dark-current of the optocoupler

Dark current is the leakage current of the transistor inside the optocoupler. This current is temperature and voltage dependent. Figure 7 shows the proposed circuit that can handle dark-current up to 10 μA.

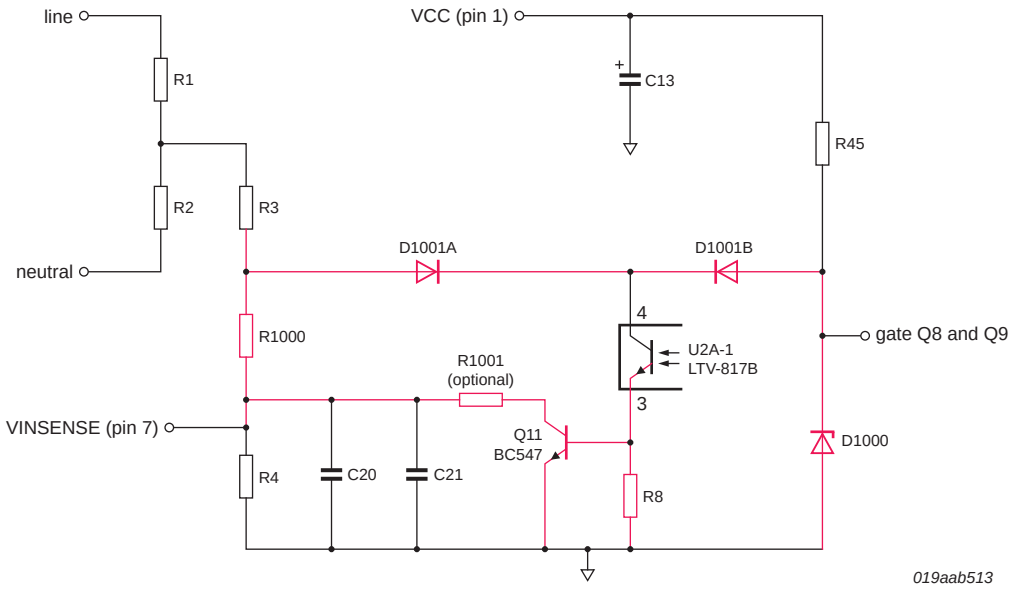


Fig 7. The proposed VSENSE circuit for minimizing the influence of the dark current

The principle of the design is: the VINSENSE voltage should be able to first reach the sum of $V_{th(pd)}$ and $V_{hys(pd)}$ before the internal HV current source inside the IC is enabled. The TEA1753 V_{CC} supply voltage increases and support any dark current (up to 10 μA) needed for the optocoupler.

The VINSENSE voltage cannot be influenced anymore by the dark current of the optocoupler. The red colored components have to be added in comparison with the schematic given in Figure 1. Diode D1001A and D1001B are available in one component. Two resistors in Figure 1 can be removed if Figure 8 is added, these two are R42 and R43.

3.5 Internal Overtemperature Protection (OTP)

The IC has an internal temperature protection to protect the IC from overheating by overloads at the V_{CC} pin. When the junction temperature exceeds the thermal shutdown temperature, the IC stops switching. As long as the OTP is active, the V_{CC} capacitor is not recharged from the HV mains. The OTP circuit is supplied from the HV pin if the V_{CC} supply voltage is not sufficient. The OTP is a latched protection.

3.6 LATCH pin

The LATCH pin is a general purpose input pin which can be used to latch both converters off. The pin sources a bias current $I_{O(LATCH)}$ of 80 μA for the direct connection of an NTC. When the voltage on this pin is pulled below 1.25 V, switching of both converters is stopped immediately and V_{CC} starts cycling between the $V_{th(UVLO)}$ and $V_{startup}$ without a restart. Switching off and then switching on the mains input voltage triggers the fast latch reset circuit and resets the latch (see Section 3.7).

At start-up, the LATCH pin has to be charged to above 1.35 V before both converters can be enabled. Charging of the LATCH pin starts when $V_{CC} = V_{startup}$.

No internal filtering is present at the LATCH pin. A 10 nF capacitor must be placed between this pin and the IC GND pin to prevent false triggering, also when the LATCH pin function is not used.

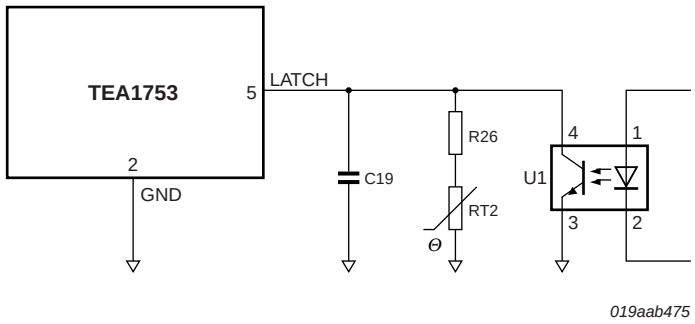


Fig 8. Usage of the LATCH pin protection

Latching on application overtemperature occurs when the total resistance value of the NTC and its series resistor drops below the following:

$$R_{OTP} = \frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = \frac{1.25\ V}{80\ \mu A} = 15.6\ k\Omega \quad (4)$$

The optocoupler triggers the latch if the driven optotransistor conducts more than 80 μA.

3.7 Fast latch reset

Switching off and then switching on the mains input voltage resets the latched protection. After the mains input is switched off, the voltage on pin VINSENSE drops below V_{flr} (0.75 V). This triggers the fast latch reset circuit, but does not reset the latched protection. After the mains input is switched on, the voltage on pin VINSENSE rises again. The latch is reset when the level has passed 0.85 V. The system restarts when the V_{CC} pin is charged to $V_{startup}$ (See step 4 of Section 3.2).

4. PFC description and calculation

The PFC operates in QR mode or DCM mode with valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to 250 kHz to reduce switching losses. If necessary, one or more valleys are skipped to keep the frequency below 250 kHz.

The PFC of the TEA1753 is designed as a dual boost converter with two output voltage levels that are dependent on the mains input voltage range. The advantage is that the overall system efficiency at low mains is improved because of the reduction of the PFC switching losses. In low and medium power adapters (< 120 W) the contribution of PFC switching losses to the total losses is relatively high.

The dual output voltage is controlled by an internal current source of 8 μA at pin VOSENSE. As shown in Figure 9, the mains input voltage measured at pin VINSENSE is used to control the internal current source. This current source, in combination with the resistors at pin VOSENSE, sets the lower PFC output voltage. At high mains, the current source is switched off. Therefore, the maximum PFC output voltage is not affected by the accuracy of the current source. In a typical adapter with a PFC output voltage of 385 V (DC) at high mains, the PFC output voltage is 250 V (DC) at low mains. A voltage of 2.2 V at pin VINSENSE corresponds with a mains input voltage of approximately 180 V (AC). The small slope at the transfer function ensures a stable switchover of the PFC output voltage without hiccups.

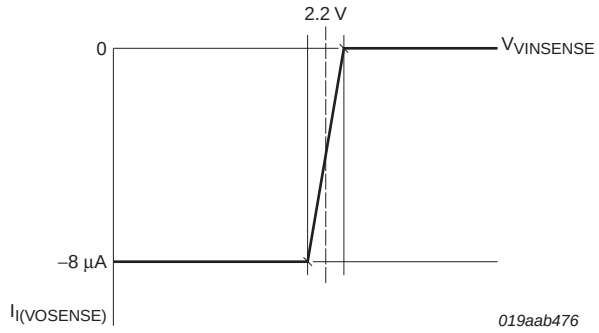


Fig 9. Transfer function of VINSENSE voltage to dual boost current at VOSENSE

The PFC is switched off to ensure high efficiency during low output currents. After switch-off the bulk elcap voltage drops to $line\ voltage \times \sqrt{2}$.

4.1 PFC output power and voltage control

The PFC of the TEA1753 is on-time controlled, therefore it is not necessary to measure the mains phase angle. The on-time is kept constant during the half sine wave to obtain a good Power Factor (PF) and a class-D Mains Harmonics Reduction (MHR).

The PFC output voltage is controlled through the VOSENSE pin. At the VOSENSE pin there is a transconductance error amplifier with a reference voltage of 2.5 V. The error at the VOSENSE pin is converted with 80 μA/V to a current on pin PFCCOMP. The voltage on pin PFCCOMP, in combination with the voltage on pin VINSENSE, determines the PFC on-time.

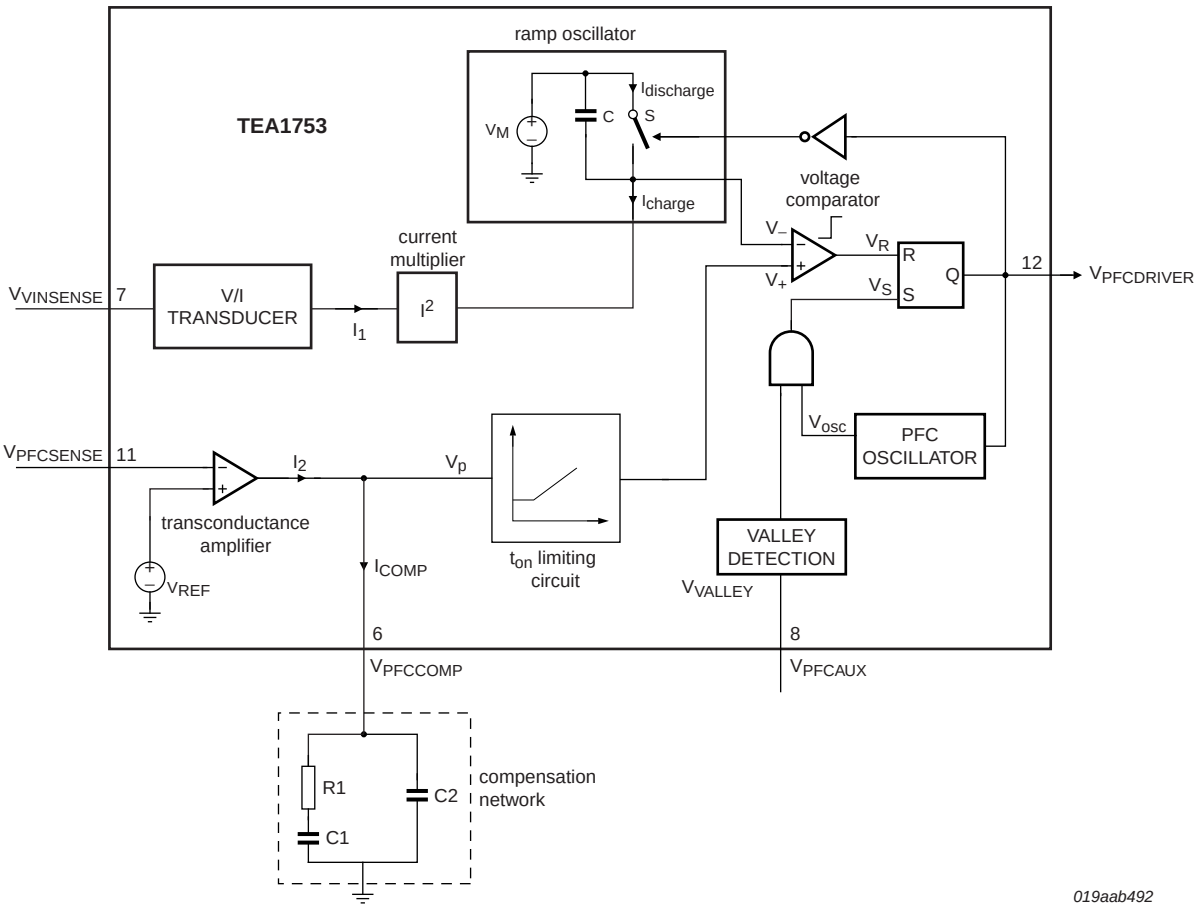


Fig 10. PFC on-time control

A network with one resistor and two capacitors at the PFCCOMP pin is used to stabilize the PFC control loop. The mathematical equation for the transfer function of a boost converter contains the square of the mains input voltage. In a typical application this results in a low regulation bandwidth for low mains input voltages and a high regulation bandwidth at high input voltage. The result might be that at high mains input voltages it can be difficult to meet the MHR requirements. The TEA1753 uses the mains input voltage measured through the VINSENSE pin to compensate the control loop gain as a function of the mains input voltage. As a result the gain is constant over the entire mains input voltage range.

The voltage at the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimally with a time constant of approximately 150 ms at the VINSENSE pin.

4.1.1 Setting the PFC output voltage

The PFC output voltage is set with a resistor divider between the PFC output voltage and the VOSENSE pin. In Normal mode, the PFC output voltage is regulated so that the voltage on the VOSENSE pin is equal to $V_{reg(VOSENSE)} = 2.5\ V$.

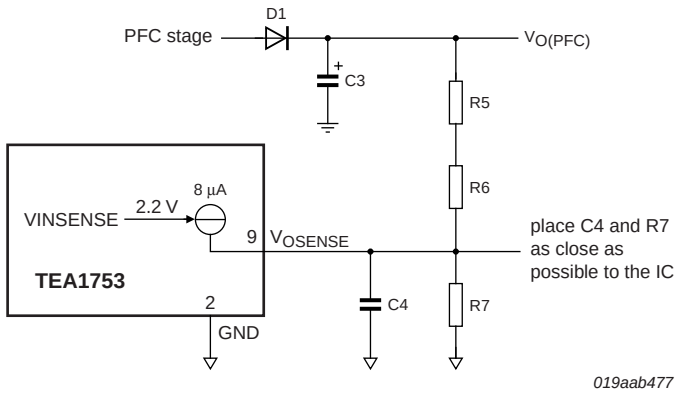


Fig 11. PFC output voltage setting

Two resistors of 9.1 MΩ (1 %) can be used between the bulk elcap and the VOSENSE pin. The dimensioning of the $I_{bst(dual)}$ current source (−8 µA) has been adapted to the use of these resistor values. With a resistor value of 9.1 MΩ for R5 and R6 and 120 kΩ to 118 kΩ for R7 a universal mains adapter has a PFC output voltage of approximately 380 V to 390 V at high mains and 235 V to 238 V at low mains.

The resistor R7 (1 %) value connected between the VOSENSE pin and ground is calculated using Equation 5:

$$R7 = \frac{(R5 + R6) \times V_{reg(VOSENSE)}}{(V_{O(PFC)} - V_{reg(VOSENSE)})} \quad (5)$$

Example using a regulated PFC output voltage of 382 V:

$$R7 = \frac{(9.1\ M\Omega + 9.1\ M\Omega) \times 2.5\ V}{(382\ V - 2.5\ V)} = 120\ k\Omega\ (1\ \%)$$

At low mains the 8 µA current source $I_{bst(dual)}$ is active. The lower PFC output voltage is calculated using Equation 6:

$$V_{O(PFC)low} = \frac{R5 + R6 + R7}{R7} \cdot (V_{reg(VOSENSE)} - I_{bst(dual)} \cdot R7) \quad (6)$$

Example for calculating the lower PFC output voltage:

- R5 and R6 = 9.1 MΩ
- R7 = 120 kΩ

$$V_{O(PFC)low} = \frac{9.1\ M\Omega + 9.1\ M\Omega + 120\ k\Omega}{120\ k\Omega} \cdot (2.5\ V - 8\ \mu A \cdot 120\ k\Omega) = 235\ V$$

The function of capacitor C4 at the VOSENSE pin is to filter noise and to prevent false triggering of the protection modes because of MOSFET switching noise, mains surge events or ElectroStatic Discharge (ESD) events. False triggering of the $V_{ovp(VOSENSE)}$ protection can cause audible noise and disturbance of the AC mains input current.

False triggering of the $V_{th(ol)(VOSENSE)}$ protection causes a safe restart cycle. A time constant of 500 ns to 1 μs at the VOSENSE pin should be sufficient, which results in a value of 4.7 nF for capacitor C4.

It is advisable to place R7 and C4 as close as possible to the IC between the VOSENSE pin and the IC GND pin.

4.1.2 Calculation of the PFC soft-start and soft-stop components

The soft-start and soft-stop are implemented through the RC network at the PFCSENSE pin.

R_{SS1} must have a minimum value of 12 kΩ to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable the start-up of the PFC. See Section 3.2 for a description of start-up.

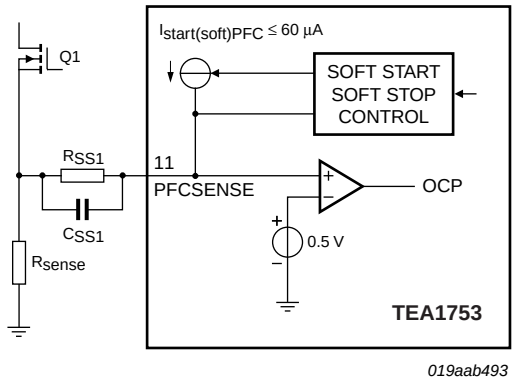


Fig 12. PFC soft-start and soft-stop

The total soft-start or soft-stop time is: $t_{soft\text{-}start} = 3 \times R_{SS1} \times C_{SSI}$

It is advised to keep the soft-start time of the PFC shorter than the soft-start time of the flyback. It is also advised that the soft-start time is kept within a range of 2 ms to 5 ms.

using C6 = 100 nF and R11 = 12 kΩ, the total soft-start time is 3.6 ms.

4.2 PFC demagnetizing and valley detection

The PFC MOSFET is switched on after the transformer is demagnetized. The internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next primary stroke is started when the voltage across the PFC MOSFET is at its minimum in order to reduce switching losses and electromagnetic interference (EMI) (valley switching).

The maximum switching frequency of the PFC is limited to 250 kHz to reduce the switching losses. If necessary, one or more valleys are skipped to keep the frequency below 250 kHz.

If no demagnetization signal is detected on pin PFCAUX, the controller generates a Zero Current Signal (ZCS) 50 μs after the last PFC gate signal. If no valley signal is detected on this pin, the controller generates a valley signal 4 μs after demagnetization was detected.

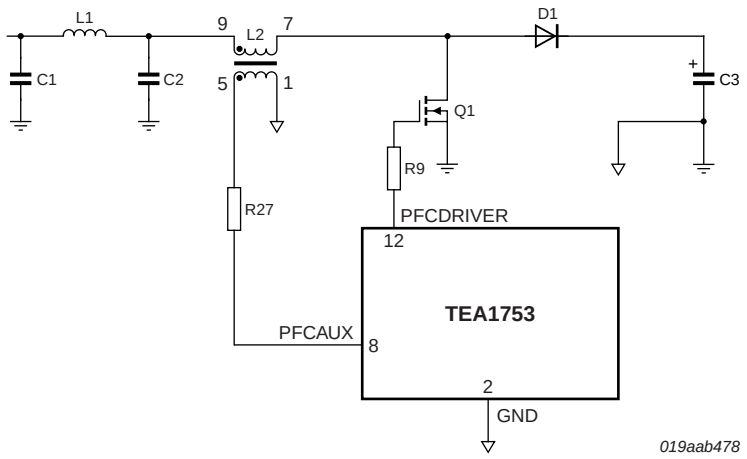


Fig 13. PFCAUX circuitry

4.2.1 Design of the PFCAUX winding and circuit

It is advised to set the voltage on pin PFCAUX as high as possible, but still within the absolute maximum voltage rating of ± 25 V. Doing this improves the valley detection at low ringing amplitudes.

Taking into account its absolute maximum rating of ± 25 V, the voltage on pin PFCAUX must be set as high as possible to guarantee valley detection at low ringing amplitudes.

The number of turns of the PFCAUX winding is calculated using Equation 7:

$$N_{aux\_max} = \frac{V_{PFCAUX}}{V_{Lmax}} \times N_p = \frac{25\ V}{V_{Lmax}} \times N_p \quad (7)$$

- V_{PFCAUX} is the absolute maximum rating of the PFCAUX pin
- V_{Lmax} is the maximum voltage across the PFC primary winding

The PFC output voltage at the PFC_{OVP} level determines the maximum voltage across the PFC primary winding and is calculated using Equation 8:

$$V_{Lmax} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \times V_{O(PFC)} = \frac{2.63\ V}{2.5\ V} \times V_{O(PFC)} \quad (8)$$

When a PFC coil with a higher number of auxiliary turns is used, a resistor voltage divider can be placed between the auxiliary winding and pin PFCAUX. The total resistive value of the divider should be lower than 10 kΩ to prevent delay of the valley detection by parasitic capacitance.

The polarity of the signal at the PFCAUX pin must be reversed compared to the PFC MOSFET drain signal.

It is recommended to have a 5 kΩ resistor between the PFC auxiliary winding and pin PFCAUX to protect the pin against electrical overstress, for example, during lightning surge events. This resistor should be placed as close as possible to the IC to prevent incorrect valley switching of the PFC because of external disturbances.

4.3 PFC protection modes

4.3.1 VOSENSE overvoltage protection

Overvoltage can occur across the bulk elcap during the initial start-up and large load changes. This overvoltage is caused by the relative slow response of the PFC control loop. The PFC control loop response must be relatively slow to guarantee a good power factor and meet the MHR requirements. The OverVoltage Protection (OVP) at the VOSENSE pin limits the overvoltage. When the $V_{ovp(VOSENSE)}$ level of 2.63 V is detected, the PFC MOSFET is switched off immediately regardless of the on-time setting. The switching of the MOSFET remains blocked until the voltage on pin VOSENSE drops below 2.63 V again.

When the resistor between the VOSENSE pin and ground is open, the OVP is also triggered.

The peak voltage across the bulk elcap generated by the PFC because of an overshoot and limited by the PFC OVP is calculated using Equation 9:

$$V_{O(PFC)peak} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot V_{O(PFC)nominal} = \frac{2.63\ V}{2.5\ V} \cdot V_{O(PFC)nominal} \quad (9)$$

4.3.2 VOSENSE open and short pin detection

The VOSENSE pin, which is sensing the PFC output voltage, has an integrated protection circuit to detect an open and short circuited pin. This pin can also sense that one of the resistors in the voltage divider is open. Therefore the VOSENSE pin is completely fail-safe. It is not necessary to add an external OVP circuit for the PFC. An internal current source pulls the pin down to below the $V_{th(ol)(VOSENSE)}$ detection level (1.15 V) when the pin is open. When $V_{th(ol)(VOSENSE)}$ is detected, level switching of the PFC and the flyback MOSFETs is blocked until the voltage on pin VOSENSE rises to above 1.15 V again.

4.3.3 VINSENSE open pin detection

The VINSENSE pin, which senses the mains input voltage, has an integrated protection circuit for detecting an open pin. An internal current source pulls the pin down to below $V_{stop(VINSENSE)}$ (0.89 V) when the pin is open.

4.3.4 Overcurrent protection

The overcurrent protection limits the maximum current through the PFC MOSFET and PFC coil. The current is measured via a current sense resistor in series with the MOSFET source. The MOSFET is switched off immediately when the voltage at pin PFCSENSE exceeds the $V_{sense(PFC)max}$ level of 0.52 V at dV/dt = 50 mV/µs. The OCP is a switching-cycle-by-switching-cycle protection.

It is recommended to take into account a margin of 0.1 V to avoid false triggering of the PFC OCP by switching of the flyback. False triggering of the $V_{sense(PFC)max}$ protection can cause disturbances to the AC mains input current. It is also advised that a small capacitor between 100 pF and 220 pF is placed directly at the PFCSENSE pin to suppress external disturbance.

The current sense resistor is calculated using Equation 10:

$$R_{OCP(PFC)} = \frac{V_{sense(PFC)max} - V_{margin}}{I_{pQR(PFC)max}} = \frac{0.52\ V - 0.1\ V}{I_{pQR(PFC)max}} \quad (10)$$

Where: $I_{pQR(PFC)max}$ is the maximum PFC peak current at the high load and low mains.

The maximum peak current for the PFC operating in Quasi-resonant mode is calculated using Equation 11:

$$I_{pQR(PFC)max} = \frac{2\sqrt{2} \cdot P_{i(max)} \cdot 1.1}{Vac_{min}} = \frac{2\sqrt{2} \cdot \frac{P_{o(max)}}{\eta} \cdot 1.1}{Vac_{min}} \quad (11)$$

Where:

- $P_{o(max)}$ is the maximum output power of the flyback
- 1.1 is a factor to compensate for the dead time between zero current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in Quasi-resonant mode
- η is the expected efficiency of the total converter at maximum output power
- Vac_{min} is minimum mains input voltage.

5. Flyback description and calculation

5.1 Flyback output power control

An important aspect of the TEA1753 flyback system is that it waits until the transformer is demagnetized and at least one valley has appeared before it is magnetized again for the next cycle. The FBAUX pin detects demagnetization via the auxiliary winding. The HV pin detects the bottom of the valley via the drain of the MOSFET or the central tap of the primary winding.

The output power (P_O) of the flyback is calculated using Equation 12:

$$P_O = \frac{1}{2} \cdot L_p \cdot I_p^{\ 2} \cdot fs \cdot \eta \quad (12)$$

Where:

- L_p stands for the primary inductance of the flyback transformer
- I_p stands for the peak current through the flyback transformer
- f_S stands for operating frequency of the flyback
- η stands for the efficiency of the flyback

L_p is selected at the start of the design, so the setting of the primary peak current controls the output power. The switching frequency is a result of external application parameters and internal IC parameters.

External application parameters are the transformer turns ratio, the primary inductance, the drain source capacitance, the input voltage, the output voltage and the feedback signal from the control loop. Internal IC parameters are the oscillator setting, the setting of the peak current and the detection of demagnetization and valley.

Another logical method of controlling the output power is keeping the primary peak current I_p fixed and changing the operating frequency. Output power and operating frequency are linearly related during this type of control. This method is usually only done at low output power. In this application note it is called "operating in Frequency reduction mode" (See Section 5.1.1.3).

The input voltage of the flyback is measured through pin FBAUX and used to implement an OverPower Protection (OPP). The OPP keeps the maximum output power of the flyback constant over the input voltage.

The flyback has an accurate OverVoltage Protection (OVP) circuit. The overvoltage is measured through pin FBAUX. Both controllers (flyback and PFC) are switched off in a latched protection when an overvoltage is detected.

5.1.1 Three different operation modes of the TEA1753

At initial start-up, the flyback always starts at the maximum output power. This means that the system starts up in the so-called Quasi-resonant mode. The flyback of the TEA1753 passes through three operation modes (see Figure 14) from maximum to minimum output power:

- Quasi-Resonant (QR) mode
- Discontinuous Conduction Mode (DCM)
- Frequency Reduction (FR) mode

Demagnetization detection and valley switching circuitry inside the IC is active in all three different operation modes.

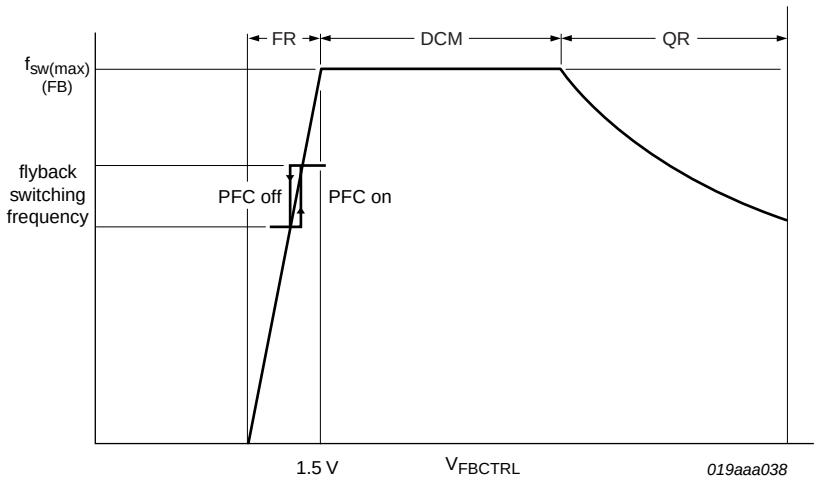


Fig 14. Flyback operation modes

5.1.1.1 Quasi-resonant mode

The flyback operates in Quasi-resonant mode at high and maximum output power. The output power is controlled by the peak current (see Section 5.1). A lower peak current than the maximum allowed value results in lower output power and a higher operating

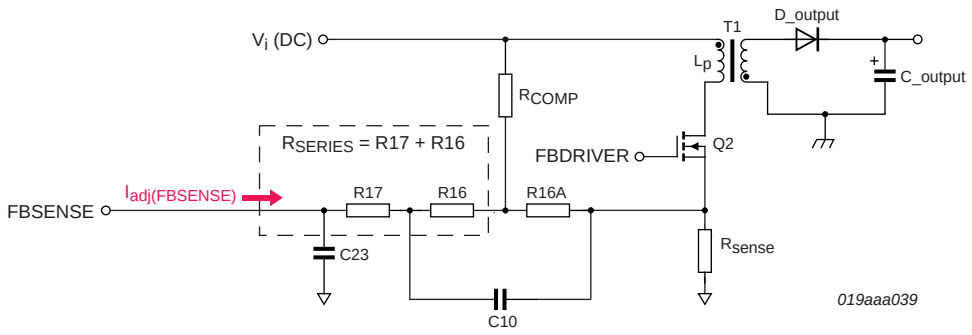
frequency until the maximum operating frequency is reached. The Quasi-resonant mode can easily be recognized. The next primary switching cycle starts when the bottom of the first valley is detected.

The primary peak current (I_p) is set by the voltage on pin FBCTRL. It is advised to place a 10 nF noise filter capacitor (C15) as close as possible to the FBCTRL pin to avoid disturbance of the flyback by switching of the PFC MOSFET. The voltage on pin FBCTRL is measured back at the FBSENSE pin and is calculated using Equation 13 (only valid during QR mode or DCM):

$$V_{sense(fb)} \cong 0.66 \times V_{FBCTRL} - I_{adj(FBSENSE)} \times (R16 + R17) - 0.69\ V \quad (13)$$

Where:

- V_{FBCTRL} is allowed to vary between the 1.5 V and 2.0 V (only valid during QR mode or DCM mode)
- $I_{adj(FBSENSE)}$ is related to a current source inside the IC, connected to the FBSENSE pin
- Resistors R16 and R17 are found in the circuit diagram, see Figure 15.



FBSENSE has two internal reference levels:

(1) $V_{sense(fb)max}$ = 0.630 V at dV/dt = 0 mV/µs

(2) $V_{sense(fb)min}$ = 0.300 V at dV/dt = 0 mV/µs

Fig 15. Most important components for adjusting the flyback in the application

The peak current I_p through the flyback transformer is defined by:

$$I_p = \frac{V_{sense(fb)} - I_{adj(FBSENSE)} \times \{R16 + R17\}}{R_{sense}} \quad (14)$$

The maximum peak current I_{pmax} is determined by $V_{sense(fb)max}$. R16A is not mentioned in Equation 14, but this is explained in Section 5.1.5. Usually the required output power continues to drop after the initial start-up. This results in the flyback entering the Discontinuous conduction mode when the maximum switching frequency is reached.

5.1.1.2 Discontinuous conduction mode

In DCM the output power is reduced by a further reduction of the peak current (I_p) and by skipping one or more valleys at the same time. In this mode the switching frequency is kept more or less constant. The exact switching frequency depends on the detection of the valleys, but it is never higher than the maximum frequency.

The output power is decreased by reducing the peak current and as a result more valleys are skipped until the voltage across FBCTRL drops below 1.5 V. When this happens the operating mode shifts from DCM to FR mode.

Sometimes the DCM is not reached when the selected primary inductance value of the transformer is too large. In such a situation the flyback skips the DCM when it is reducing power, it jumps directly from the QR mode to the FR mode.

5.1.1.3 Frequency reduction mode

The voltage across the FBCTRL pin in Frequency reduction mode no longer sets the peak current. Instead it sets the operating frequency. The minimum peak current (I_{pmin}) through the transformer is kept constant during the FR mode.

The ratio between I_{pmin} and I_{pmax} depends mainly on the value of the sense resistor R_{sense}, assuming that the core is not saturated at I_{pmax}. The output power is reduced by reducing the operating frequency and as a result more valleys are skipped.

The operating frequency of the flyback during FR mode determines if the PFC is turned on or turned off. The turn-on operating frequency for enabling the PFC is selected at a higher rate than the turn-off operating frequency. So the PFC is turned on at a higher output power and turned off again at a lower output power.

In general the output voltage of an adapter is fixed, so a higher or lower output power of the flyback results in a higher or lower output current.

The overall efficiency of the system is improved if the PFC is disabled at low output currents. For this reason the PFC is turned off above 25 % of the nominal output current. On the other hand, the PFC is turned on at larger output currents in order to improve the power factor of the line current. This is often done below 50 % of the nominal output current.

The hysteresis between turning on and turning off the PFC depends on the primary inductance value, the output power and the line voltage. It is therefore important to select the right inductance value to ensure enough PFC on/PFC off hysteresis. Section 5.1.2 describes how this is done.

5.1.2 The relationship between inductance value and the hysteresis of the PFC

The TEA1753 runs using a fixed minimum peak current (I_{pmin}) to control the output power during the Frequency reduction mode, see Section 5.1 (the value of I_{pmin} is calculated in Equation 17). Therefore the on-time (conducting time of the MOSFET) depends on the selected inductance value and the input voltage, it is linearly related to the inductance value and inversely proportional to the input voltage. The relationship between on-time and off-time of the MOSFET is fixed via the turns ratio of the transformer and the output voltage (neglecting the influence of the relatively short valley time). At lower line voltages the operating frequency and output power decrease when a relatively large primary inductance is selected, see also Section 5.1 and Figure 16.

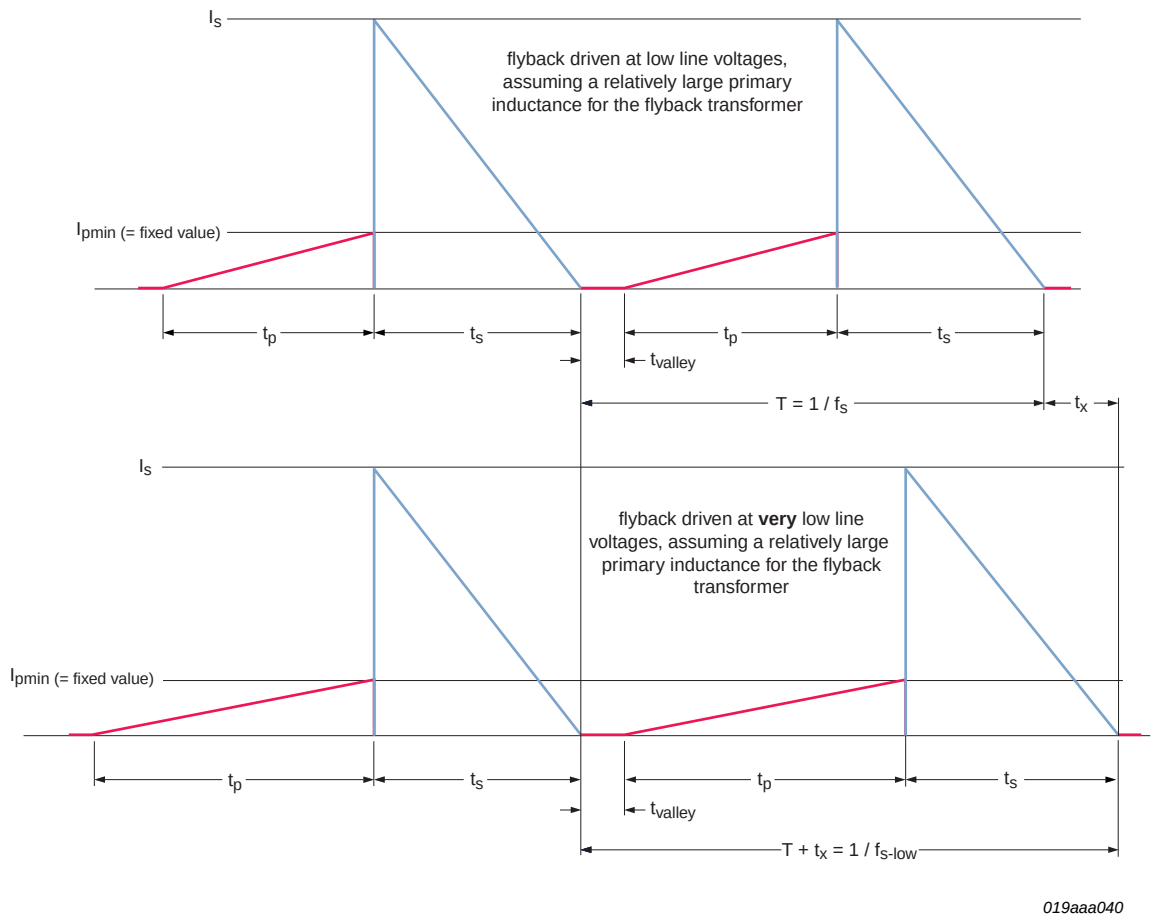
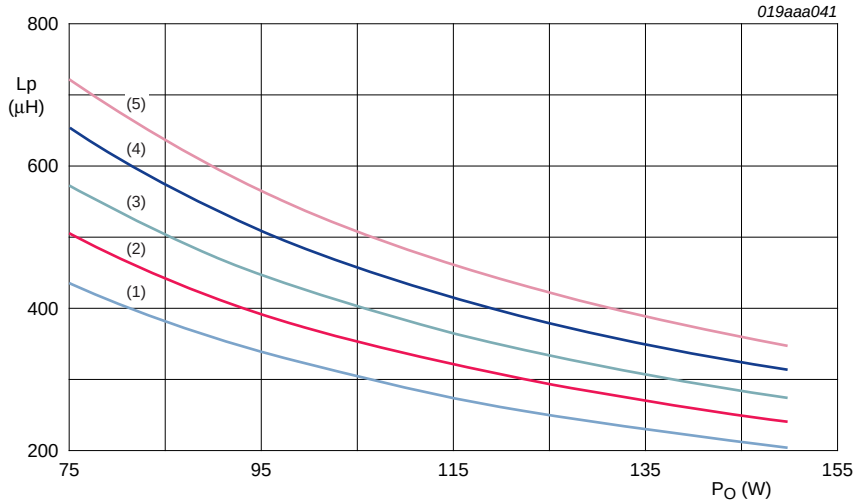


Fig 16. Operating frequency as a function of (low) line voltages, assuming a relatively large selected primary inductance value for the flyback transformer

The situation becomes worse when the primary inductance value is increased as well, because this limits the maximum deliverable output power at low line voltages even more (by default the flyback runs at a lower operating frequency, assuming a fixed peak current). In practice this means that the flyback supports a limited amount of power at low line voltages. Asking more power activates the feedback loop and results in enabling the PFC at lower output power than was originally intended. In other words, the hysteresis between turning on and turning off the PFC becomes smaller at low line voltages in comparison to typical line voltages, assuming that a relatively large primary inductance value for the transformer is selected. When the selected primary inductance value is much too large, unwanted system behavior occurs, because there is no hysteresis left. The maximum inductance value should be limited to prevent this unwanted system behavior at low line voltages.

Most customers prefer a certain minimum hysteresis between turning on and turning off the PFC at low line voltages. So it is helpful to have an indication of the acceptable maximum primary inductance value of the transformer at the start of the design. Note that several assumptions have to be made to calculate these inductance values in Figure 17. Therefore these values should only be thought of as indications.



$L_p = f(P_O)$

Assumptions: Minimum voltage across the buffer capacitor (C3) is approximately 100 V (DC) at 50 % of the nominal output power.

(1) $N \times (V_O + V_f) = 80$ V

(2) $N \times (V_O + V_f) = 92$ V

(3) $N \times (V_O + V_f) = 104$ V

(4) $N \times (V_O + V_f) = 118$ V

(5) $N \times (V_O + V_f) = 130$ V

Fig 17. Indication of the maximum primary inductance value, related to output power and $N \times (V_O + V_f)$

Figure 17 shows an indication value for the maximum primary inductance value of the flyback at different output powers and different turn ratios. Selecting a larger value than proposed here can result in too much loss of hysteresis. Selecting a smaller value prevents that, but causes more overall switching losses. The inductance values shown in Figure 17 results in loss of some hysteresis below roughly 115 V (AC) line voltage. However, they are usually still acceptable at 90 V (AC), assuming that the voltage across bulk elcap C3 does not drop too much. A rule of thumb is that the value of the buffer capacitor C3 in microfarads is usually selected equal to the output power in Watts. Applying this general rule of thumb results in a minimum voltage across the buffer capacitor of approximately 100 V (DC) at 90 V (AC) line voltage at 50 % of the nominal output power.

Selecting the inductance value with the help of Figure 17 is one method. Another method is using Equation 15:

$$L_p = \left(\frac{N \times (V_O + V_f)}{104.3}\right) \times 43061 \times 10^{-6} \times (I_{O(nom)} \times (V_O + V_f))^{-1.0005} \quad (15)$$

Where:

- $I_{O(nom)}$ stands for the nominal output current according to the type plate of the adapter
- V_O stands for the output voltage
- V_f stands for forward voltage across the secondary diode

- L_p stands for the primary inductances of the flyback transformer
- N is the turns ratio between the primary and secondary windings (N_p/N_s)

Equation 15 gives some deviation at a low and a high value of the $N \times (V_O + V_f)$ product. It is therefore recommended to keep this value between 80 V and 130 V.

Example:

- $I_{O(nom)}$ = 4.62 A
- V_O = 19.5 V
- V_f = 0.05 V
- $N \times (V_O + V_f)$ = 104.3

$$L_p = \left(\frac{104.3}{104.3}\right) \times 43061 \times 10^{-6} \times (4.62 \times (19.5 + 0.05))^{-1.0005} = 476 \times 10^{-6}\ H$$

The final value used is 450 μH.

5.1.3 Relationship between I_{pmin} and the required PFC-on/off level

The PFC is usually turned on and turned off between 50 % and 25 % of the nominal output current of the flyback. The PFC can only be turned on or turned off by the flyback when it is running in FR mode. The typical internal operating frequency of the flyback for turning on the PFC is 86 kHz and for turning off the PFC is 48 kHz. Using the average of both values (percentage wise and frequency wise) in combination using Equation 12 results in Equation 16:

$$0.375 \times I_{O(nom)} \times (V_O + V_f) = \frac{1}{2} \times L_p \times I_{pmin}{}^2 \times 67000 \times \eta_{fb} \quad (16)$$

or:

$$I_{pmin} = \sqrt{\frac{2 \times 0.375 \times I_{O(nom)} \times (V_O + V_f)}{L_p \times 67000 \times \eta_{fb}}} \quad (17)$$

Where:

- 0.375 is the average value of 50 % and 25 % of the nominal output current
- V_O is the output voltage
- V_f is forward voltage across the secondary diode
- L_p is the primary inductances of the flyback transformer
- 67000 is the average value of 86000 Hz and 48000 Hz
- η_{fb} is the efficiency of the flyback (please use relatively high values, such as 0.97…0.98)

Example:

- $I_{O(nom)}$ = 4.62 A
- V_O = 19.5 V
- V_f = 0.05 V
- L_p = 450 μH
- η_{fb} = 0.98

$$I_{pmin} = \sqrt{\frac{2 \times 0.375 \times 4.62 \times (19.5 + 0.05)}{450 \times 10^{-6} \times 67000 \times 0.98}} = 1.514\ A$$

5.1.4 The influence of R_{sense} and the series resistance R16 + R17

The sense resistor, R_{sense}, together with the series impedance R16 and R17, has four functions:

- Prevent or minimize the risk of saturation of the flyback transformer.
- Allow enough power to the output (assuming the inductance is not going into saturation).
- Allow some adjustment for enabling or disabling the PFC at a certain output power level. Note that the value of R_{sense} is more dominant for this adjustment than the values of R16 and R17, as their influence is much smaller.
- R17 and C23 prevent FBSENSE being charged negative because of disturbances across R_{sense}.

The saturation level ($I_{p(sat)}$) of the transformer and the value of the sense resistor are important design parameters. Section 5.1.4.1 shows the calculation for the saturation level of the transformer. After that the maximum peak current (I_{pmax}) through the transformer is determined. This value should preferably be below the saturation level of the transformer.

5.1.4.1 Calculating the saturation current $I_{p(sat)}$ of the flyback transformer

The saturation level of a transformer is calculated using Equation 18.

$$I_{p(sat)} = \frac{N_p \times B_{max} \times A_e}{L_p} \quad (18)$$

Example based on the following assumptions:

- N_p = 32 turns
- B_{max} = 390 mT (PQ3220, material PC44, B_{max} at 100 °C)
- A_e = 170 × 10^{-6} m^2 (from transformer supplier data sheet)
- L_p = 450 × 10^{-6}

Result: $I_{p(sat)} = \frac{32 \times 0.39 \times 170 \times 10^{-6}}{450 \times 10^{-6}} = 4.71\ A$

Values for A_e and B_{max} can be found in the data sheet of the transformer supplier. The B_{max} value depends on temperature. It decreases rapidly at high operating temperatures. Therefore the B_{max} value should be selected at high operating temperatures. Saturation of the core does not happen when the maximum peak current (I_{pmax}) is below the saturation current ($I_{p(sat)}$). Section 5.1.4.2 shows the calculation of I_{pmax}. A saturated core does not deliver more power to the output, but only deteriorates the overall performance of the system (more stress and EMI and, worst case, a possible system failure).

5.1.4.2 Calculation of I_{pmax} for flyback operating in Quasi-resonant mode

The flyback peak current operating in quasi-resonant mode is calculated using Equation 19:

$$I_{pmax} = \frac{-b + \sqrt{(b^2 - 4 \times a \times c)}}{2 \times a} \quad (19)$$

Where:

- $a = N \times V_{i(DC)min} \times L_p$
- $b = -2 \times I_O \times L_p \times \{N \times (V_O + V_f) + V_{i(DC)min}\}$
- $c = -2 \times I_O \times t_{valley} \times N \times V_{i(DC)min} \times (V_O + V_f)$

For a, b and c:

- V_O is the output voltage
- N is the turns ratio between the primary and secondary windings (N_p/N_s)
- L_p is the inductance value of the primary winding
- t_{valley} is the valley time, sometimes also described as dead time. This time is usually around the 1.1 μs
- $V_{i(DC)min}$ is the minimum voltage across bulk elcap C3 at its nominal output load. In this example this is 75 V (DC). The actual voltage depends on how fast the PFC is enabled. It is therefore recommended to check this value in every application.

Examples:

- $a = 5.3333 \times 75 \times 450 \times 10^{-6} = 180 \times 10^{-3}$
- $b = -2 \times 4.62 \times 450 \times 10^{-6} \times \{5.3333 \times (19.5 + 0.05) + 75\} = -745.39 \times 10^{-3}$
- $c = -2 \times 4.62 \times 1.1 \times 10^{-6} \times 5.3333 \times 75 \times (19.5 + 0.05) = -79.4824 \times 10^{-3}$

$$I_{pmax}\ (at\ I_O = 4.62\ A) = \frac{745.39 \times 10^{-3} + \sqrt{(-745.39 \times 10^{-3})^2 - 4 \times 180 \times 10^{-3} \times -79.4824 \times 10^{-3}}}{2 \times 180 \times 10^{-3}} = 4.25\ A$$

The calculated peak current is below the saturation level of 4.71 A (see Section 5.1.4.1). It is recommended to have some margin between this calculated value and the saturation level of the core. For example, the system might still run into a problem during a peak load. This is something that has to be checked as well for the final design. The calculation

below shows the results if the assumed peak output current is 5.7 A and the PFC has been on for some time. It is assumed that the minimum voltage across buffer cap C3 is 240 V (DC).

- $a_1 = 5.3333 \times 240 \times 450 \times 10^{-6} = 576 \times 10^{-3}$
- $b_1 = -2 \times 5.70 \times 450 \times 10^{-6} \times \{5.3333 \times (19.5 + 0.05) + 240\} = -1.7661$
- $c_1 = -2 \times 5.70 \times 1.1 \times 10^{-6} \times 5.3333 \times 240 \times (19.5 + 0.05) = -313.8 \times 10^{-3}$

$$I_{pmax}\ (at\ I_O = 5.7\ A) = \frac{1.7661 + \sqrt{(-1.7661)^2 - 4 \times 576 \times 10^{-3} \times -313.8 \times 10^{-3}}}{2 \times 576 \times 10^{-3}} = 3.23\ A$$

Select the highest value of I_{pmax} (at I_O = 4.62 A and at I_O = 5.7 A) and compare this value with $I_{p(sat)}$. The highest value of I_{pmax} should preferably be lower than $I_{p(sat)}$. If so, then use the value of $I_{p(sat)}$ for I_{pmax}, because this gives more margin to the deliverable maximum output power.

5.1.4.3 Calculation of the current sense resistor R_{sense}

The next step is calculating the value for R_{sense}, see Equation 20:

$$R_{sense} = \frac{V_{sense(fb)max} - V_{sense(fb)min}}{I_{pmax} - I_{pmin}} = \frac{0.63 - 0.3}{I_{pmax} - I_{pmin}} = \frac{0.33}{I_{pmax} - I_{pmin}} \quad (20)$$

Remarks:

- $V_{sense(fb)max}$ and $V_{sense(fb)min}$: measured at dV/dt = 0 mV/µs.
- I_{pmax}: Fill in the highest I_{pmax} level (see Section 5.1.4.2).

Using the saturation current $I_{p(sat)}$ for I_{pmax} is often preferred (assuming that $I_{p(sat)} > I_{pmax}$) because it generally allows a slightly higher maximum output power for the design (it gives some extra margin). Using the highest peak current of all ($I_{p(sat)}$ = 4.715 A, see Section 5.1.2) results in a value for R_{sense} as calculated in Equation 21:

$$R_{sense} = \frac{0.33}{4.715 - 1.514} = 0.103 \approx 0.100\ \Omega \quad (21)$$

5.1.4.4 Calculation of the series resistance R16 and R17

Equation 22 calculates the series resistance of R16 and R17:

$$R_{SERIES} = \frac{I_{pmax} \times V_{sense(fb)min} - V_{sense(fb)max}}{I_{adj(FBSENSE)} \times (I_{pmax} - I_{pmin})} = \frac{I_{pmax} \times 0.3 - I_{pmin} \times 0.63}{3 \times 10^{-6} \times (I_{pmax} - I_{pmin})} \quad (22)$$

Remarks:

- $V_{sense(fb)max}$ and $V_{sense(fb)min}$: measured at dV/dt = 0 mV/µs

Example for a typical 90 W adapter:

$$R_{SERIES} = \frac{4.715 \times 0.3 - 1.514 \times 0.63}{3 \times 10^{-6} \times (4.715 - 1.514)} = 48504\ \Omega$$

The value of R17 is often a value roughly between 680 Ω and 1200 Ω. Its purpose is to prevent C10 being charged in an unwanted way because of spikes across R_{sense} that may trigger the ESD protection inside the IC. Selecting a value between these two limits allows some freedom for trimming R16 or the delay compensation resistor R16A. The value of R17 is chosen at 1000 Ω. The value of R16 then becomes: 48504 − 1000 = 47504 Ω.

5.1.5 Calculation of the delay compensation resistors R_{COMP} and R16A

R_{COMP} and R16A are intended to compensate the sum of the following three delays:

- The internal delay time of the IC
- The switch-off time of the MOSFET
- The delay time related to R17 × C23 (filter in front of the FBSENSE pin).

The transformer is still conducting current at the primary side during the sum of all these delay times. This delay can be translated into an extra current, I_{DELAY}, through the transformer (see Figure 18) and results in extra energy for the output. The amount of extra energy depends on the input voltage.

The purpose of the resistors R_{COMP} and R16A is to compensate for the unwanted current (I_{DELAY}) with the corresponding delay time. The voltage across R16A can be translated to a current I_{PRESET} with the corresponding preset time. The system is compensated if the preset values match the delay values.

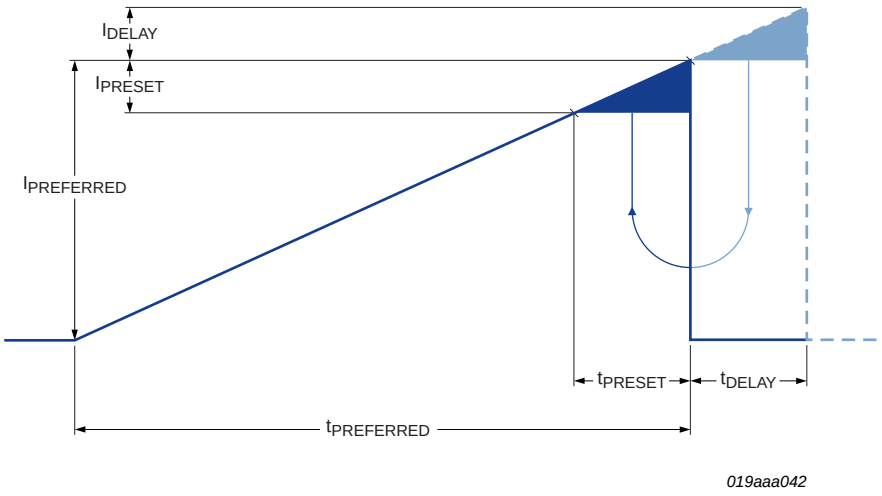


Fig 18. Principle of delay compensation

The voltage across R16A depends on the current through this resistor. This current flows via R5 and R5A. One resistor can replace both resistors. This resistor is called R_{COMP}. The value of this resistor is calculated using Equation 23 when the schematic is built according to Figure 1:

$$R_{COMP} = R5 + R5A \quad (23)$$

Example calculation for a typical 90 W adapter:

$$R_{COMP} = 2 \times (4.7\ M\Omega + 4.7\ M\Omega) = 9.4\ M\Omega = 9400\ k\Omega$$

The final delay time is determined by the internal delay time of the IC, the response time needed for switching off the MOSFET and the time-constant, R17 × C23. A minimum RC time is required in order to filter out disturbances on pin FBSENSE. An RC time selection that is too large cannot follow the ramping up input voltage properly. Therefore all other delays are first subtracted from the conducting time of the flyback MOSFET. The remaining time should be at least 5.5 times the minimum RC time required for filtering out disturbances on the FBSENSE.

A common value for the internal delay time of the IC is 220 ns. Switching of the MOSFET usually takes around 60 ns (but check this value in the final application, as the situation might be different because of the use of different MOSFETs, gate resistors, etc). The conduction time of the flyback MOSFET is shortest when the input voltage is at its highest. The highest value is usually 390 V (DC). Equation 24 shows the calculation for R17 × C23:

$$R17 \times C23\ (ns) \leq \frac{\frac{L_p \times I_{pmin}}{390 \times 10^{-9}} - t_{int.delay} - t_{MOSFET-off}}{5.5} \quad (24)$$

Example calculation for a typical 90 W adapter:

$$R17 \times C23 \leq \frac{\frac{450 \times 10^{-6} \times 1.514}{390 \times 10^{-9}} - 220 - 60}{5.5} \leq 293\ ns$$

A commonly used RC time for this filter is 220 ns at R17 = 1 kΩ and C23 = 220 pF. This value is therefore used for the following equations. The output follows the input with a delay of just one RC time after roughly five RC times. The total delay time is calculated using Equation 25:

$$t_{delay} = t_{int.delay} + t_{MOSFET-off} + R17 \times C23 \quad (25)$$

Example for a typical 90 W adapter:

$$t_{delay} = 220 \times 10^{-9} + 60 \times 10^{-9} + 1 \times 10^{3} \times 220 \times 10^{-12} = 500\ ns$$

The value of R16A is calculated using Equation 26:

$$R16A = \left(1 - \frac{R_{COMP}}{83.333 \times 10^{6}}\right) \times \left(\frac{R_{sense} \times R_{COMP} \times t_{delay}}{L_p}\right) \quad (26)$$

Example for a typical 90 W adapter:

$$R16A = \left(1 - \frac{9.4 \times 10^{6}}{83.333 \times 10^{6}}\right) \times \left(\frac{0.100 \times 9.4 \times 1 \times 10^{6} \times 500 \times 10^{-9}}{450 \times 10^{-6}}\right) = 927\ \Omega$$

5.1.6 Calculation of the flyback soft-start components

The soft-start is implemented through the RC network at pin FBSENSE.

The sum of R16, R16A and R17 must be at least 16 kΩ (*see the TEA1753T and TEA1753LT data sheets*). This ensures that the voltage $V_{start(soft)fb}$ (0.63 V) is reached and the start-up of the flyback is enabled.

In general the values of R16A and R17 are much smaller than the value of R16.

Therefore the soft-start time is: $t_{softstart} \approx 3 \times R16 \times C10$.

It is recommended to make the soft-start time for the flyback longer than the soft-start time of the PFC. It is also recommended to keep the soft-start time within the range of 5 ms to 10 ms.

The total soft-start time is approximately 8 ms when C10 = 56 nF and R16 = 49 kΩ.

5.2 Flyback control and PFC with delay options

The flyback controls the operation mode of the PFC. The PFC is turned on at an internal flyback frequency of 86 kHz and it is turned off at an internal frequency of 48 kHz (see Figure 14 and the *TEA1753T and TEA1753LT data sheets*). PFC has a relatively fast turn-on, but its turn-off is delayed via capacitor C24, which is connected to the PFCTIMER pin (see Figure 19). In this way it is possible to prevent the PFC from entering a kind of burst mode because of fast and substantial repetitive load changes at the output. Preventing this results in a more stable input voltage for the flyback. The amount of time for ignoring the shutting down signal of the PFC depends on the capacitance value connected to the PFCTIMER pin. This time is calculated using Equation 27:

$$t_{delay-PFC_{off}} \approx C24 \times 72 \times 10^{4} \quad (27)$$

Example: a capacitance value of 1.5 μF for C24 results in a delay of approximately 1.1 s. It is recommended to use a minimum value of 1 nF for C24. It is also recommended to place the 10 nF noise filter capacitor C15 as close as possible to the FBCTRL pin to guarantee a smooth transition from PFC off to PFC on and to avoid audible noise in the flyback transformer.

Note that the hysteresis between turning on and turning off the PFC is influenced by the inductance value (see Section 5.1.2). Also the valley time and other disturbances on the FBCTRL pin makes the hysteresis smaller. It is therefore advised to use the layout guidance (see Section 7) and keep the valley time short (usually a value close to 1.1 μs leads to good results).

5.2.1 Improving start-up time of the PFC

The PFC in the TEA1753 is turned on when the flyback is suddenly heavily loaded by a step load. It is in general turned on fast enough, but sometimes an even shorter start-up time is required. This is especially valid at very low line voltages in combination with large load changes. The flyback may enter the Safe restart mode when the maximum on-time protection ($t_{on(fb)max}$) is hit because of a voltage that has become too low across the bulk elcap. Selecting a larger value for the bulk elcap and/or starting up the PFC as soon as possible improves this situation. Figure 20 shows an example of how this can be done.

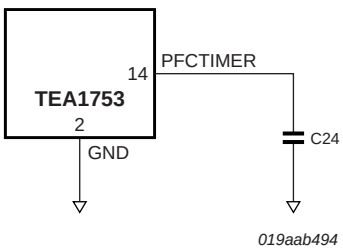


Fig 19. Standard configuration for the PFCTIMER pin

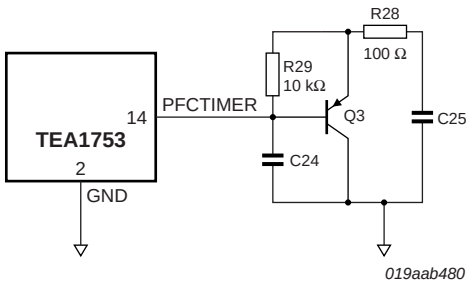


Fig 20. Improving the start-up time of the PFC

The delay time of the PFC (described in Section 5.2) is no longer determined by the value of C24 in Figure 20, but by C25. The value of capacitor C24 has to be very small, typically 1 nF. The start-up time of the PFC can be disregarded. It is recommended to use a transistor with a large DC current gain (= h_{FE}).

The start-up time of the PFC in Figure 19 is determined by Equation 28:

$$t_{delay} - PFC_{on} = 1802 \times C24 \quad (28)$$

Example:

A capacitance value of 1.5 μF for C24 results in a delay of 2.7 ms before the PFC is turned on. The ratio between the turning off and the turning on of the PFC (in Figure 19) therefore equals 400.

5.3 Flyback protection mode

5.3.1 Short circuit on pin FBCTRL

If pin FBCTRL is shorted to ground, switching of the flyback controller is inhibited. This situation equals the minimum or a no output power situation.

5.3.2 Open FBCTRL pin

As shown in Figure 21, the FBCTRL pin is connected to an internal voltage source of 3.5 V via an internal resistor of 3 kΩ. When the voltage on pin FBCTRL exceeds 2.5 V, this connection is disabled and the FBCTRL pin is biased with an internal 30 μA current source. When the voltage on the FBCTRL pin exceeds $V_{to(FBCTRL)}$ (4.5 V) a fault is assumed. Switching of the flyback (and also the PFC) is blocked and the controller enters the Safe restart mode (TEA1753T) or triggers the latched protection (TEA1753LT).

An internal switch pulls the FBCTRL pin down when the flyback is disabled.

5.3.3 Time-out flyback control loop

A time-out function can be realized to protect against an output short circuit at initial start-up or against an open control loop situation. This can be done by placing a resistor in series with a capacitor between pin FBCTRL and ground. The triggering of the time-out protection generates a safe restart for the TEA1753T and a latched protection for the TEA1753LT.

When the voltage on pin FBCTRL exceeds 2.5 V (see Figure 21) the switch in series with the resistor of 3 kΩ is opened. Pin FBCTRL and therefore the RC combination is biased with a 30 μA current source. When the voltage on pin FBCTRL exceeds 4.5 V, the switching of the flyback (and also of the PFC) is blocked and the controller enters the Safe restart mode (TEA1753T) or is latched (TEA1753LT). The capacitor can be used to set the time for reaching 4.5 V at the FBCTRL pin. The resistor is necessary to separate the relatively large time-out capacitor from the control loop response. It is advised to use a resistor of at least 30 kΩ. This resistor also influences the charge time of the capacitor.

The time-out time t_{to} is calculated using Equation 29:

$$t_{to} = \frac{C_{to} \cdot V_{to(FBCTRL)} - (I_{O(FBCTRL)} \cdot R_{to})}{I_{O(FBCTRL)}} \quad (29)$$

The capacitor is calculated using Equation 30:

$$C_{to} = \frac{I_{O(FBCTRL)} \cdot t_{to}}{V_{to(FBCTRL)} - (I_{O(FBCTRL)} \cdot R_{to})} \quad (30)$$

The resistor is calculated using Equation 31:

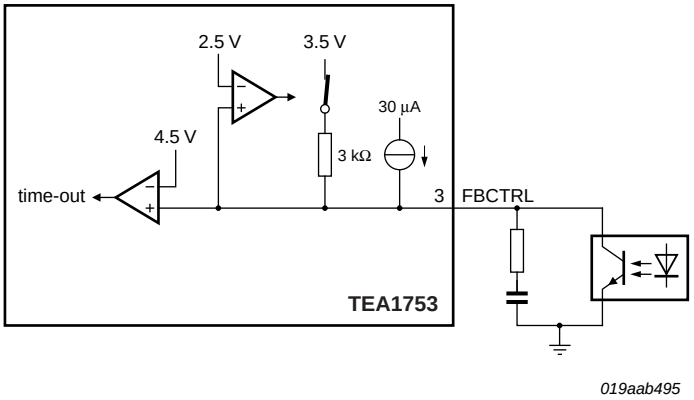
$$R_{to} = \frac{V_{to(FBCTRL)}}{I_{O(FBCTRL)}} - \frac{t_{to}}{C_{to}} \quad (31)$$

Example based on the following assumptions:

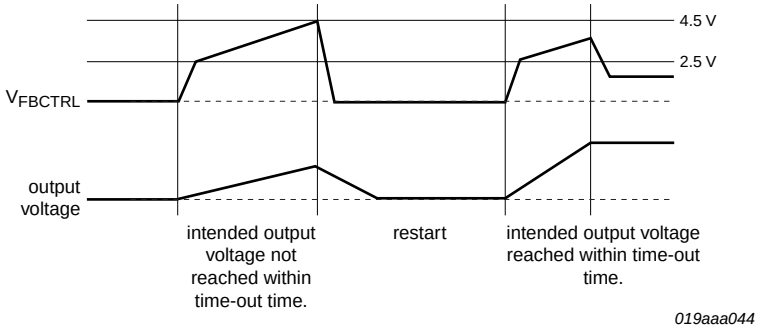
- t_{to} = 37 ms
- C_{to} = 330 nF

$$R_{to} = \frac{4.5\ V}{30\ \mu A} - \frac{37\ ms}{330\ nF} = 37.9\ k\Omega \approx 39\ k\Omega$$

If time-out protection is not required, it is disabled by placing a resistor of 100 kΩ between pin FBCTRL and ground.



a. Circuit diagram



b. Timing diagram

Fig 21. Time-out protection

5.3.4 Overvoltage protection flyback

The IC has an internal latched overvoltage protection circuit, which switches off both controllers when an overvoltage is detected at the output of the flyback. The IC can detect an overvoltage at a secondary winding of the flyback by measuring the voltage at the auxiliary winding during the secondary stroke. A series resistor between the auxiliary winding and the FBAUX pin converts this voltage to a current through the FBAUX pin.

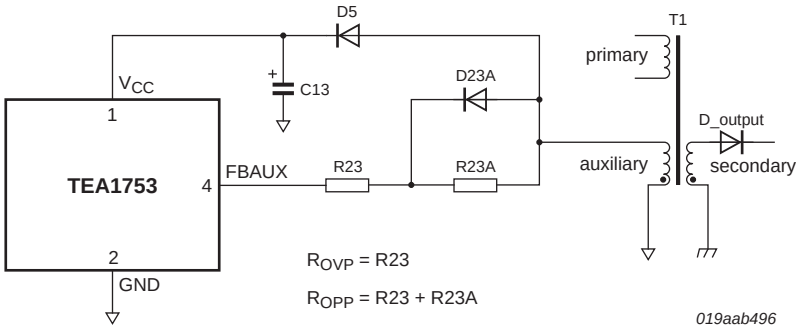


Fig 22. Flyback OVP and OPP circuit

At a current, $I_{ovp(FBAUX)}$, of 300 μA into the FBAUX pin, the IC detects an overvoltage. An internal integrator filters noise and voltage spikes. The output of the integrator is used as an input for an up-down counter. The counter has been added as an extra filter to prevent false OVP detection, which might occur during ESD or lightning events.

If the integrator detects an overvoltage, the counter increases its value by 1. If another overvoltage is detected during the next switching cycle, the counter increases its value by 1 again. If no overvoltage is detected during the next switching cycle, the counter subtracts its value by 2 (the minimum value is 0). If the value reaches 8, the IC assumes a true overvoltage and activates the latched protection. Both converters are switched off immediately and V_{CC} starts cycling between $V_{th(UVLO)}$ and $V_{startup}$ without a restart.

Switching off and then switching on the mains input voltage triggers the fast latch reset circuit and resets the latch.

The OVP level can be set by the resistor R_{ovp}:

$$R_{ovp} = \frac{\left(\frac{N_{aux}}{N_s} \times V_{ovp(VOSENSE)}\right) - V_{clamp(FBAUX)} - V_{f(D23A)}}{I_{ovp(FBAUX)}} = \frac{\left(\frac{N_{aux}}{N_s} \times V_{ovp(VOSENSE)}\right) - 0.7\ (typical) - V_{f(D23A)}}{300\ \mu A\ (typical)} \quad (32)$$

Where:

- N_s is the number of turns on the secondary winding.
- N_{aux} is the number of turns on the auxiliary winding of the flyback transformer.
- $V_{clamp(FBAUX)}$ is the positive clamp voltage of the FBAUX pin.
- $V_{f(D23A)}$ is the forward voltage of D23A at a current of 300 μA.

The tolerances on $I_{ovp(FBAUX)}$ have to taken into account for the calculation of the $V_{ovp(VOSENSE)}$ level to avoid triggering of the OVP during normal operation.

5.3.5 OverPower Protection (OPP)

The maximum output power in a flyback in Quasi-resonance mode depends on the (mains) input voltage. An OPP is implemented to compensate for this. During the primary stroke of the flyback the mains voltage is sensed by measuring the current drawn from pin FBAUX. With a resistor between the flyback auxiliary winding and pin FBAUX the voltage at the auxiliary winding is converted to a current I_{FBAUX} (see Figure 22). The IC uses the current information to reduce the setting of the maximum flyback peak current measured through pin FBSENSE. See Figure 23 for the limitation of the maximum $V_{FBSENSE}$ level as a function of I_{FBAUX}.

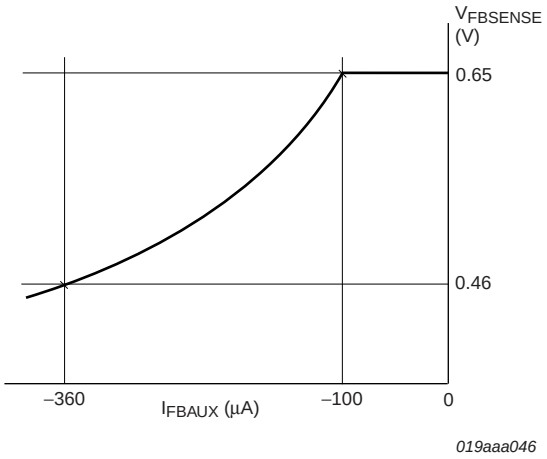


Fig 23. OPP maximum FBSENSE voltage

The total OPP resistance determining the I_{FBAUX} current during the primary stroke of the flyback exists of R23 + R23A (see Figure 22). The OVP resistor R23 has to be calculated before the remaining part of the OPP resistor R23A can be calculated.

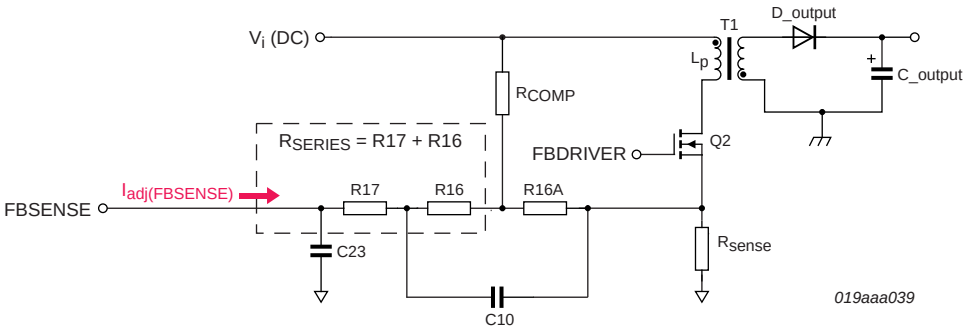
The value of R23A is calculated using Equation 33:

$$R23A = \frac{\frac{N_{aux}}{N_p} \cdot V_{O(PFC)low} - V_{clamp(FBAUX)}}{I_{start(OPP)FBAUX}} - R_{OVP} = \frac{\frac{N_{aux}}{N_p} \cdot 240\ V - 0.8\ V}{100\ \mu A} - R_{OVP} \quad (33)$$

The sum of R23 and R23A should be lower than 666 kΩ.

6. Summary of calculations for adjustment of the flyback

See Figure 1 application schematic for component reference numbers.

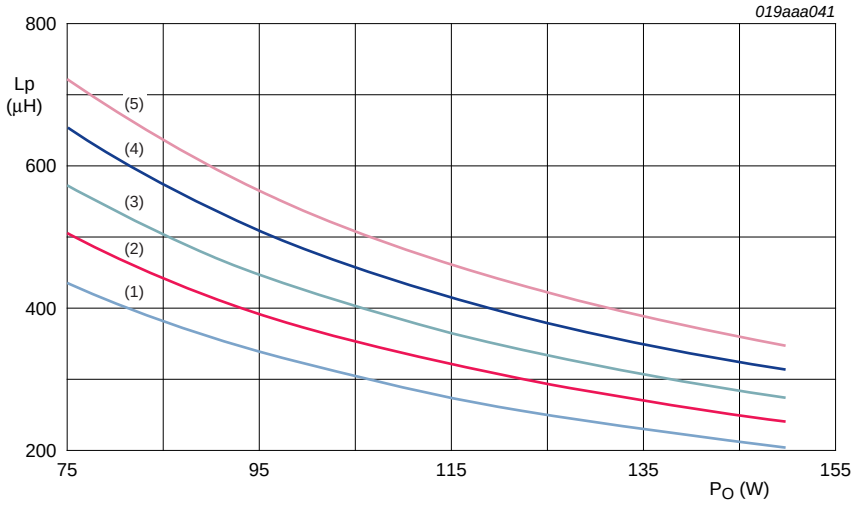


FBSENSE has two internal reference levels:

(1) $V_{start(soft)fb}$ = 0.630 V at dV/dt = 0 mV/µs

(2) $V_{sense(fb)min}$ = 0.300 V at dV/dt 0 mV/µs

a. Most important components for adjusting the flyback in the application



$L_p = f(P_O)$

Assumptions: Minimum voltage across buffercap (C3) is approximately 100 V (DC) at 50 % of the nominal output power.

(1) $N \times (V_O + V_f)$ = 80 V

(2) $N \times (V_O + V_f)$ = 92 V

(3) $N \times (V_O + V_f)$ = 104 V

(4) $N \times (V_O + V_f)$ = 118 V

(5) $N \times (V_O + V_f)$ = 130 V

b. Indication of the maximum inductance value, related to output power and $N \times (V_O + V_f)$

Fig 24. Most important components and maximum inductance value for adjusting the flyback in the application

Step 1: Use the graph in Figure 24 to determine an indication for the maximum primary inductance value or use Equation 34:

$$L_p = \left(\frac{N \times (V_O + V_f)}{104.3}\right) \times 43061 \times 10^{-6} \times (I_{O(nom)} \times (V_O + V_f))^{-1.0005} \quad (34)$$

Step 2: Select a transformer and calculate the saturation current:

$$I_{p(sat)} = \frac{N_p \times B_{max} \times A_e}{L_p} \quad (35)$$

Step 3: Calculate the required peak current through the flyback transformer. Calculate this value during nominal output current in combination with the minimum electrolytic buffer capacitor voltage and at peak output current when the PFC is operating. Only the highest value of these two needs to be taken into account. Name this value I_{pmax}.

Common rule is that $I_{p(sat)} > I_{pmax}$. Selecting the higher $I_{p(sat)}$ value for I_{pmax} prevents saturation of the transformer and allows a power margin. Therefore in general the calculation is continued with $I_{pmax} = I_{p(sat)}$.

$$I_{pmax} = \frac{-b + \sqrt{(b^2 - 4 \times a \times c)}}{2 \times a} \quad (36)$$

Where:

- $a = N \times V_{i(DC)min} \times L_p$
- $b = -2 \times I_O \times L_p \times \{N \times (V_O + V_f) + V_{i(DC)min}\}$
- $c = -2 \times I_O \times t_{valley} \times N \times V_{i(DC)min} \times (V_O + V_f)$

Step 4: Calculate I_{pmin} (related to the turning on or the turning off of the PFC):

$$I_{pmin} = \sqrt{\frac{2 \times 0.375 \times I_{O(nom)} \times (V_O + V_f)}{L_p \times 67000 \times \eta_{fb}}} \quad (37)$$

η_{fb} stands for the efficiency of the flyback. Use relatively high values, e.g. close to 0.97…0.98.

Step 5: Calculating the value of R_{sense}:

$$R_{sense} = \frac{0.33}{I_{pmax} - I_{pmin}} \quad (38)$$

Step 6: Calculating the value of R_{SERIES}:

$$R_{SERIES} = \frac{I_{pmax} \times 0.3 - I_{pmin} \times 0.63}{3 \times 10^{-6} \times (I_{pmax} - I_{pmin})} \quad (39)$$

Note that the R_{SERIES} comprises two components, R16 and R17. The common value for R17 is between 820 Ω and 1200 Ω. A typical value that is used often is 1000 Ω.

Step 7: Checking/calculating the time constant R17 × C23:

$$R17 \times C23\ (ns) \leq \frac{\frac{L_p \times I_{pmin}}{390 \times 10^{-9}} - t_{int.delay} - t_{MOSFET-off}}{5.5} \quad (40)$$

Where:

- $t_{int.delay}$ = 220 ns
- $t_{MOSFET-off} \cong$ 60 ns (Note that the value can be different in other applications)

In general the calculation often shows that R17 × C23 ≥ 220 ns. If this is so then 220 ns should be sufficient for R17 × C23. A slightly smaller value might be acceptable but is not preferred (has to be checked on the application board).

Step 8: Calculate the delay time:

$$t_{delay} = t_{int.delay} + t_{MOSFET-off} + R17 \times C23 \quad (41)$$

Remark: The commonly used value for R17 × C23 is 220 ns (see also step 7).

Step 9: Calculating the compensating resistor R_{COMP}:

$$R_{COMP} = R5 + R5A \quad (42)$$

Calculating the value of R_{16A}:

$$R16A = \left(1 - \frac{R_{COMP}}{83.333 \times 10^{6}}\right) \times \left(\frac{R_{sense} \times R_{COMP} \times t_{delay}}{L_p}\right) \quad (43)$$

7. PCB layout considerations

A good layout is considered to be an important part of the final design. It minimizes all kinds of disturbances and makes the overall performance more robust with less risk of EMI. Guidelines for the improvement of the layout of the print-circuit board are given below:

- Separate large signal grounds from small signal grounds (see Figure 25). Small signal grounds can be easily recognized by their triangle shaped symbol. All other ground symbols are related to large signal grounds
- Try to make the print area that fits within the separate large signal loops (see Figure 25) as small as possible. Each separate large signal loop has its own color. Make the copper tracks as wide and short as possible
- The connection between both MOSFETs (PFC and flyback) and both driver outputs of the IC should be as short as possible (green line in Figure 25). Try to minimize the coupling between these two signals by increasing the distance between them and/or preferably using a guided ground track for both connections
- The power ground and small signal ground are only connected with one short copper track (make this track as short and as wide as possible). Preferably it should become one spot (connection between ground 4a and ground 6a, shown as a green line in Figure 25)
- Use a ground shield underneath the IC, connect this ground shield to pin 2 of the IC
- All resistors connected in series to an IC pin should be connected as close as possible to that pin
- Any heatsink connected to a component must be connected to that component's nearest corresponding ground signal. Make this connection as short as possible. Connect the heatsink of diode bridge BD1 to ground 1, Q1 to 4 and Q2 to 4b. In typical applications all three components are often mounted on one single heatsink. If this is indeed the case, just make one wide copper track that connects all three grounds mentioned above to each other. Also combine in this copper track ground 2
- Connect the grounds of 6b to each other
- Make a so-called "star ground" from ground 6a, 6b, 6c, and 7. Ground 6a is the middle of the star and is connected to pin 2 (this is the ground of the IC)
- Grounds marked 7 do not have to be a so-called "star ground”
- Place the y-cap across grounds 1 and 8. Preferably use one special copper track, separated from all others for this connection (or use the connection copper track of the heatsinks in a typical application setup for this purpose)
- C4, C15, C23 and C22 (in order of priority) should be placed as close as possible to the IC. Reduce coupling between the PFC switching signals (PFC driver and PFCAUX) and the flyback sense signals (FBSENSE and FBCTRL) as much as possible, because this minimizes the risk of electromagnetic interference and audible noise
- Figure 25 shows an overview of the hierarchy of the different grounds at the bottom
- Connect the anode of the TL431 (ground 8) to ground 9 using one special separate connecting copper track. Minimize all other currents in this special track. The actual place of connection should preferably be located as close as possible to the output
- Place the TEA1791 close to the power MOSFET Q4

- Connect the ground of the TEA1791 directly to a wide and short copper track to the source of Q4
- Connect the series resistor R32 directly between the drain of Q4 and pin 1 of the IC. Use a separate copper track for this purpose
- The connection between MOSFET Q4 and driver pin of the TEA1791 should be as short as possible (green line in Figure 25). Preferably, use a guided ground track
- Make the connection between R50 and SWDET of the TEA1703 as short as possible and place the resistor close to the IC

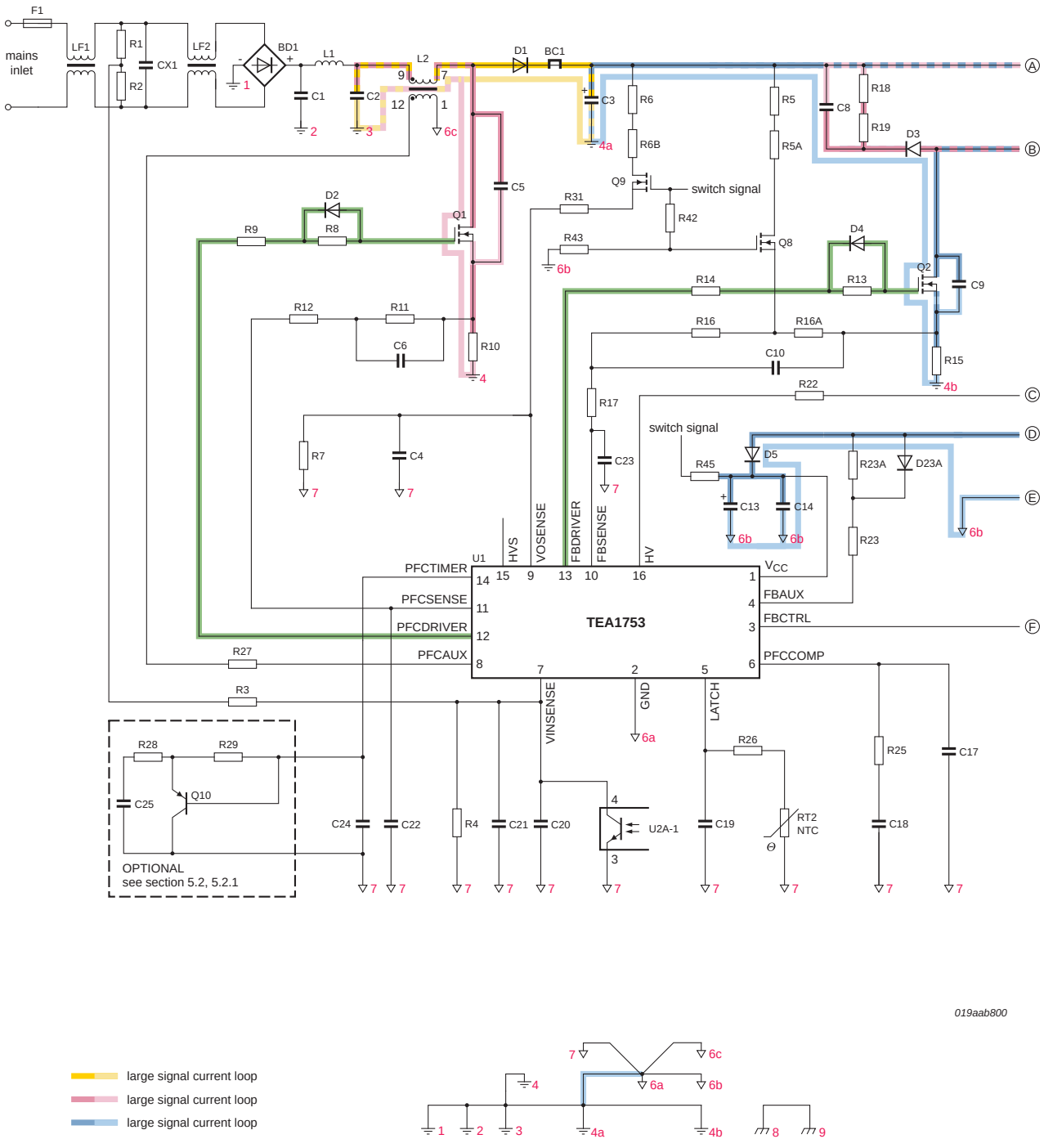


Fig 25. PCB layout considerations (part 1)

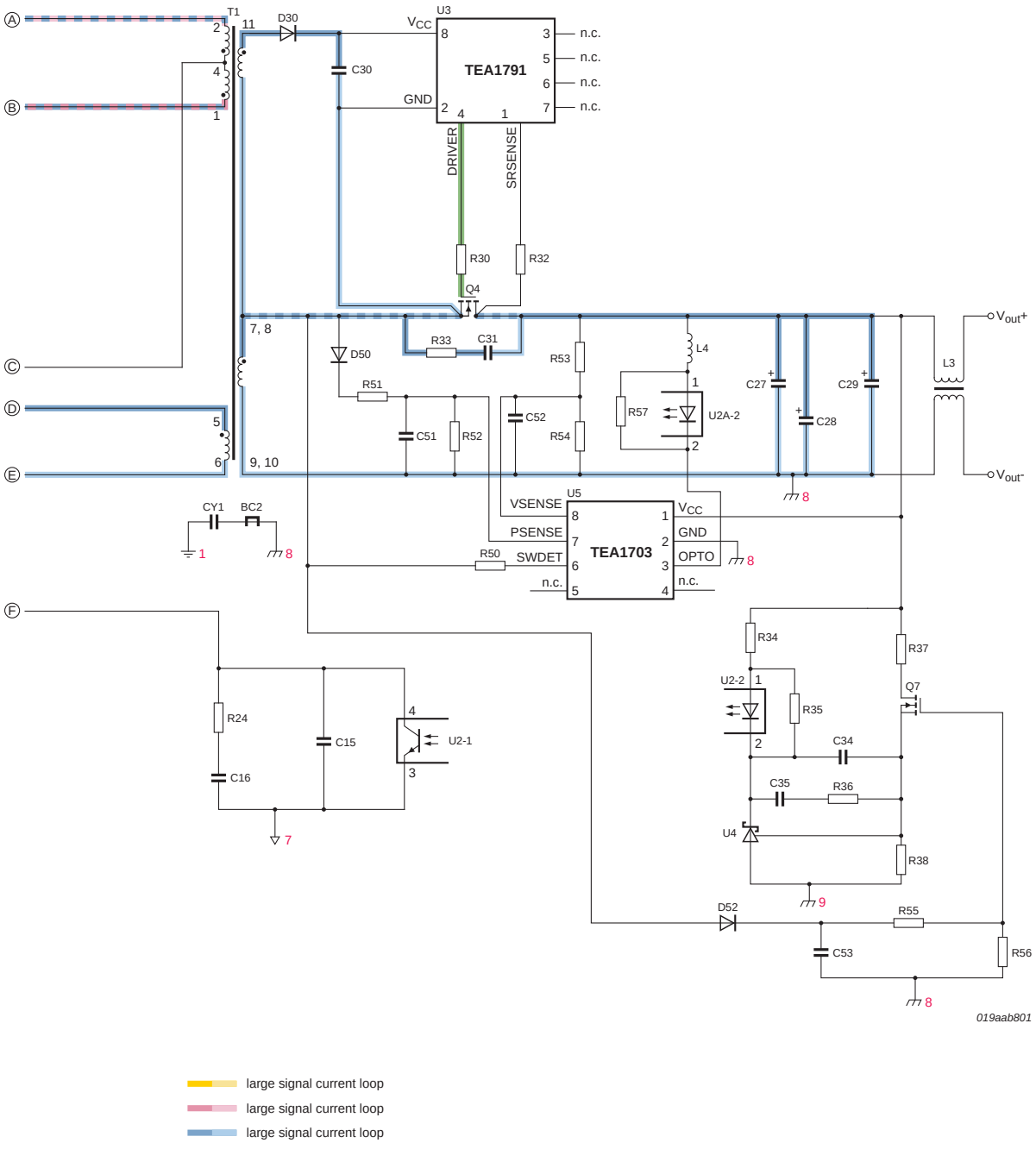


Fig 26. PCB layout considerations (part 2)

8. References

[1] IEC-60950 — Chapter 2.1.1.7 “discharge of capacitors in equipment”

9. Legal information

9.1 Definitions

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10. Contents

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