AN11022

CLRC663 evaluation board quick start guide

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Document information

Information	Content
Keywords	CLRC663, CLRC663 plus, CLEV6630A, CLEV6630B, CLRC663 evaluation board, CLRC663 customer board, CLRC663 GUI, GUI, CLRC663 Support Tool, NFC Cockpit
Abstract	This document describes the CLEV6630A and CLEV6630B (CLRC663 evaluation board), and how to use it. It describes the NFC Cockpit (Version 3.6), which allows an easy basic access to the CLRC663 registers and EEPROM in combination with basic reader functionality.

1 Introduction

This document describes the CLEV6630A and CLEV6630B (CLRC663 evaluation board), which provides an easy evaluation of the features and functions of the CLRC663 and CLRC663 *plus* families.

It provides the first steps to operate the board, using the NFC Cockpit (Version 3.6 or higher).

The default antenna is a 65 mm x 65 mm antenna with some metal layer inside the antenna area. This antenna is not an optimum antenna as such, but intends to demonstrate the performance and register settings of the CLRC663 under typical design constraints like LCD or some metal (e.g. PCB) inside the antenna area (see [2] for more information).

In this document the term "MIFARE Classic card" refers to a MIFARE Classic IC-based contactless card, the term "MIFARE DESFire card“ refers to a MIFARE DESFire IC-based contactless card.

1.1 CLRC663 registers and EEPROM concept

The CLRC663 uses internal registers to adapt and optimize the functionality and performance for each of the supported protocols and data rates dependent on the connected antenna, matching network and receiver path. It offers an EEPROM, which contains the default settings for all the supported protocols (locked). These settings are loaded into the registers with the LoadProtocol command for each supported protocol and data rate.

The default EEPROM configuration settings are optimized for the generic use, based on the 65mmx65mm antenna of the board CLEV6630A / CLEV6630B, and cannot be updated by the user as such. Individual settings must be overwritten by the host µC after the LoadProtocol.

Alternatively, customized settings can be used for the major relevant registers in an extra EEPROM area. Then the command LoadReg must be used to copy the customized EEPROM content into the registers.

Some of these settings can or even **must** be adapted toward a new antenna design (e.g. the RX settings). See [3].

Some EEPROM configuration data is independent from the used protocols and defines e.g. the startup behavior of the CLRC663 or the functionality of LowPower Card detection and requires attention as well for optimum performance of the chip.

1.2 CLEV6630A / CLEV6630B concept

The basic **concept of the CLEV6630A** / **CLEV6630B** is to enable the user to perform a quick evaluation of the CLRC663, and also connect their own antenna to the CLRC663 board. In addition, dedicated boards which allow to solder custom matching components are available. The NFC Cockpit can be used to optimize the CLRC663 antenna tuning, to perform the related TX and RX optimization without touching any source code.

All the relevant CLRC663 registers can be modified and fine-tuned using the NFC Cockpit. For the most relevant registers, the customized settings can typically be stored in the CLRC663 EEPROM.

The NFC Cockpit also allows a dump of the complete user EEPROM content into an XML file. This file then can be loaded again into the EEPROM. That allows to manage and exchange different user or antenna configurations. In addition, the register settings found to work well using the NFC Cockpit, can be used during user code development as well.

As soon as the register settings for the targeted protocols and data rates are defined, the NFC Reader Library including the HAL can be used to start the development of the user application (see [6]). Examples illustrate the usage of the library for typical use cases.

The source code examples of the NFC Reader Library can be used to develop an own application directly on the LPC1769 (see Figure 3), or can serve as a starting point for porting the NFC Library to any other microcontroller platform.

2 Hardware

The CLEV6630, as shown in Figure 1 and Figure 2, provides many test functions which might not be used for the typical hardware and software evaluation. It can be used as a simple standard reader without modification, it can be used to define and optimize the analog settings for any connected antenna or it can be used to develop and modify any RFID and NFC application based on the NFC Reader Library.

The CLEV6630A and CLEV6630B share the same hardware, except these differences:

1. CLEV6630A uses the CLRC66302, while CLEV6630B uses the CLRC66303.
2. The CLEV6630A PCB color is red, while the CLEV6630B is blue.
3. The antenna tuning is slightly different (see 2.2.3).

2.1 Hardware introduction

The CLRC663 is supplied with a supply voltage, which can be chosen between: internal and external supply. For the internal supply either 5 V or 3.3 V can be used. The external power supply can be an AC or DC supply (polarity does not matter) with at least 7.5 V, since the board provides a rectifier and LDO to supply the circuit with 5 V and 3.3 V.

The CLRC663 is connected to an NXP LPC1769 µC via SPI. A specific firmware on the LPC1769 allows to use the CLEV6630A / CLEV6630B together with the NFC Cockpit.

The connection to the PC is done via USB: USB micro connectors are supported. The use of the shielded USB cable is required to meet the FCC/CE specifications.

Another connection option allows to connect an LPC-LINK2 board to the CLEV6630A / CLEV6630B with a debug cable. This allows the development of custom software or the execution of the NFC Reader Library code including samples.

In case a different host microcontroller shall be used, the SPI interface is available for connection to an external host (the on board LPC1769 is not used in this case).

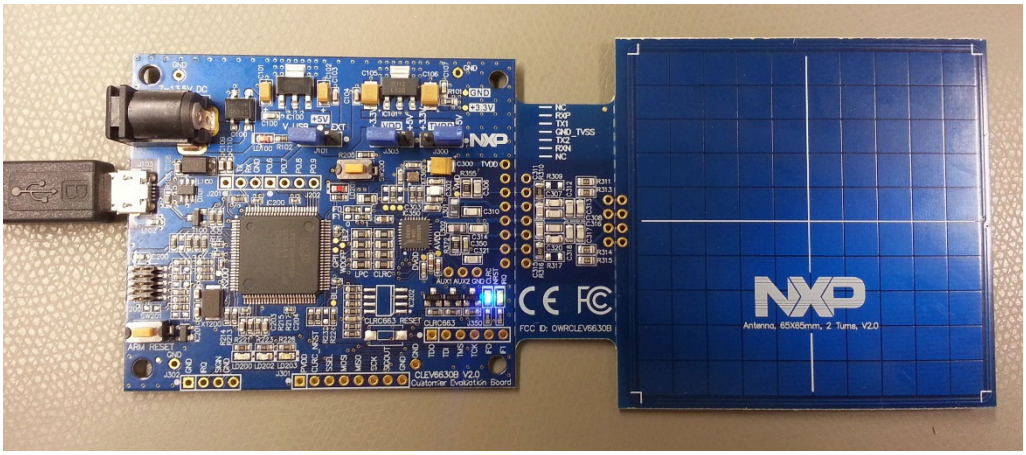


Figure 1. CLEV6630B Customer evaluation board

Note: The CLEV6630A looks identical, but with a red PCB.

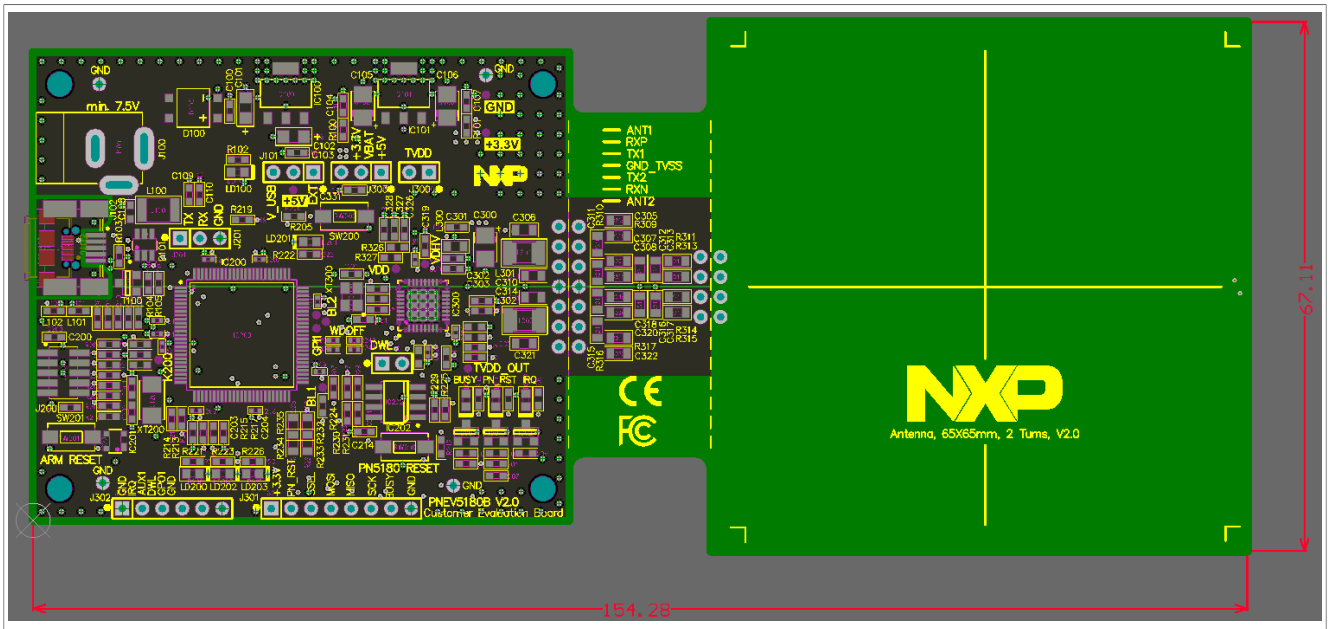


Figure 2. CLEV6630B top view

2.2 Schematics

The complete schematics of the CLRC663 evaluation board are shown in Figure 3, Figure 4, Figure 5 Figure 6, Figure 8, and Figure 9.

2.2.1 LPC1769

The CLEV6630A / CLEV6630B contains an NXP LPC1769 (see Figure 3).

An LPC Linker can be connected to the LPC1769 via the JTAG interface (see Figure 4 and Figure 5).

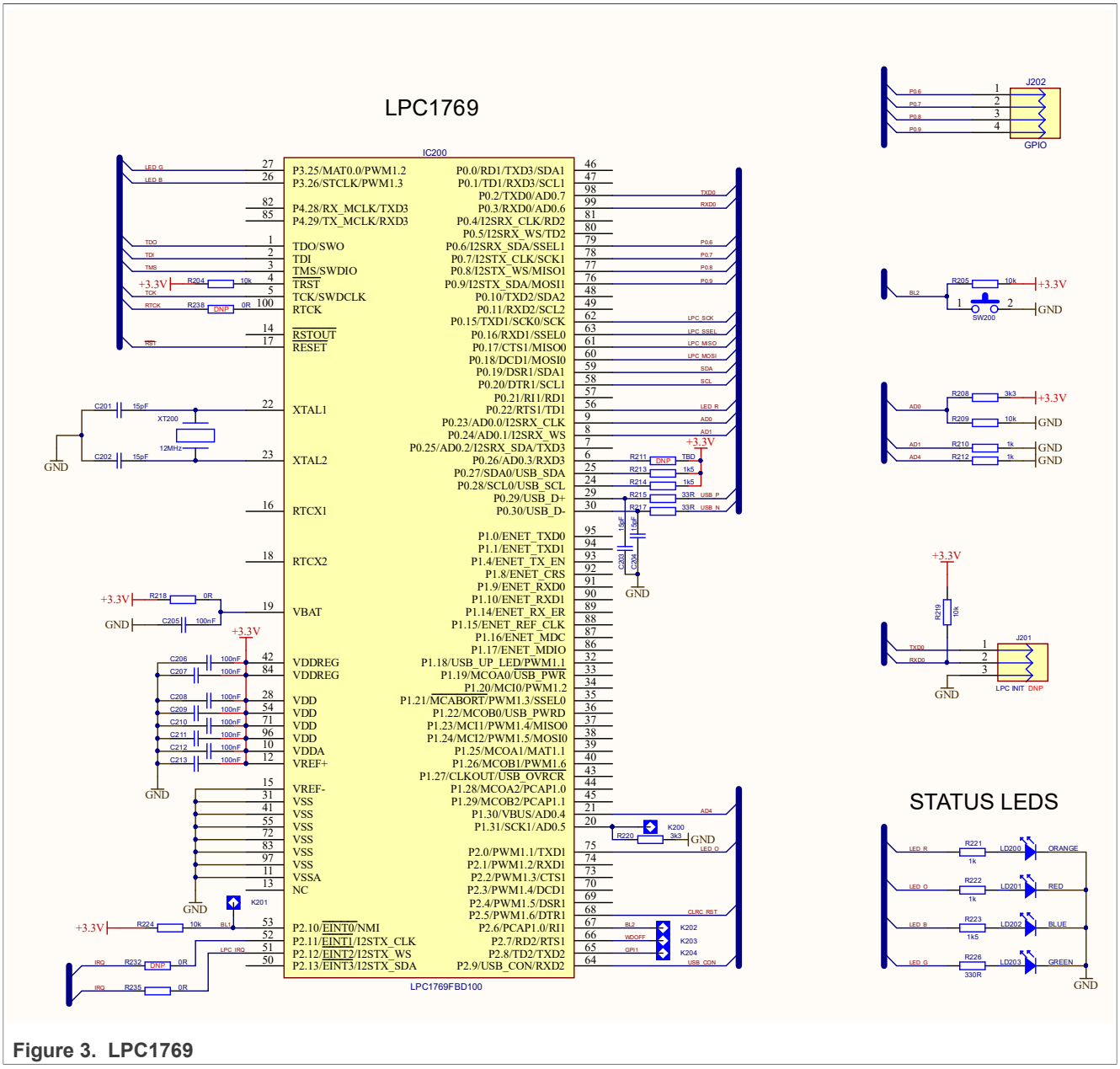


Figure 3. LPC1769

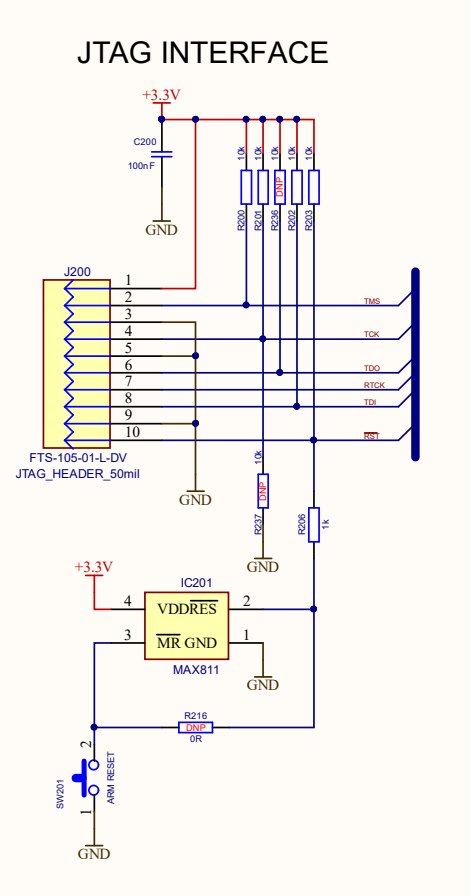


Figure 4. JTAG interface

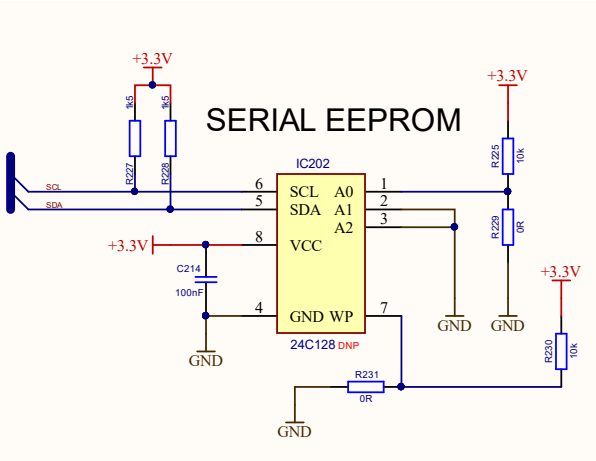


Figure 5. Serial EEPROM not assembled

2.2.2 Power supply

The default settings use the power supply from the USB connector. For the maximum performance and a better test capability, the external power supply should be connected. The AC or DC power input can cover any power supply providing an AC or DC voltage between 7.5 and 12 V.

Figure 6 shows the USB supply, external supply and LPC1769 supply.

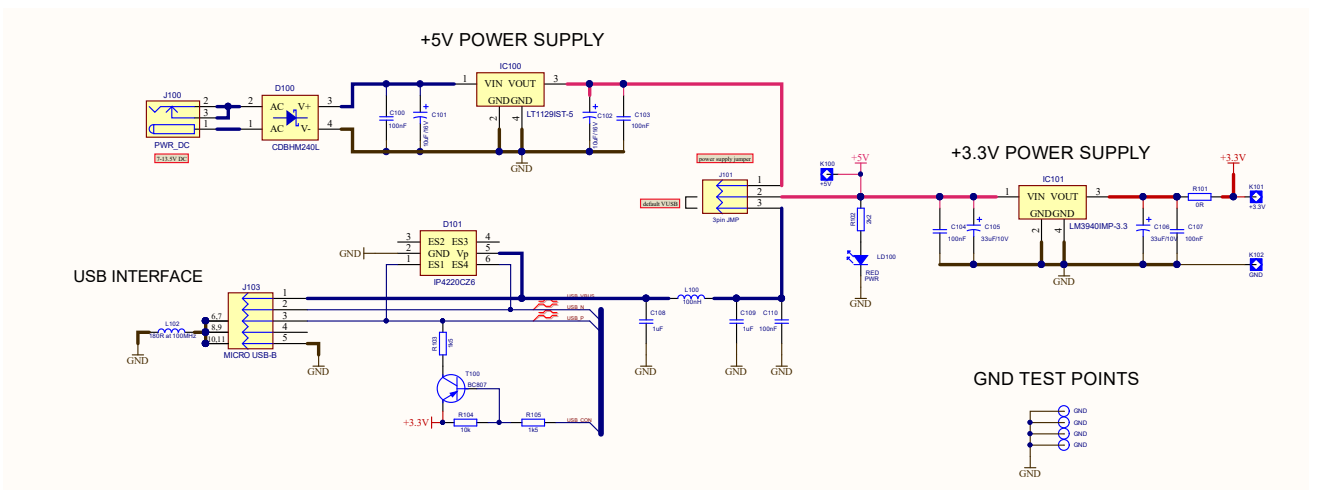


Figure 6. Power supply

As soon as the board is supplied with power, the red LED LD100 must be on.

The CLRC663 evaluation board provides two LDOs, one for 5 V and one for 3.3 V. 5 V LDO can only be used, if the external power supply is connected and used (J101 default). Using USB power might not give the best RF performance, since the USB voltage level might not be stable 5 V.

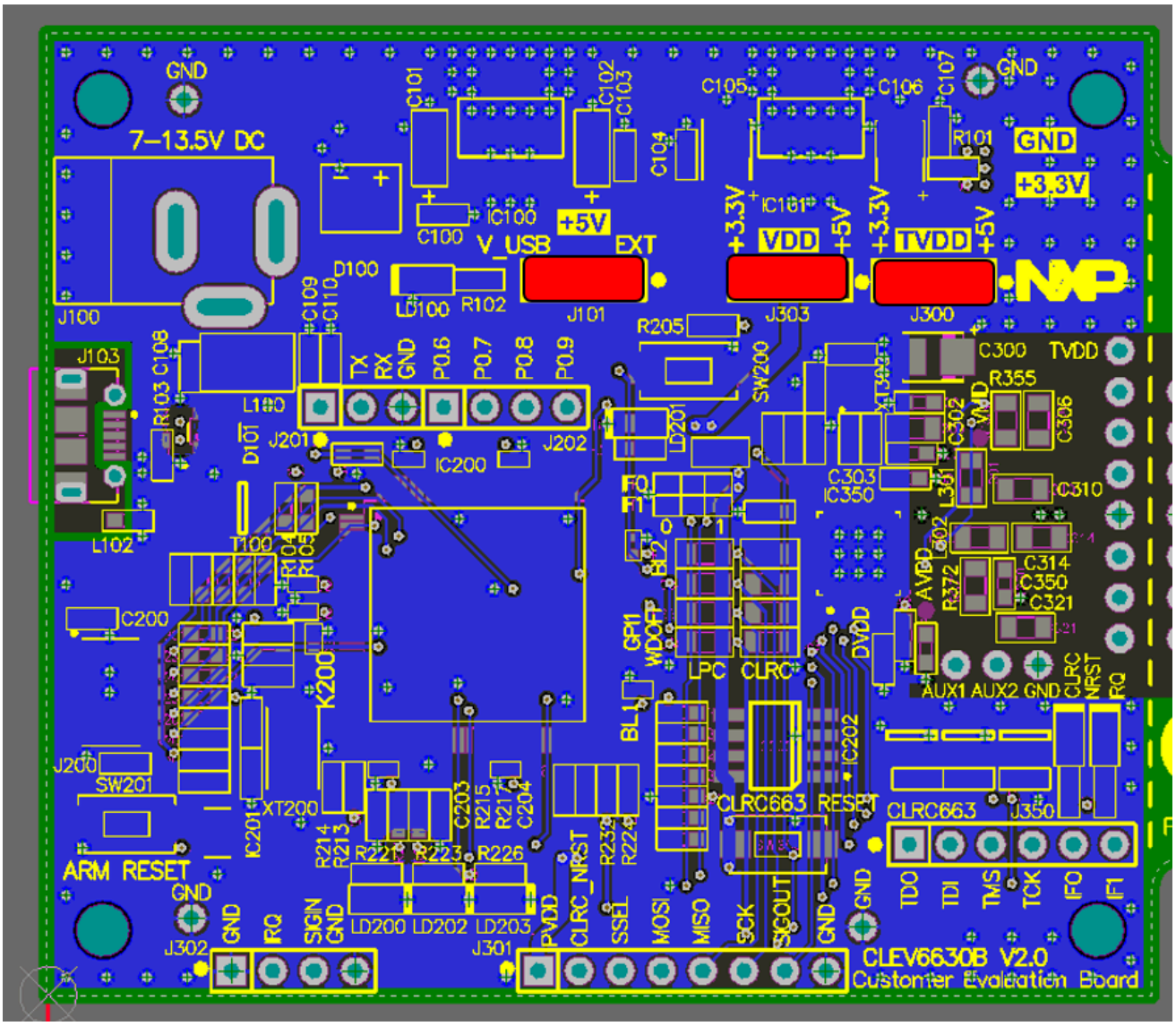


Figure 7. CLEV6630A / CLEV6630B jumpers

Three jumpers can be used to evaluate the different power supply options:

- J101: either external or USB power supply (default)
- J303: either VBAT = 5 V or 3.3 V (default)
- J300: closed (default) or to measure the ITVDD (bridge with an ampere meter) or to supply the CLRC663 (center pin of J300) with external TVDD from an external DC power supply

Note: *The best RF performance can be achieved with an external power supply.*

2.2.3 CLRC663

The clock is based on a 27.12 MHz crystal.

During the antenna tuning and overall hardware design typically the ITVDD must be checked. This can be done with the JP300 (“TVDD”), either using an external power supply or just using an ampere meter instead of the jumper.

The relevant test signals can be derived from the digital test pins at the bottom of the board and the two analog test pins AUX1 and AUX2.

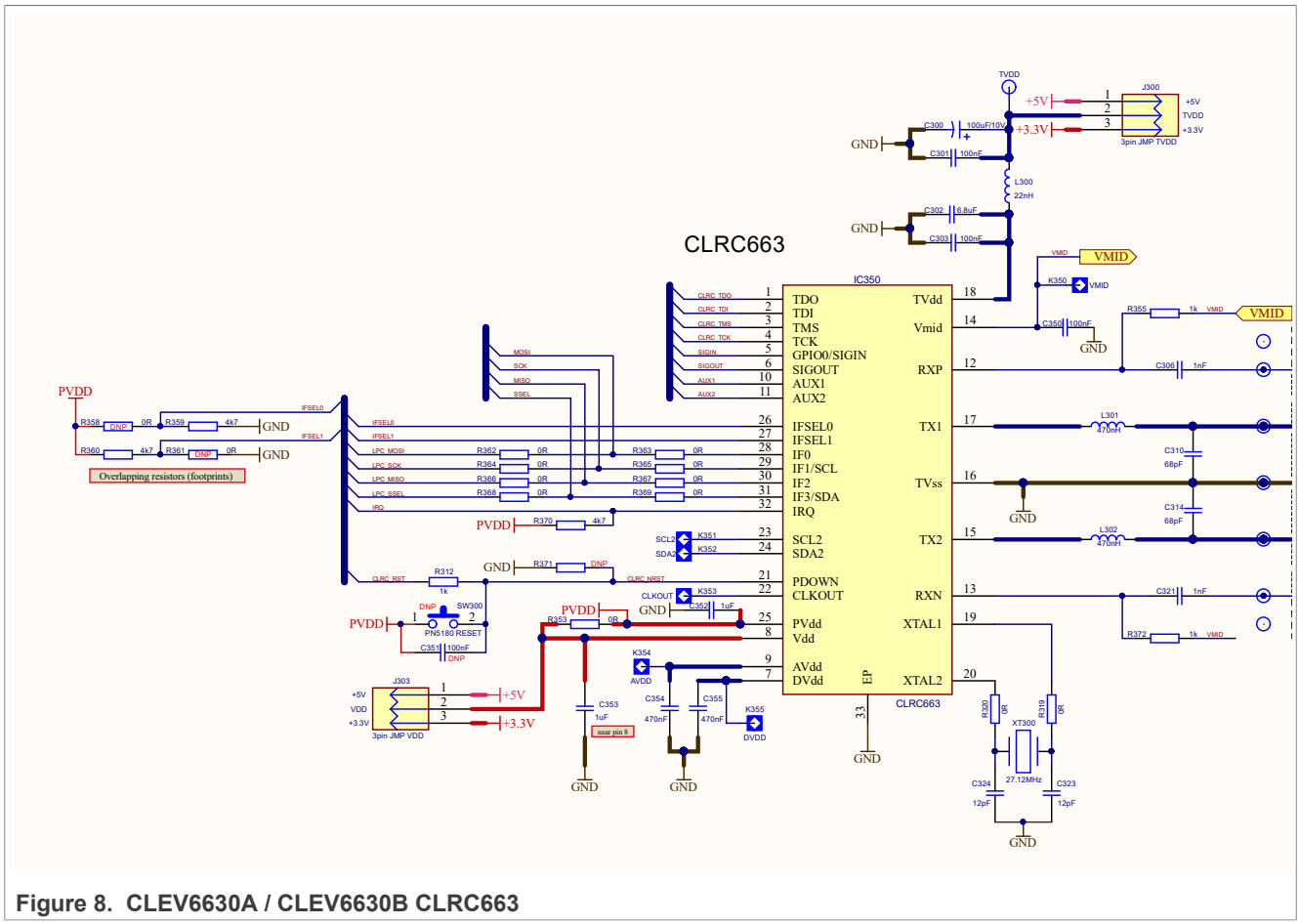


Figure 8. CLEV6630A / CLEV6630B CLRC663

The antenna connection uses the standard tuning circuit. The EMC filter is designed with a cut-off frequency of $f_{EMC} \approx 21$ MHz, and the antenna impedance is tuned to $Z \approx 20\ \Omega$.

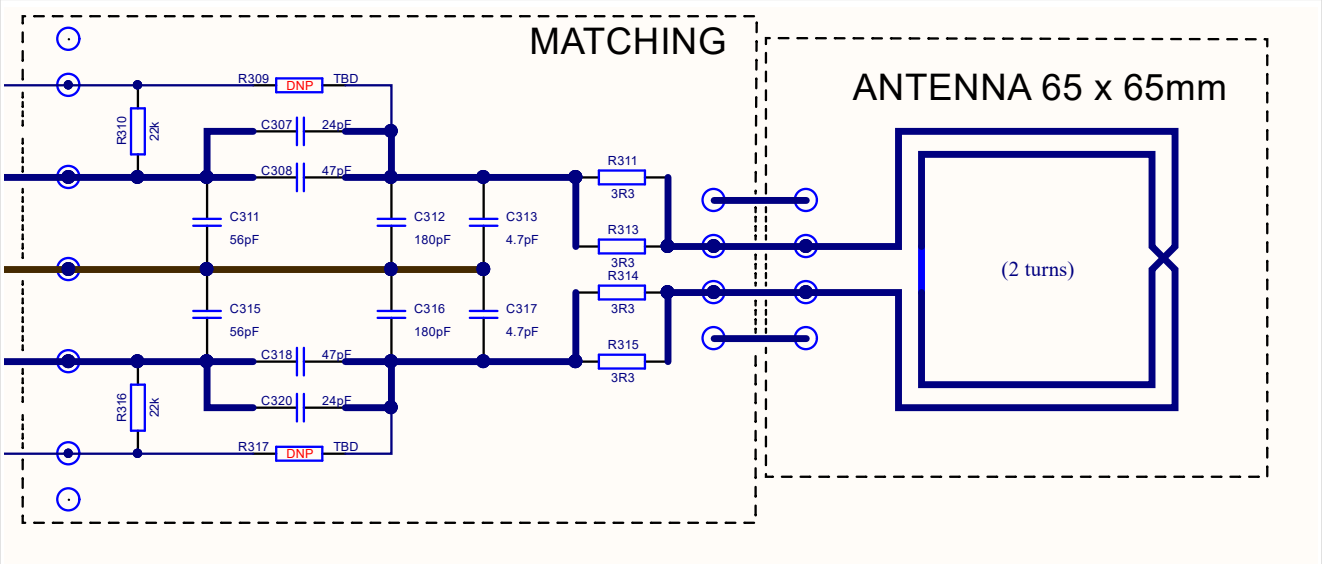


Figure 9. CLEV6630B antenna circuit

The “asymmetrical” tuning (see Figure 10) is a compromise to provide optimum power transfer and good wave shapes in combination with good loading effects, which automatically reduce the field strength under strong loading conditions.

The CLEV6630A antenna tuning is the same as the tuning of the CLEV6630B, except these differences:

1. C307 = C320 = 12 pF
2. C316 = C317 = 33 pF

Note: *The CLRC663 plus (CLEV6630B) can drive more output power than the CLRC663 (CLEV6630A), so the antenna for the CLRC663 plus could be tuned with a lower impedance to increase the field strength. However, the maximum allowed field strength must be taken into account, too.*

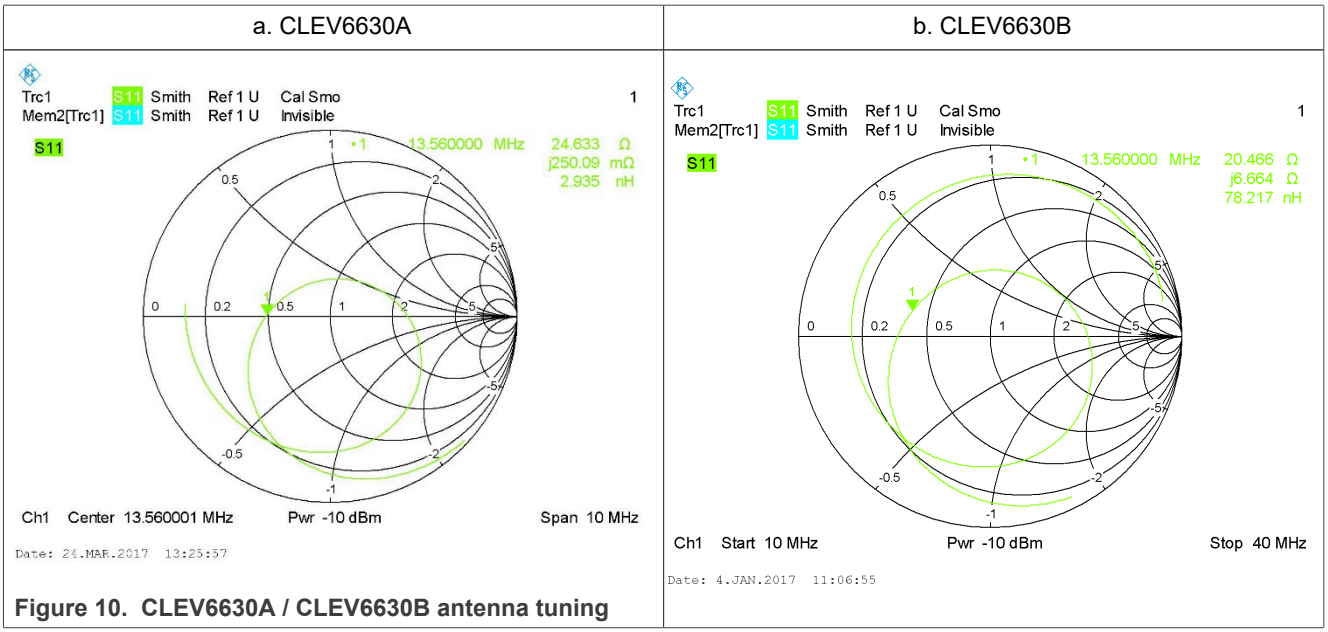


Figure 10. CLEV6630A / CLEV6630B antenna tuning

2.3 Jumper settings

Three jumpers can be used to evaluate the different power supply options:

J101: either external or USB power supply (default)

J303: either VBAT = 5 V or 3.3 V (default)

J300: closed (default) or to measure the ITVDD

Figure 11 shows the default jumper settings for operation powered via USB.

Figure 12 shows the jumper setting for the operation externally powered.

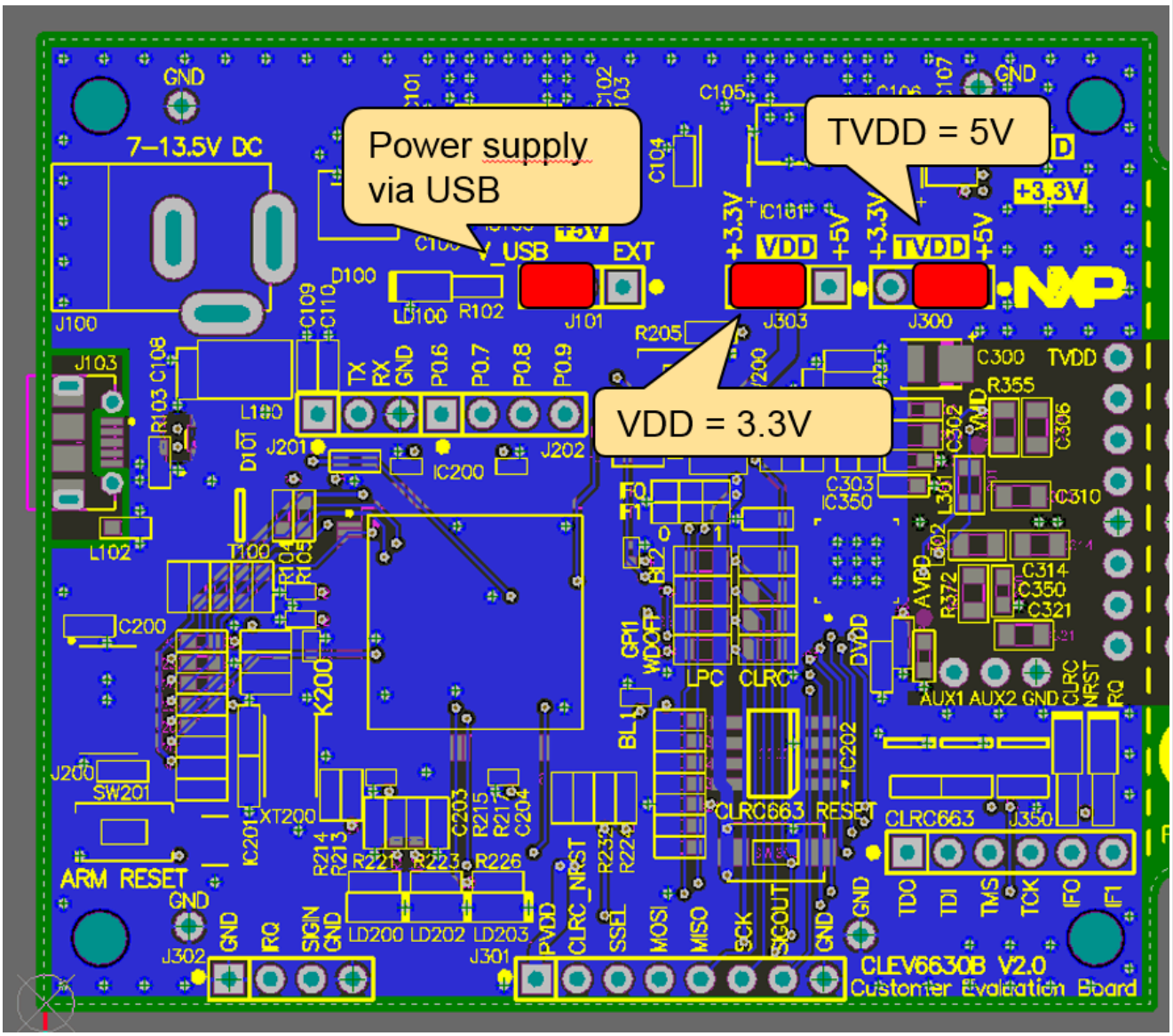


Figure 11. CLEV6630A / CLEV6630B default jumper settings

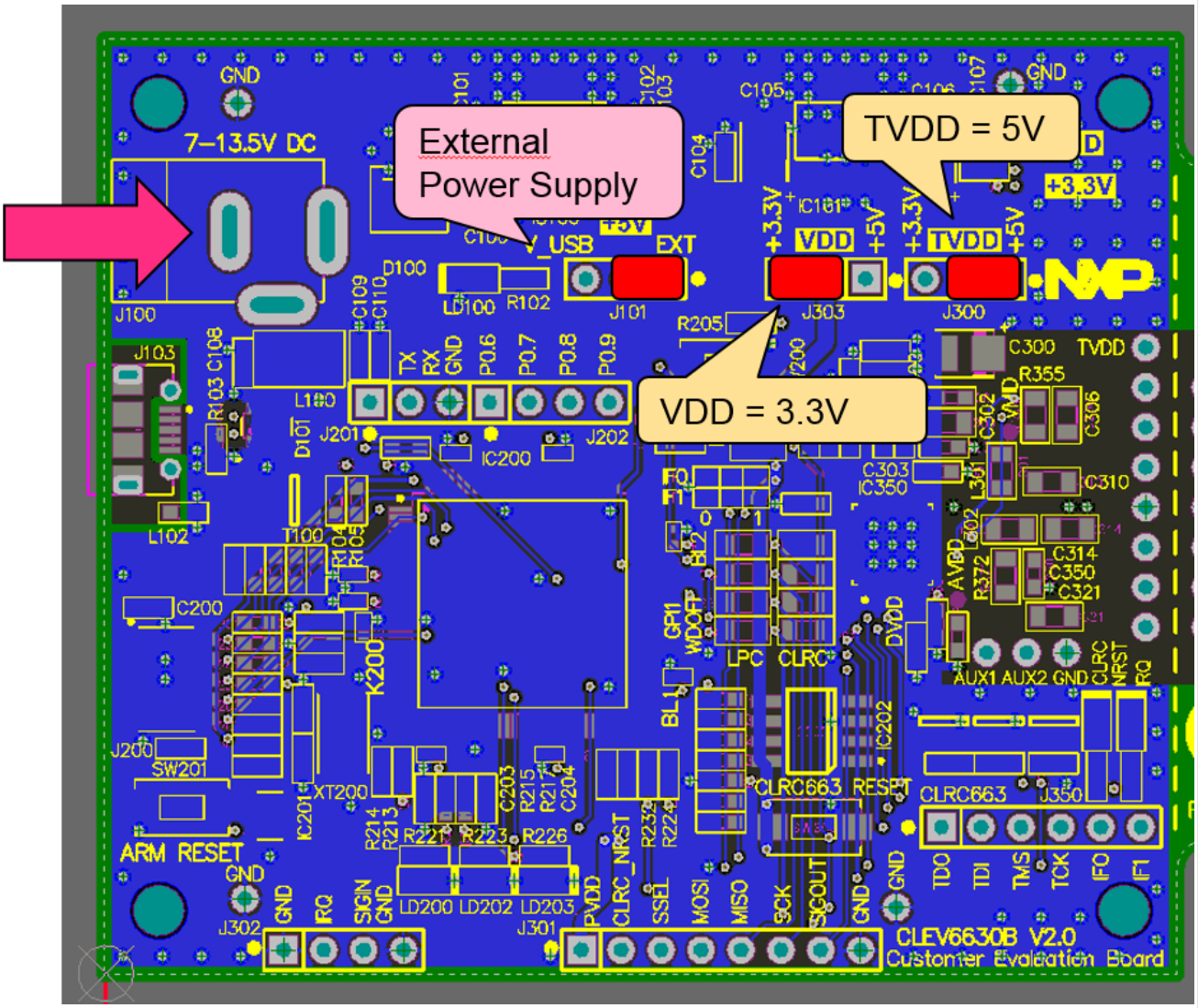


Figure 12. CLEV6630A / CLEV6630B jumper settings for external power supply

3 Software

The CLEV6630A / CLEV6630B evaluation board is delivered with a graphical user interface application (GUI), the NFC Cockpit. The NFC Cockpit can be used to explore the functionality of the CLRC663 and perform RF and antenna design-related tests. It allows a direct register access as well as EEPROM read and write access. The NFC Cockpit can therefore be used to configure and test the CLRC663.

3.1 LPC firmware and driver

The LPC firmware is installed by default on the CLEV6630A / CLEV6630B and is ready to use. No LPC firmware installation is required, if the board is only used with the NFC Cockpit.

However, the LPC1769 might be used for software development together with one of the NXP software examples (including the NFC Reader Library). In such case the LPC FW must be reinstalled afterwards, if the CLEV6630A / CLEV6630B is supposed to be used together with the NFC Cockpit again. The reason for this is that any software development using the LPCXpresso erases the default firmware. The use and reinstallation of the LPC firmware using the LPCXpresso is described in [5].

In any case the correct PC VCOM driver must be installed, before the NFC Cockpit can be used with the CLEV6630A / CLEV6630B evaluation board. This driver needs to be manually installed, using the “install_vcom.bat” in the subdirectory NFC Cockpit _v xyz \VCOM.

For the first start with the CLEV6630A / CLEV6630B, refer to section 4.

3.1.1 LPC firmware installation

For installation of LPC firmware, the LPC link and a LPCXpresso tool is required. For details refer to [5].

3.1.2 LPC driver installation

Before the first connection of the CLEV6630A / CLEV6630B (with LPC firmware) to the PC, the driver must be installed with

\Name of the GUI package\VCOM\install_vcom.bat

After successful installation of the driver, the CLEV6630A / CLEV6630B can be connected to the PC and will show up as VCOM device on a COM port, as shown in Figure 13.

Note for possible future NFC Cockpit updates: Make sure to use the latest driver version, otherwise the application might not work correctly. In case of doubt, reinstall the driver of the corresponding NFC Cockpit package.

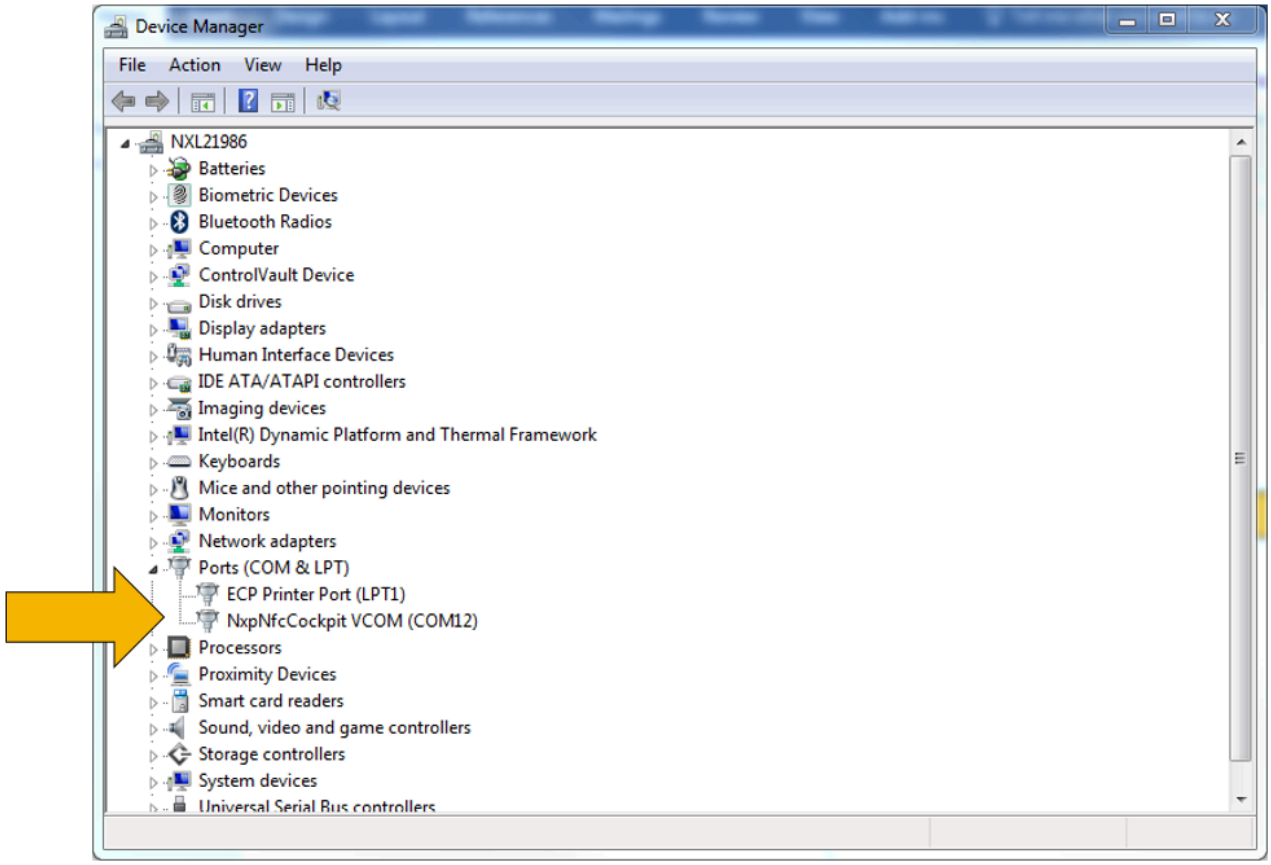


Figure 13. NFC Cockpit VCOM driver

CLEV6630A / CLEV6630B connected to the PC, driver properly installed.

3.2 NFC Cockpit

The NFC Cockpit can be installed and started (see Figure 14).

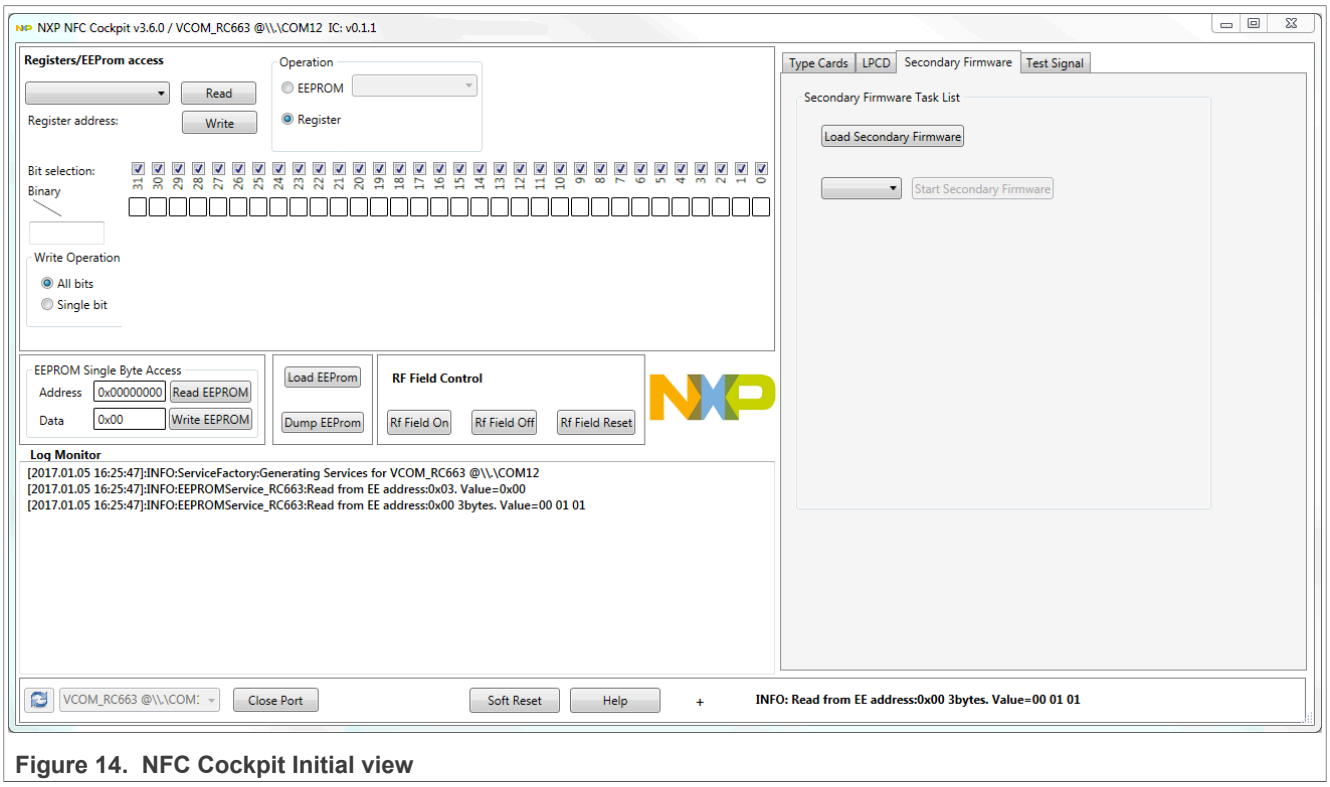


Figure 14. NFC Cockpit Initial view

After starting the NFC Cockpit, the communication link between the PC and the CLEV6630A / CLEV6630B (via the LPC VCOM interface) is enabled automatically.

Note: The NFC Cockpit is a development tool, and therefore allows many different kinds of operations, even “useless” ones at a first glance. The correct use of the NFC Cockpit is required to operate the CLRC663 properly.

Example: without enabling the RF Field no card can be operated, even though the CLRC663 can be operated.

The Figure 15 shows the activation of a MIFARE DESFire card, using the <Load Protocol> + <Field On> + <Activate Layer3>, followed by <Activate Layer4>. The NFC Cockpit shows the card responses like ATQA, SAK, and ATS.

Afterwards the ISO/IEC 14443-4 protocol can be used to exchange data. The Figure 15 shows the MIFARE DESFire command “Get Application ID” (0x6A), which returns the AIDs.

Note: Make sure that either the CRC is enabled or added manually in the data field.

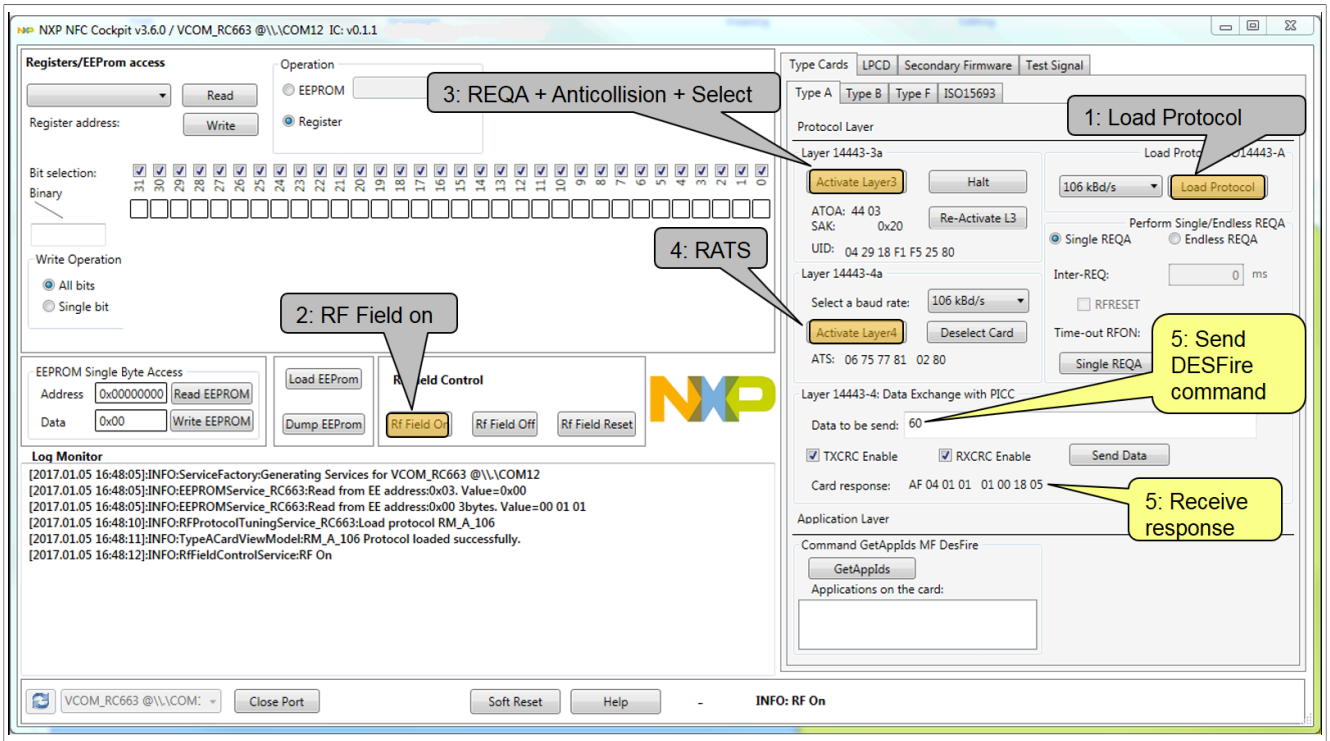


Figure 15. NFC Cockpit: Activation of a MIFARE DESFire EV1 card

Note: 0x60 = Get Version command of MIFARE DESFire EV1.

Similar functionality does exist for ISO/IEC 14443 A and B, for NFC type F and for ISO/IEC 15693 communication.

Be aware that a Load Protocol command must be executed manually before the corresponding protocol settings are loaded from the EEPROM into the registers. The tab “Type A” can be used to perform:

1. <Load Protocol> (e.g. type A 106)
2. <Field On>
3. <Single REQA> (using the EEPROM settings)
4. Select a TX register, e.g. DRVMODREG, change TXCLOCKMODE
5. Change some register bits, and write back into RAM
6. <Single REQA> shows the register changes (probing the field and checking the envelop)

This allows an easy and quick optimization of TX and RX parameters. Using the default settings from the EEPROM always resets the relevant registers.

1. <Load Protocol> (e.g. type A 106)
2. <Single REQA> (using again the EEPROM settings)

Note: *The EEPROM of the CLRC663 is locked for all the LoadProtocol area.*

3.2.1 CLRC663 register access

The NFC Cockpit allows the reading and writing of all the CLRC663 registers (see Figure 16).

Selecting a register reads and shows the hexadecimal content as well as the corresponding bit values. The input allows to change each bit separately as well as writing hexadecimal values. Writing back the value changes the CLRC663 register.

A help function automatically shows a short description of the (part of the) registers itself, if the mouse is moved over the names.

Note: Some register content cannot be changed manually (“read only”) and some content might be overwritten by the LPC firmware.

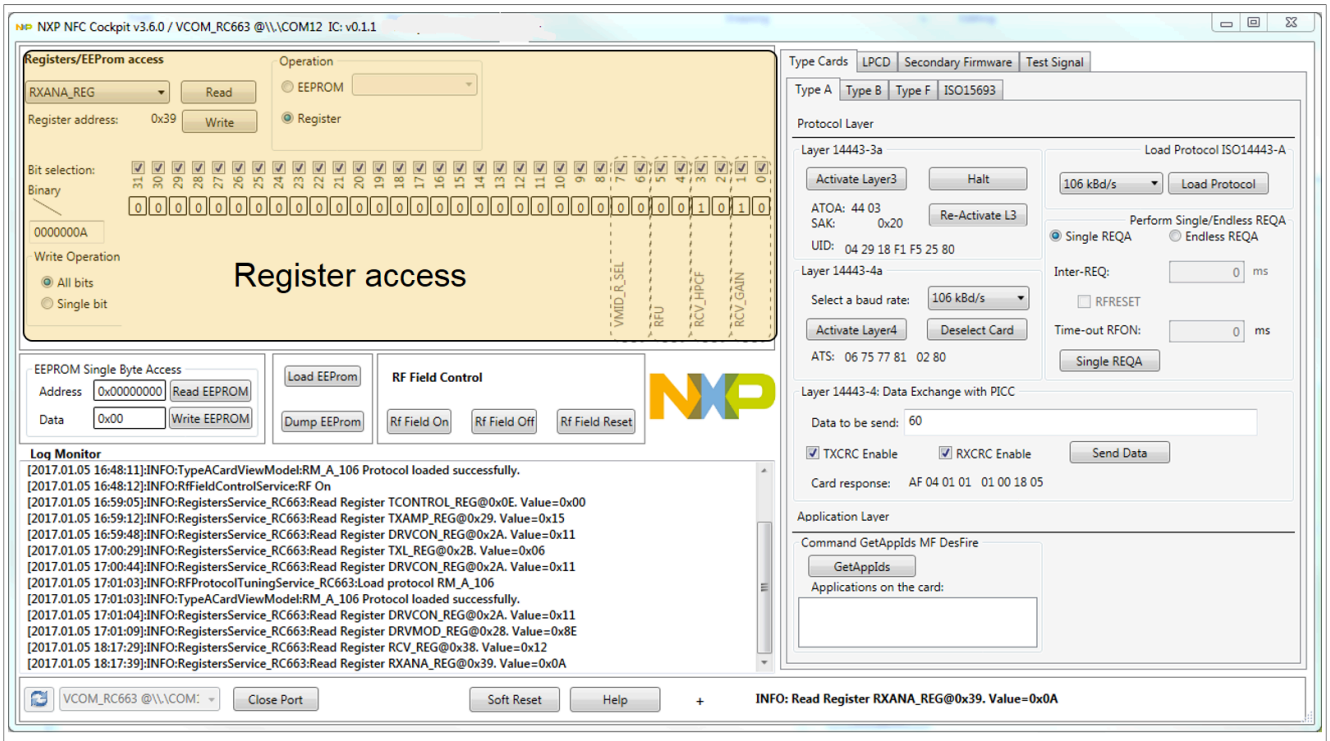


Figure 16. CLRC663 register access

Registers are temporary stored, i.e. might be overwritten with Load Protocol.

3.2.2 CLRC663 analog and digital test signals

The NFC Cockpit allows to route the CLRC663 digital test signals to the SIGOUT pin, as well as to unlock and route the CLRC663 analog test signals to test pins AUX1 and AUX2. This is shown in Figure 17.

The digital test pin SIGOUT can be found at the J301 (pin row). While the analog signals are routed to two test pads as close to the CLRC663 as possible (below the antenna tuning area).

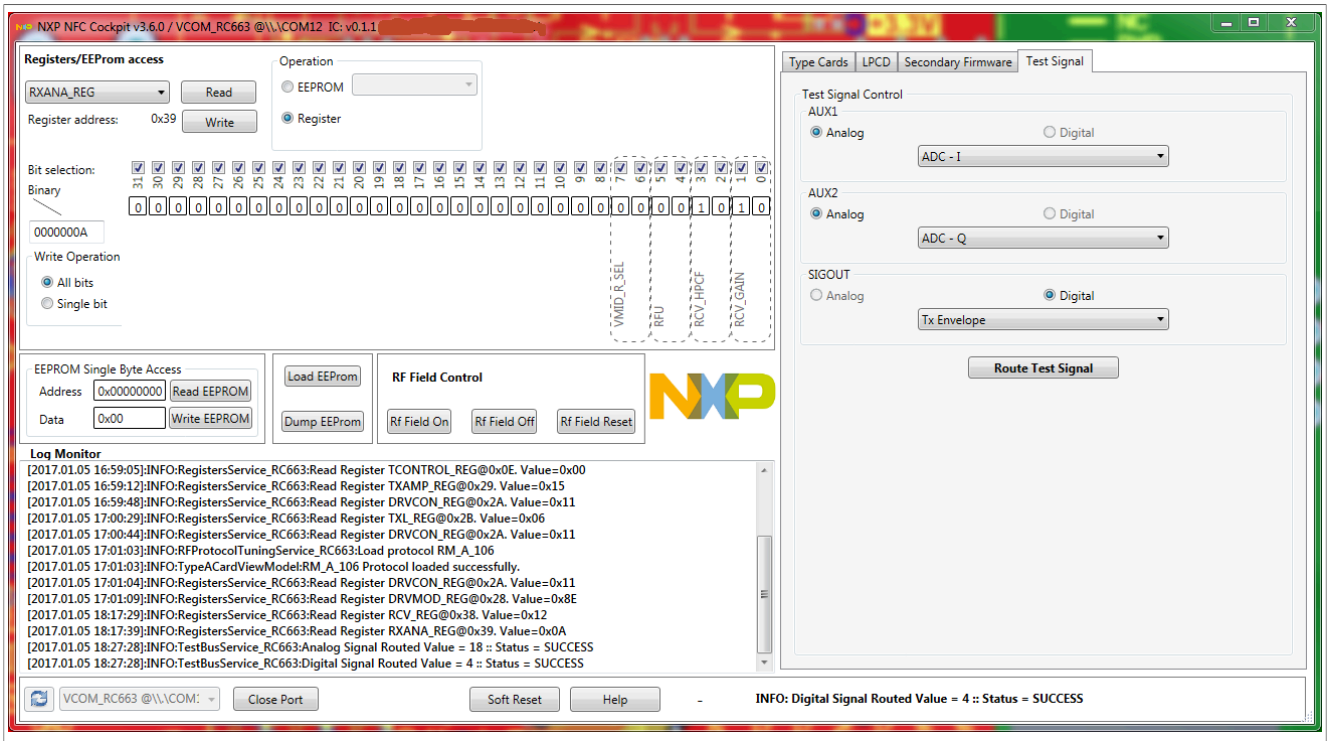


Figure 17. CLRC663 analog and digital test signals

After selecting the signals <Route Test Signal> activates the chosen test signals at the chosen test pins.

3.2.3 CLRC663 low-power card detection

The NFC Cockpit allows the configuration and test of the low-power card detection (LPCD) of the CLRC663 as shown in Figure 18. The offered LPCD functionality depends on the detected board: The CLEV6630A offers the CLRC66302 features, while the CLEV6630B offers the enhanced LPCD features of the CLRC66303 (CLRC663 *plus*).

The LPCD parameter, which is used to define the LPCD performance (sensitivity versus robustness) can be entered manually, if needed (details refer to [4]).

Otherwise the standby time can be entered and the LPCD can be started. During the LPCD being activated the CLRC663 does not react on any command, so only a detuning (-> place a card) or a Reset (press <Stop LPCD>) can end the LPCD mode.

Note: The NFC Cockpit automatically stops the LPCD after 60 seconds.

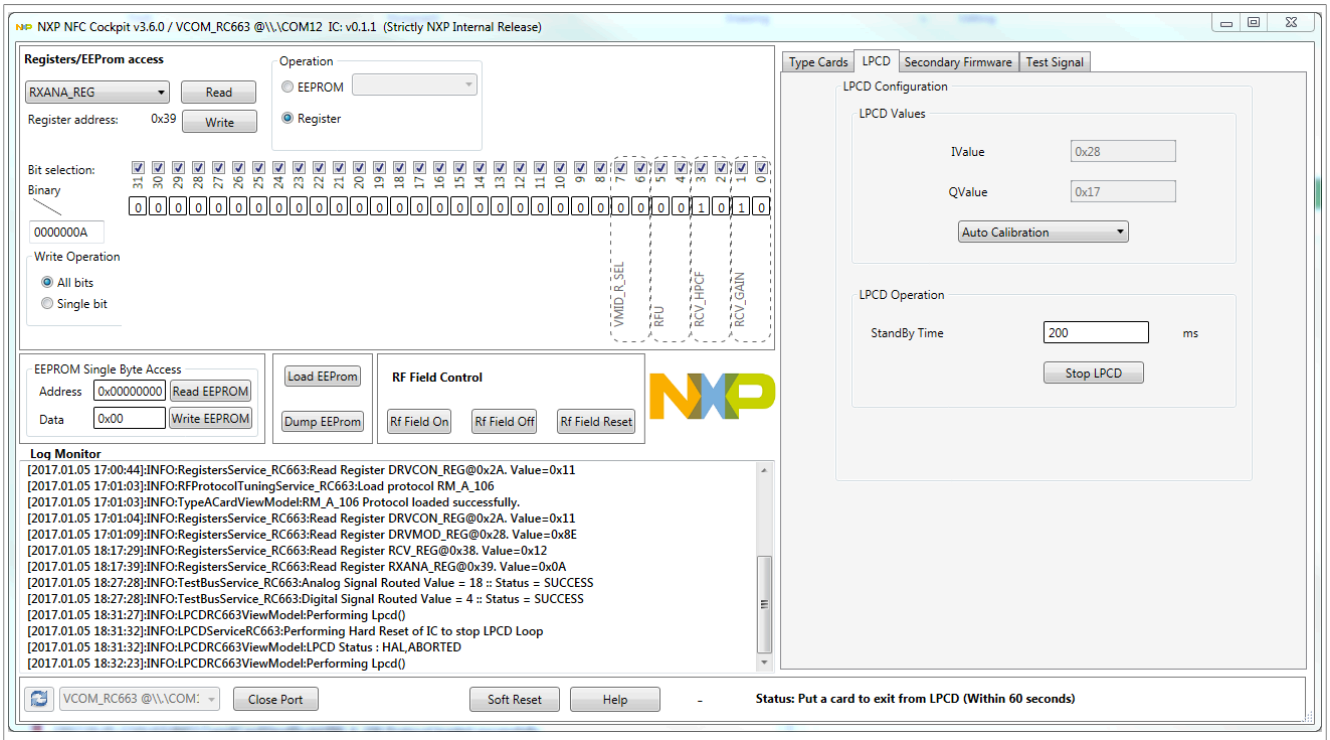


Figure 18. CLRC663 LPCD

3.2.4 Secondary firmware options: EMVCo loopback application

The NFC Cockpit offers the option to flash (“load”) and start applications into the LPC µC. The default application is an EMVCo loopback function, but other samples are provided within the NFC Cockpit delivery package.

Each application can be easily flashed into the LPC by pressing the <Load Secondary Firmware>. The application then defines the user commands, as indicated in the NFC Cockpit.

The Figure 19 shows the default with the EMVCo loopback which can be started and stopped.

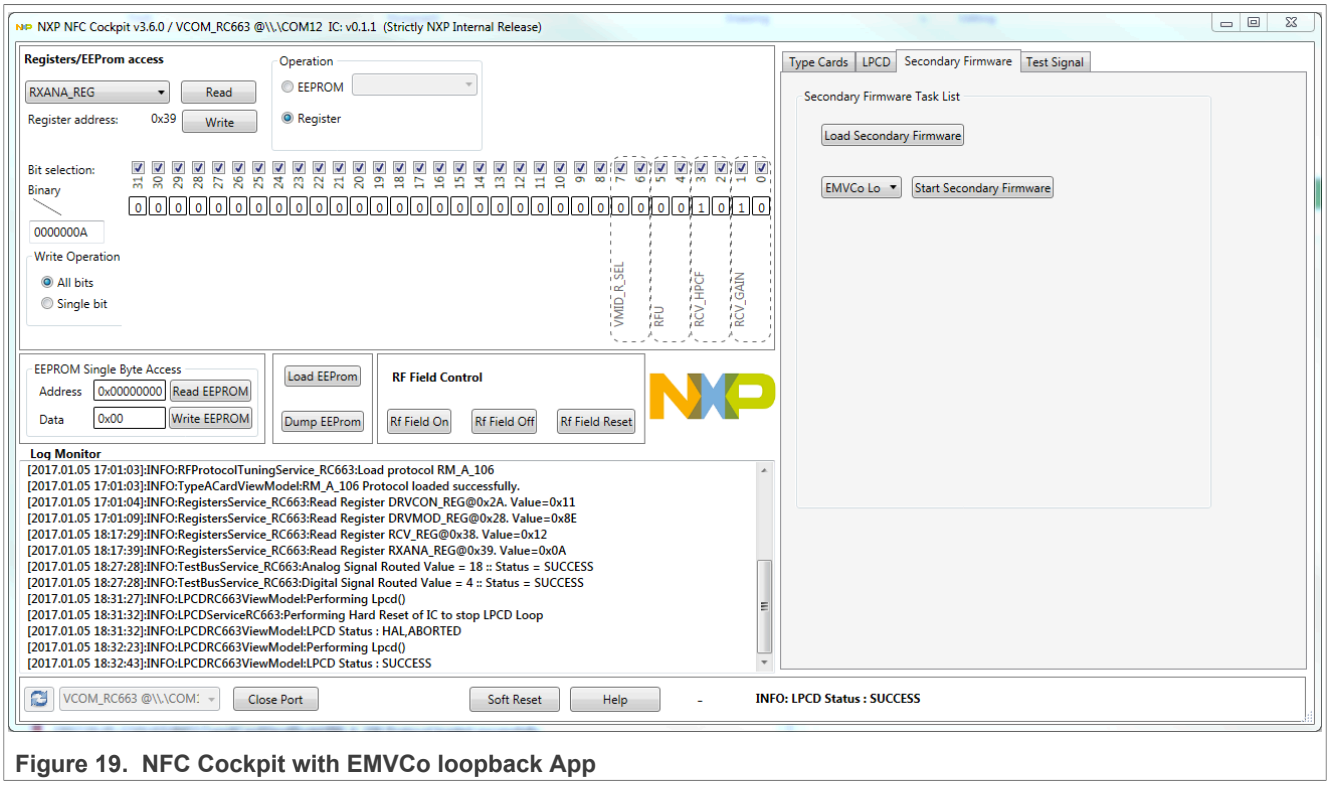


Figure 19. NFC Cockpit with EMVCo loopback App

4 First-time use

Make sure that the LPC1769 is flashed with the correct Secondary FW (default after delivery). Check [5] in case the CLEV663 had been used with customized code before and the proper secondary firmware has to be flashed.

4.1 Jumper settings

The default jumper settings allow a direct use with the USB connector only. This might show limited performance due to a current limitation on the USB host. So for real performance measurements the external power supply should be used.

4.1.1 USB only

The jumper settings as shown in Figure 11 provide the default settings, using only USB for power supply (no external supply required).

4.1.2 External power supply

For the use of an external power supply, the jumper J101 must be changed as shown in Figure 12.

The external power supply must provide a voltage level of V_{ext} = 7 V … 12 V with 500 mA.

For some of the analog tests (i.e. measuring ITVDD) it might be useful to only power the TVDD supply externally. This can be done using the jumper JP300, as shown in Figure 20.

Either the jumper can be replaced with a DC ampere meter to measure the ITVDD, or an external 5 Vdc power supply can be directly connected to the center pin of JP300.

Note: Several GND pins are provided on the board. They are all connected to the same GND plane.

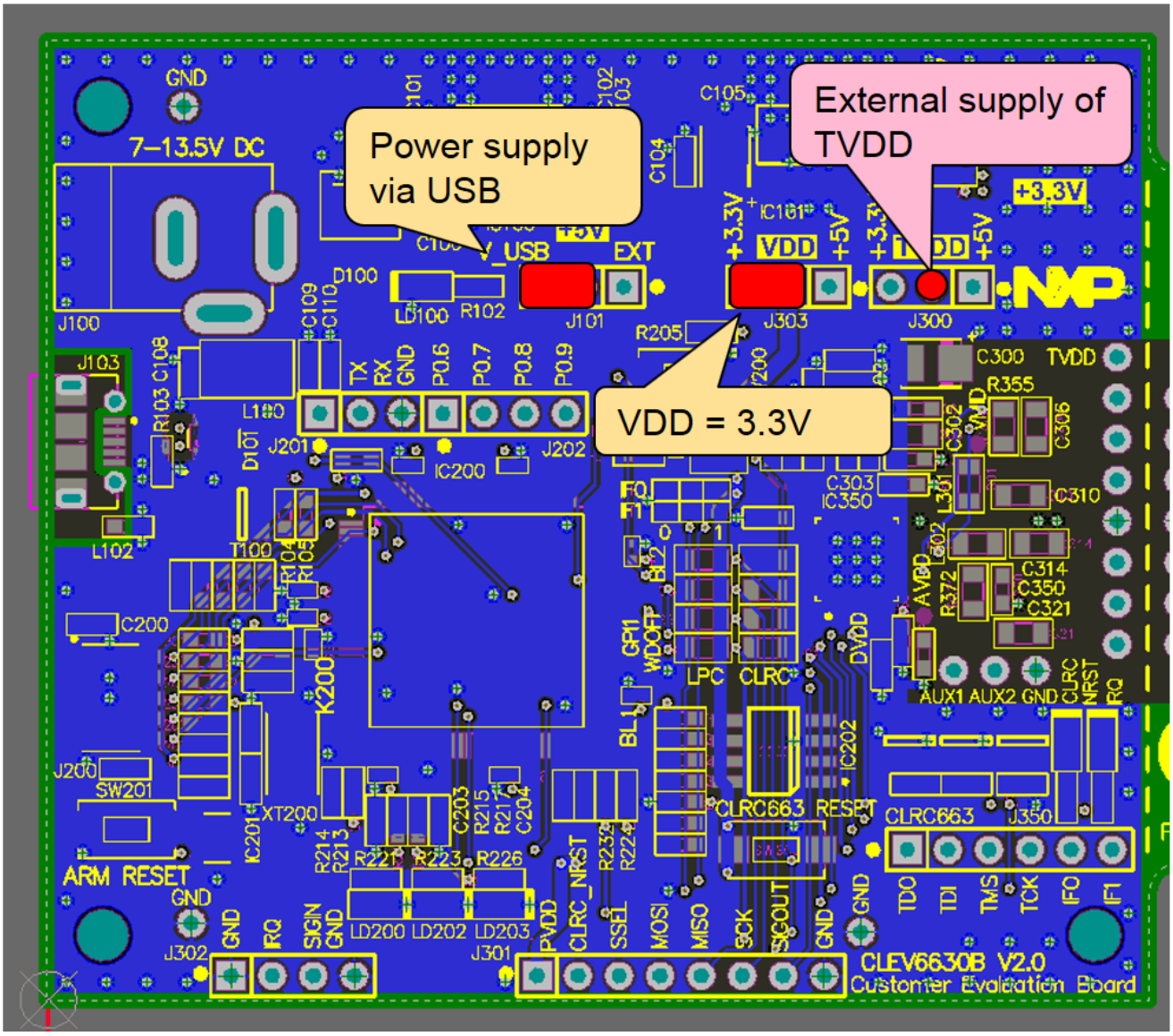


Figure 20. CLEV6630A / CLEV6630B jumper settings with external TVDD

JP300 can be used to externally supply TVDD.

5 Managing the CLRC663 SW projects with MCUXpresso IDE

The CLRC663 SW projects are delivered in a *NFC Reader Library for CLRC663* package available through the product page [1] or through Secure Files on NXP.com (https://www.nxp.com/mynxp/secure-files) in case of export controlled version. The example projects can be build and run with MCUXpresso IDE [7].

The MCUXpresso IDE is a low-cost highly integrated software development environment for NXP's LPC microcontrollers. It includes all the tools necessary to develop high-quality software solutions in a timely and cost effective fashion. MCUXpresso IDE is based on Eclipse and has many enhancements to simplify development with NXP LPC microcontrollers. It also features the industry-standard GNU tool chain, with a choice of a proprietary optimized C library or the standard “Newlib” library. The MCUXpresso IDE can build an executable of any size with full code optimization.

Designed for simplicity and ease of use, the MCUXpresso IDE provides software engineers a quick and easy way to develop their applications.

This tool can be freely downloaded from the MCUXpresso website [7]. Before one can download the software, it is necessary to create an account. Creating an account is free.

5.1 Development environment

To use CLEV663 prepared software package, all components listed in the Table 1 are required.

Table 1. Development environment

Item	Version	Description
CLEV6630A / CLEV6630B	1.0 or higher	CRC663 Customer evaluation board (hardware)
MCU-Link, LPC-Link, or SEGGER J-Link	1.0 or higher	Standalone debug adapter (hardware)
MCUXpresso IDE	11.6.0 or higher	Development IDE (PC software)

5.2 Installation procedure of the MCUXpresso IDE

The MCUXpresso IDE is installed into a single directory of your choice. Unlike many software packages, the MCUXpresso IDE does not install or use any keys in the Windows Registry, or use or modify any environment variables (including PATH). That results in a very clean installation that does not interfere with anything else on your PC. Should you wish to use the command-line tools, a command file is provided to set up the path for the local command window.

Multiple versions can be installed simultaneously without any issues.

The installation starts after double-clicking the installer file.

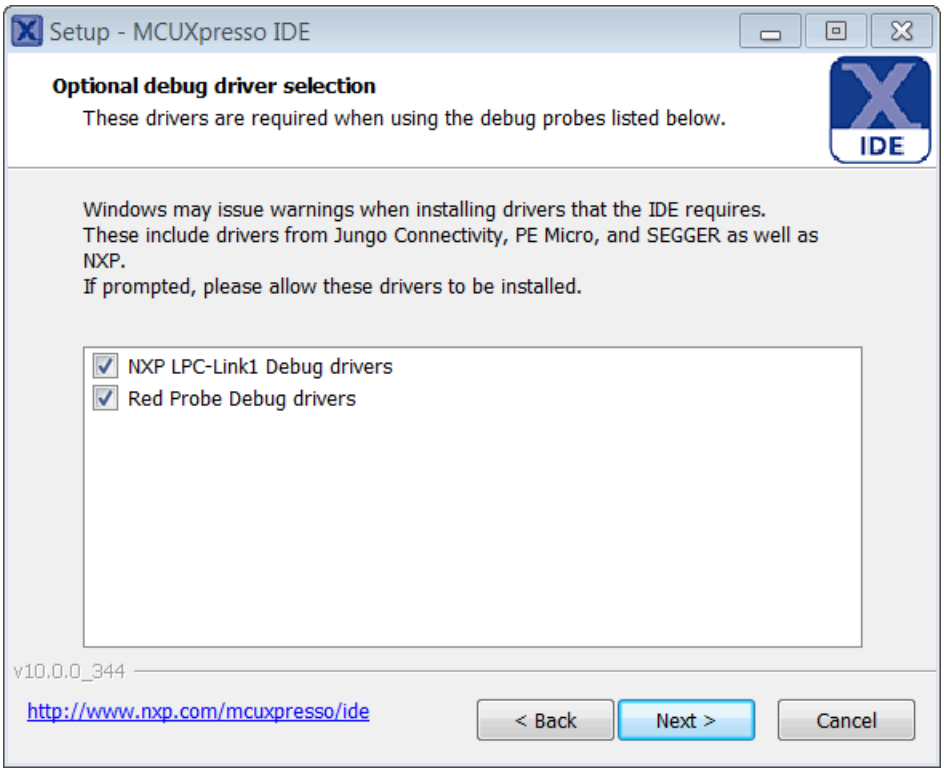


Figure 21. Checkbox for NXP debug drivers

Make sure, the checkbox for installing the NXP debug drivers is activated.

During the installation, the user is asked to install some required drivers. The installation of these drivers shall be accepted.

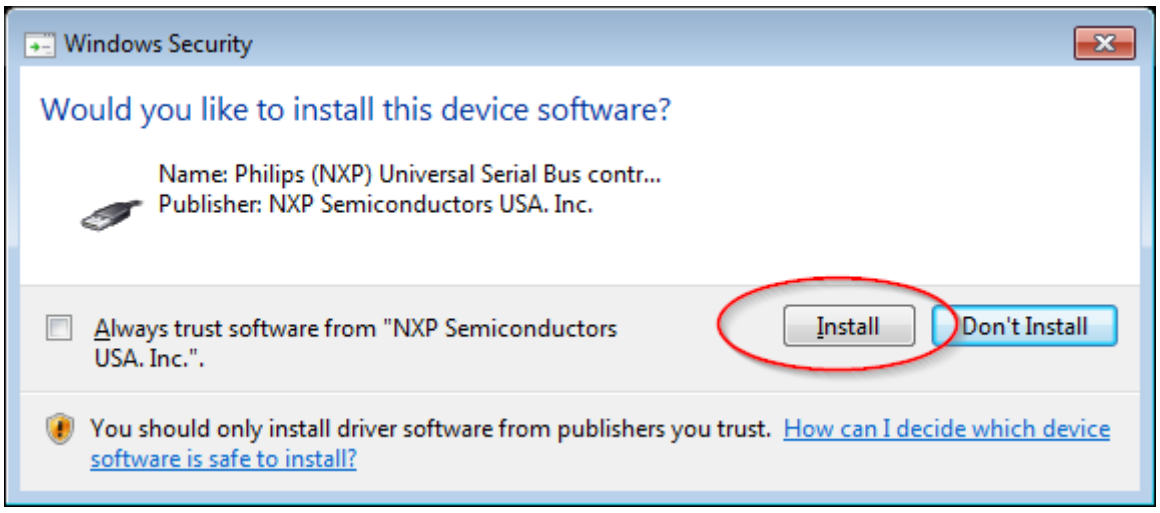


Figure 22. Windows security dialog

After the setup wizard has finished, the newly installed IDE can be launched.

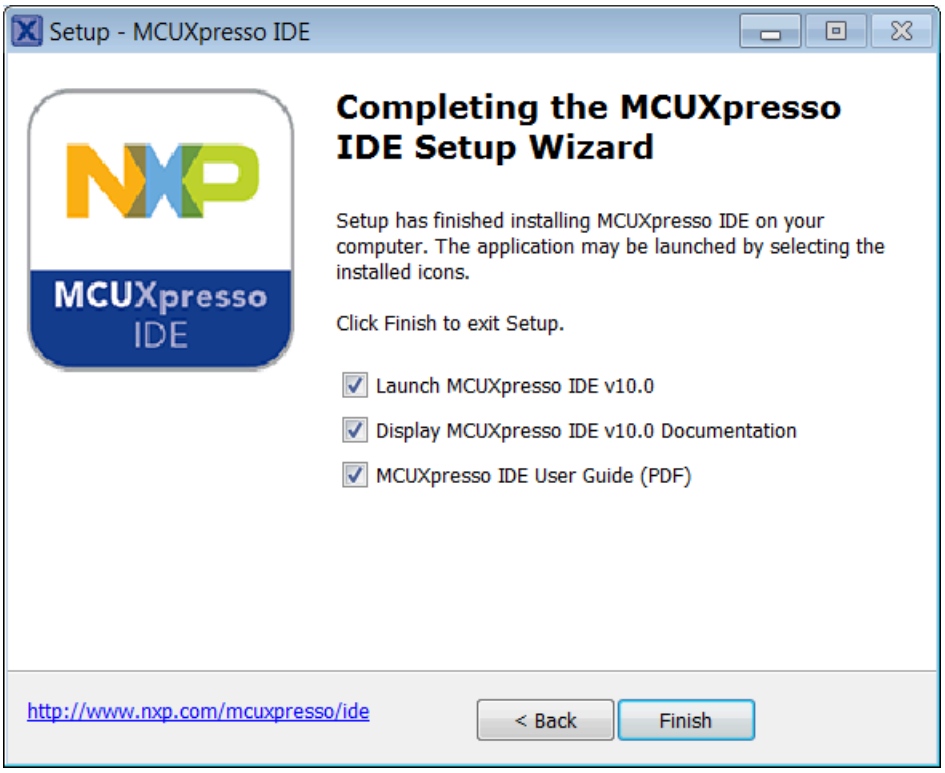


Figure 23. MCUXpresso IDE

5.3 Importing provided SW example projects

The use of the quick start panel provides rapid access to the most commonly used features of the MCUXpresso IDE. The quickstart panel allows easy import projects, create new projects, build, and debug projects.

The sequence of installing the software projects is indicated:

- Start the MCUXpresso IDE.
- Open a new or dedicated workspace
- Select the option “Import project(s)” (see picture below).
- Browse to the root folder of the previously downloaded and unzipped NFC Reader Library.
- The software package is ready for use.

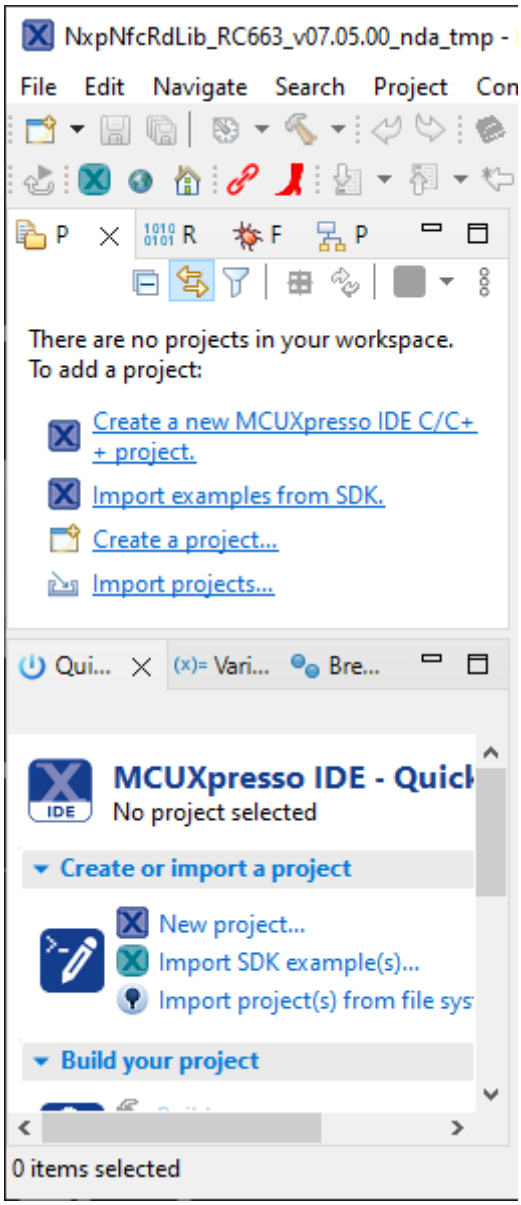


Figure 24. Importing project

In the Quickstart panel on the left-hand side, choose “Import projects(s)”.

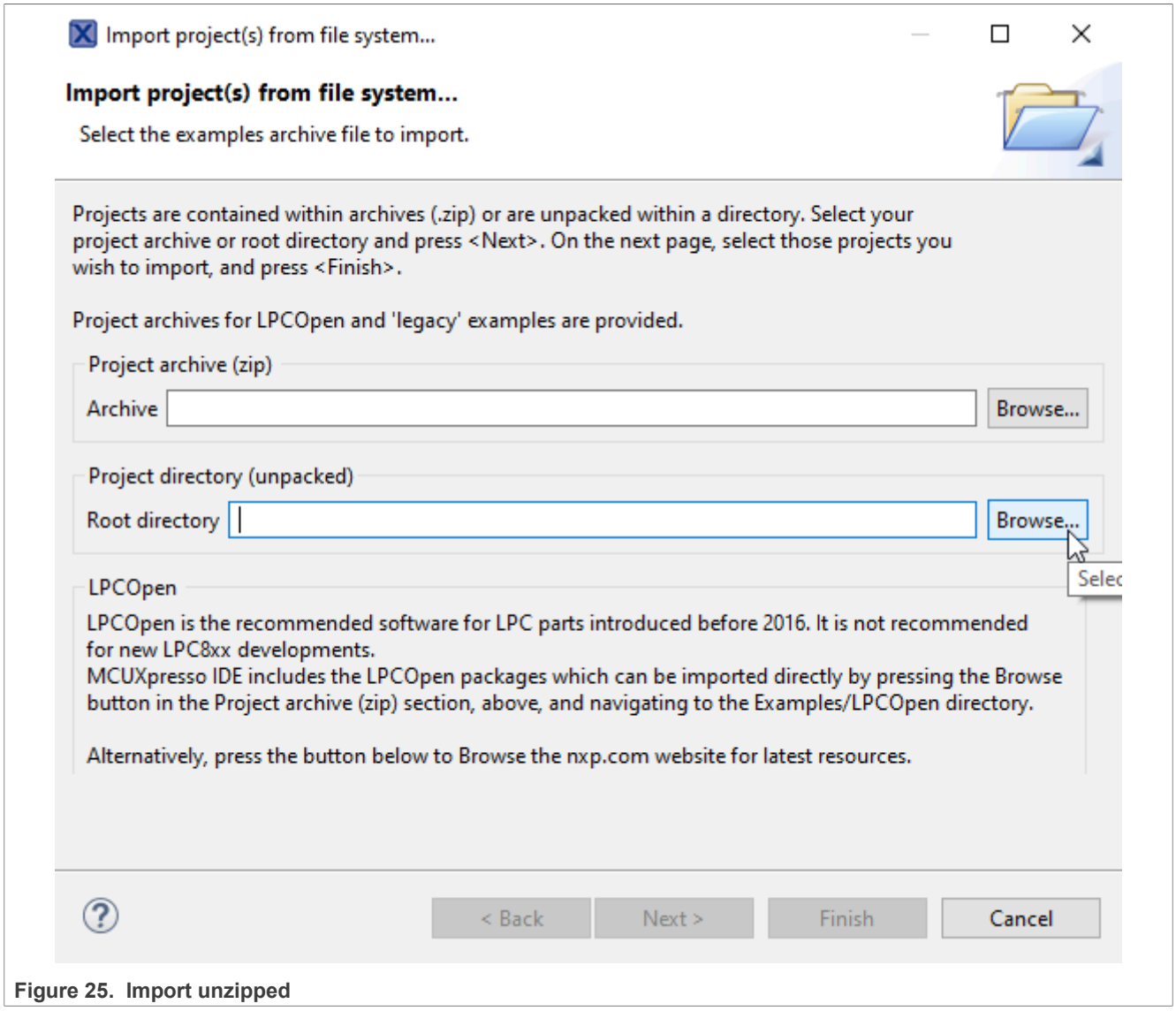


Figure 25. Import unzipped

Browse the desired package and click “Next”.

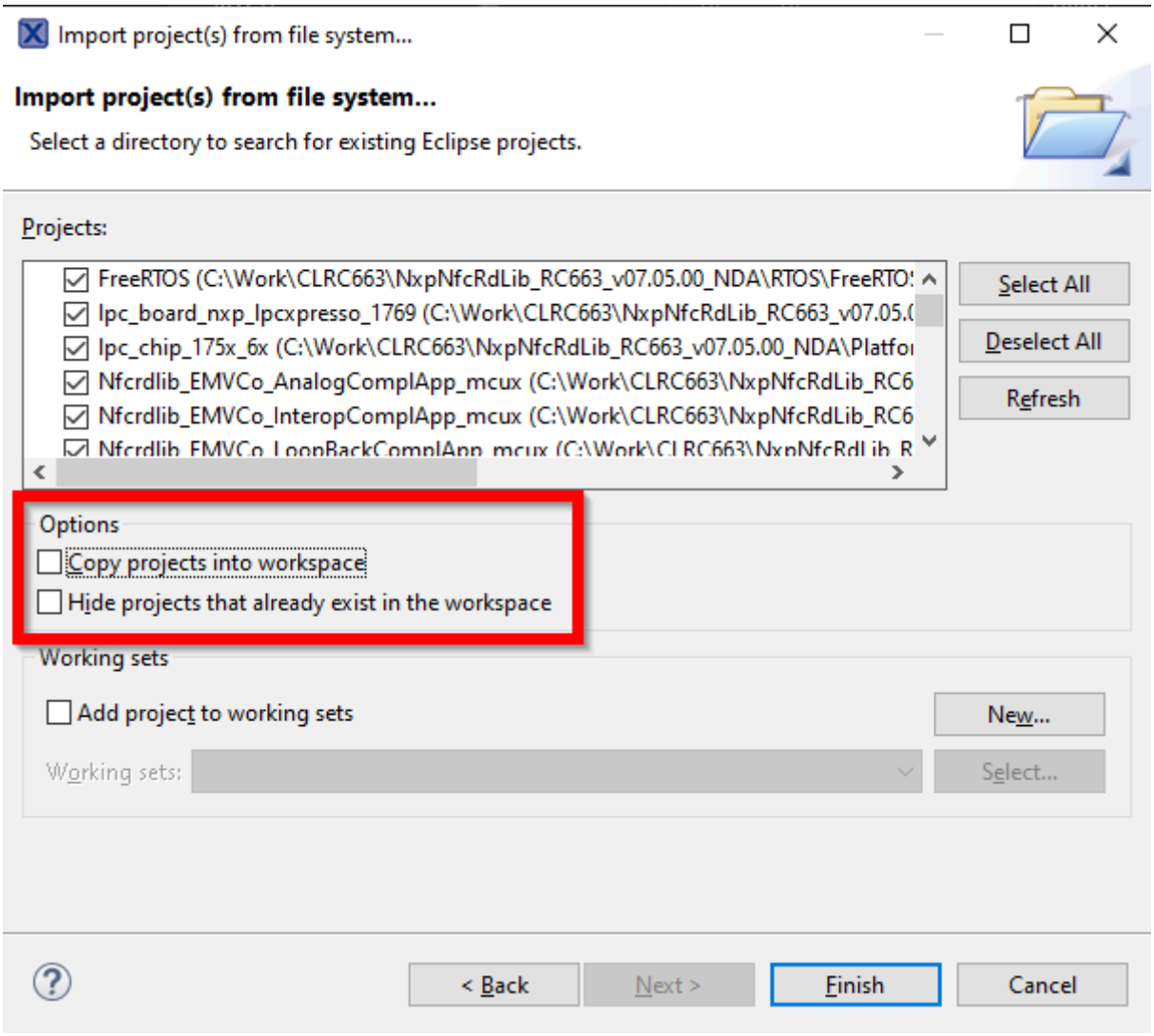


Figure 26. Import files

Make sure that the option "Copy projects into workspace" is not checked. Else cross-references will be corrupted and the example projects will not compile.

For a working demo project, you must import at least four subprojects. One example project, the NFC Reader Library, FreeRTOS, one chip library and one board library.

When the import process has finished, one can start browsing the code.

5.4 Building projects

Building projects in a workspace is a simple case of using the Quickstart Panel - ‘Build all projects’. Alternatively, a single project can be selected in the “Project Explorer View” and built separately. Note that building a single project may also trigger a build of any associated library projects.

The project can be built as shown in Figure 27.

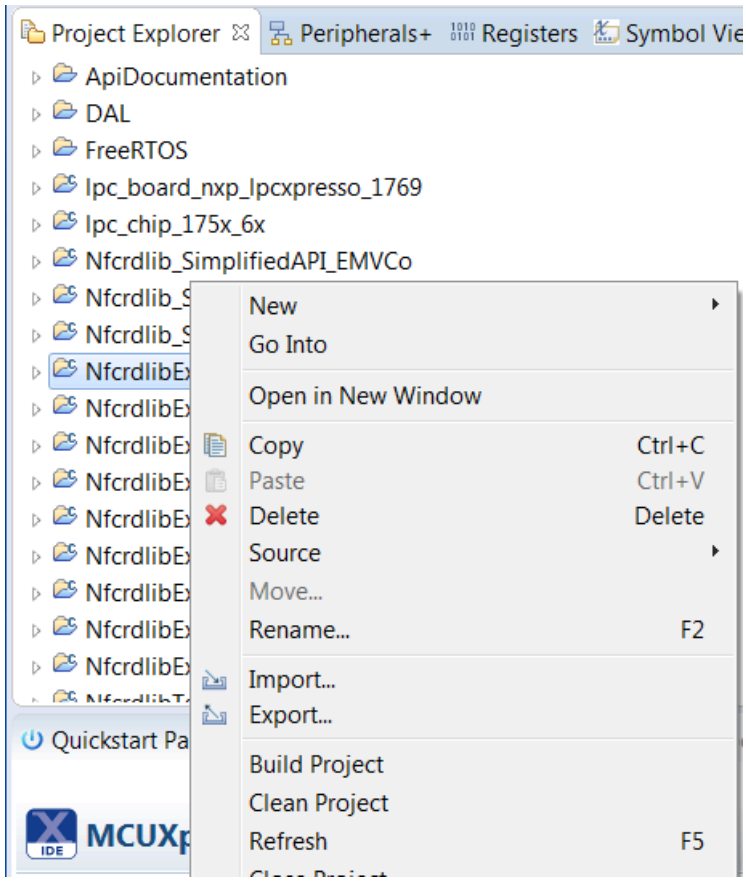


Figure 27. Building the project

As a part of the build output, the binary for the “User Flash” file is created. This binary file can also be used to update LPC1769 User Flash via USB mass storage interface.

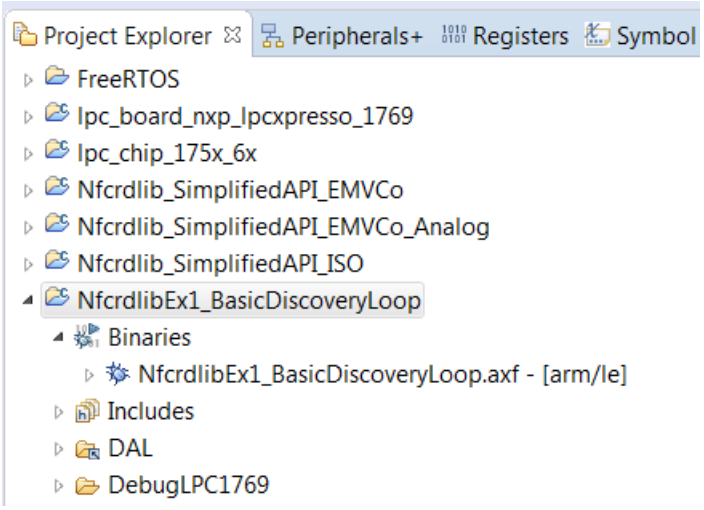


Figure 28. Generated binaries

The project settings, compiler, and link flags can be changed in the project properties dialog. To open the project properties dialog, select appropriate project in the “Project Explorer View” and click “Edit ‘selected-project’ project settings”.

5.5 Running and debugging a project

This description shows how to run the "*NfcrdlibEx1_CasicDiscoveryLoop*" example application for the CLEV6630A / CLEV6630B evaluation development board. The same basic principles apply for all other examples. Examples that require additional configuration provide detailed information in the example description.

Initially, the CLEV6630A / CLEV6630B evaluation board must be connected to the computer via LPC-Link 2, as shown in Figure 29.

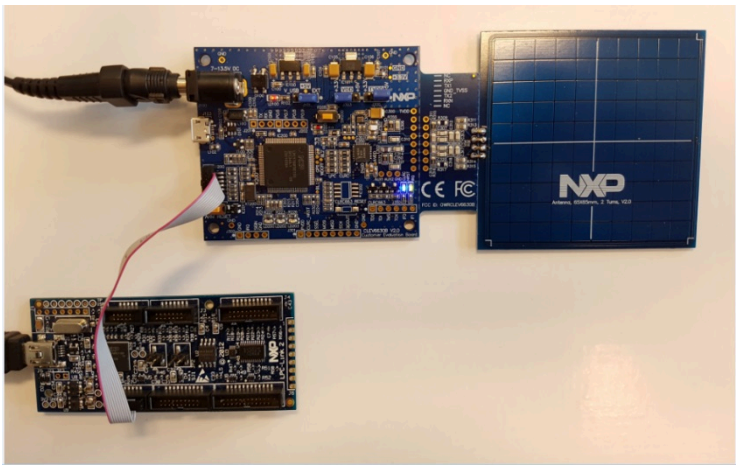


Figure 29. CLEV6630B with LPC-Link 2

When debug is started, the program is automatically downloaded to the target and it is programmed to the LPC1769 flash memory. A default breakpoint is set on the first instruction in *main()*, the application is started (by simulating a processor reset), and code is executed until the default breakpoint is hit.

To start debugging your application on the CLEV6630A / CLEV6630B, simply highlight the project in the Project Explorer and then in the *Quickstart Panel* click Debug, as shown in Figure 30. The MCUXpresso IDE will first build an application, flash application binary and then start a debug session.

Figure 30. Launch debug session

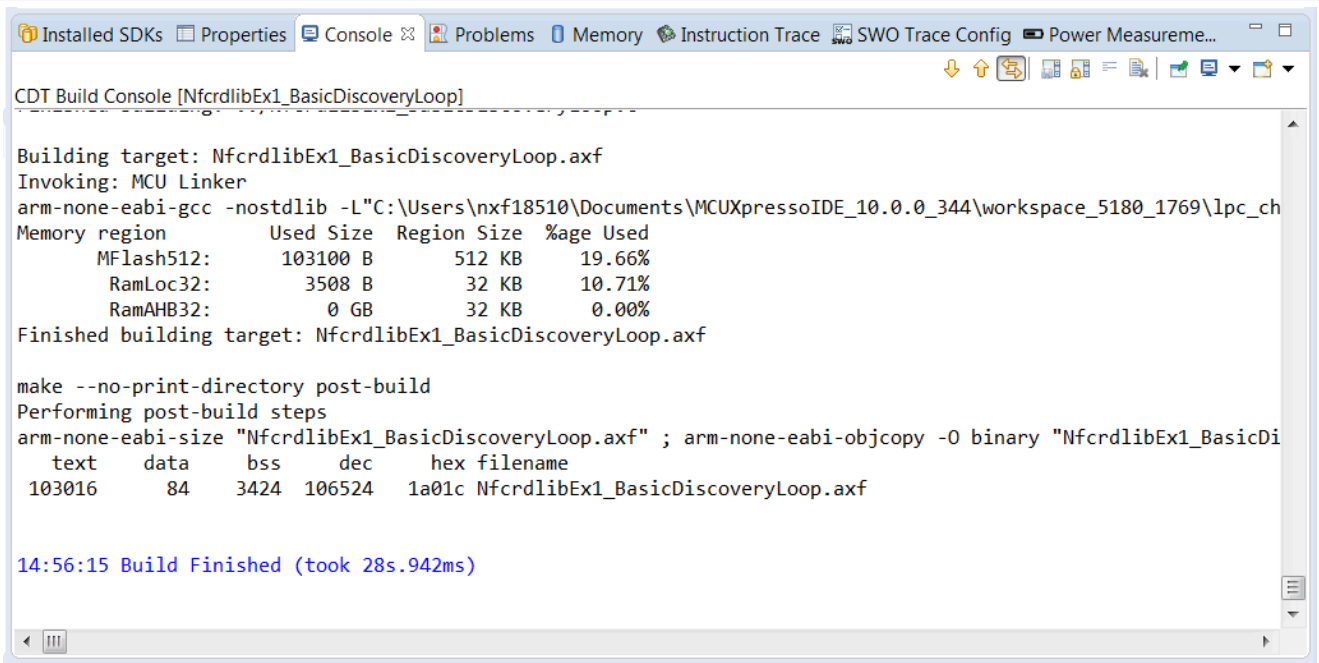


Figure 31. Successful compile

Select “LPC-Link 2” as a debug probe.

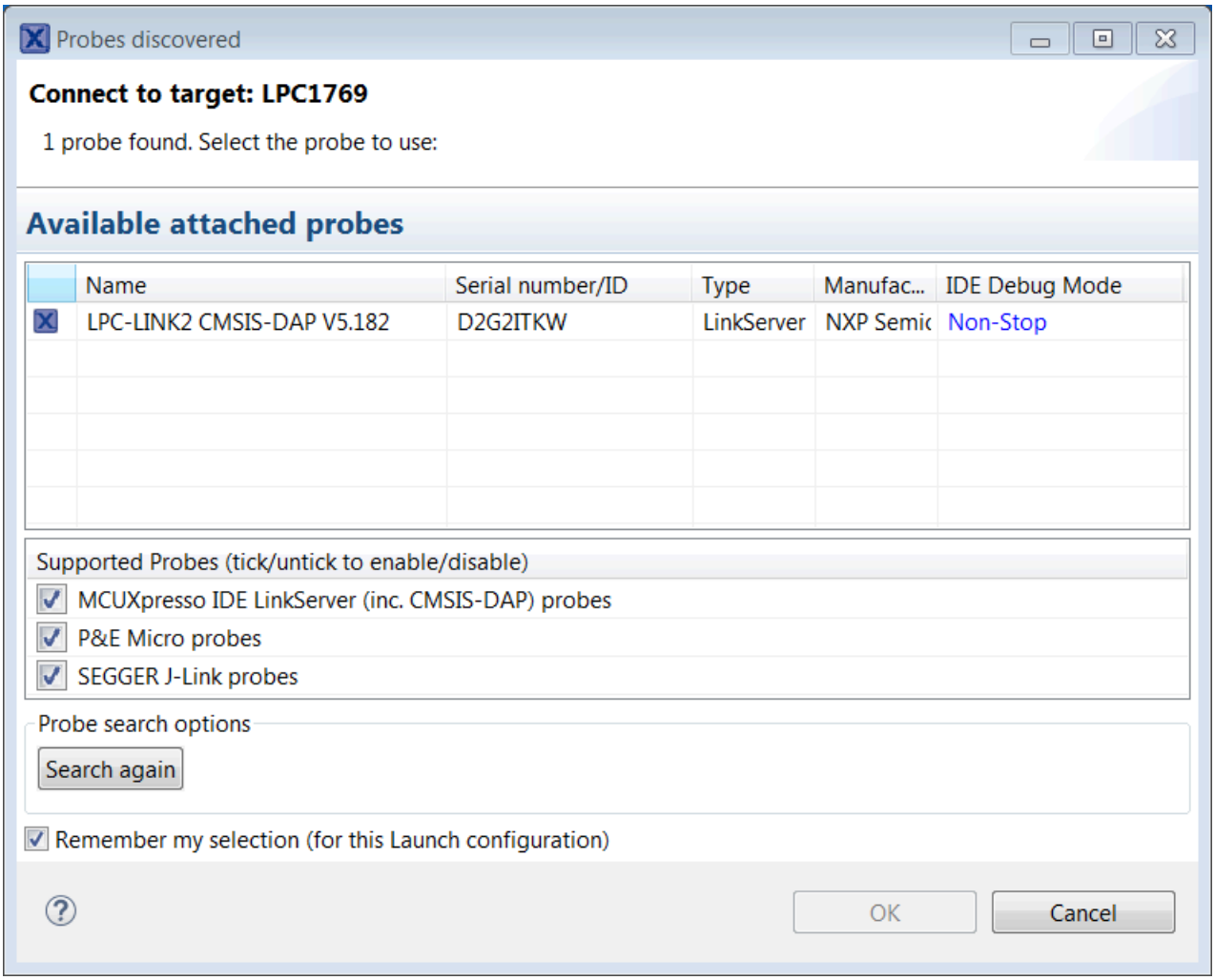


Figure 32. Select the launch configuration

After a successful software upload, the execution of the project starts immediately, but might halt at the initial breakpoint. To resume execution, click the resume button.

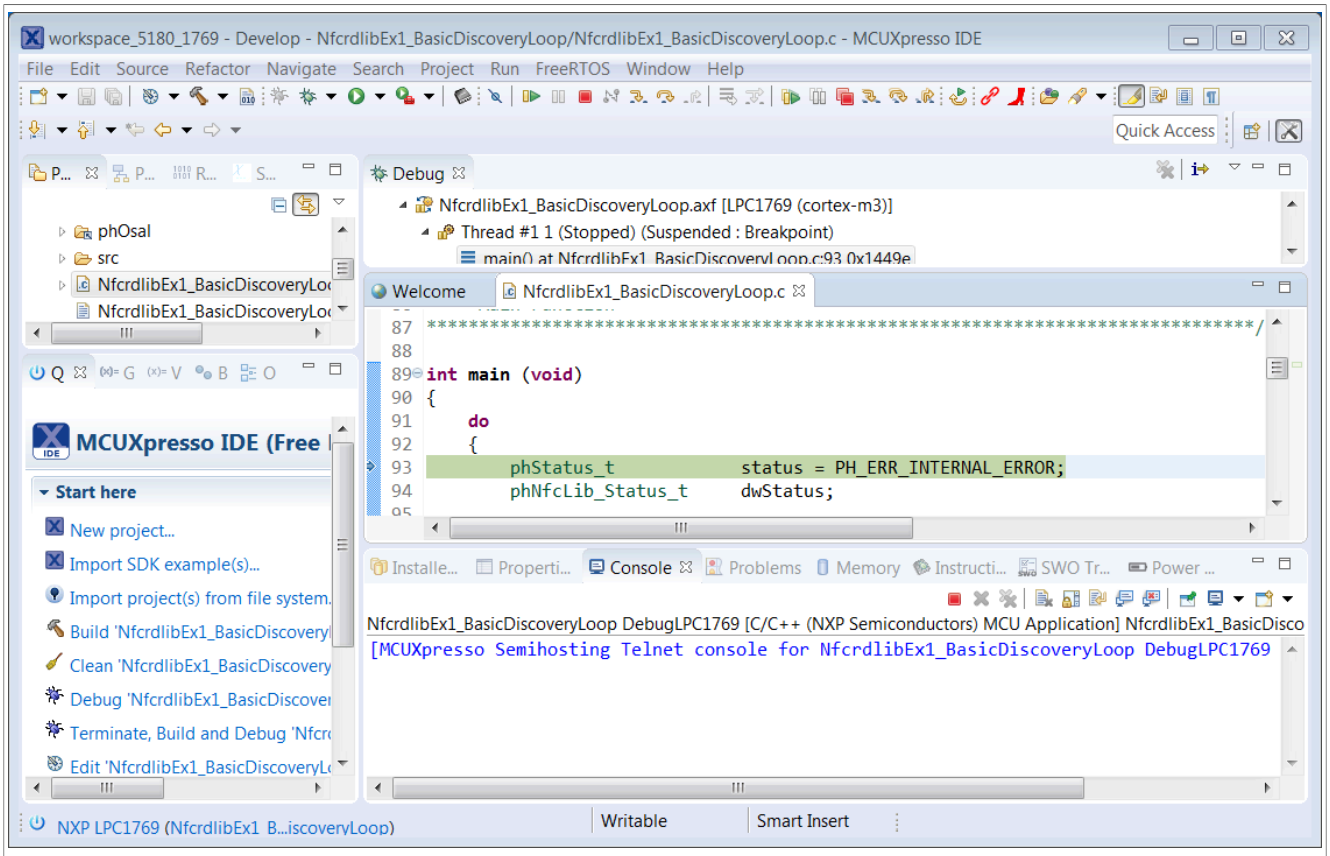


Figure 33. Debug project

In the console window, application debug outputs of the execution can be seen.

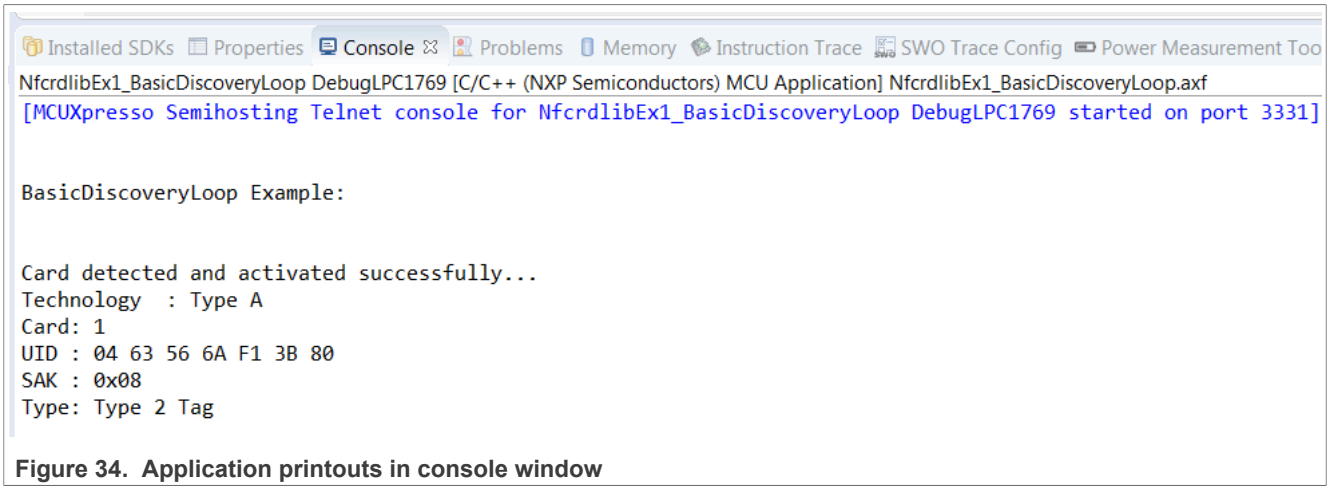
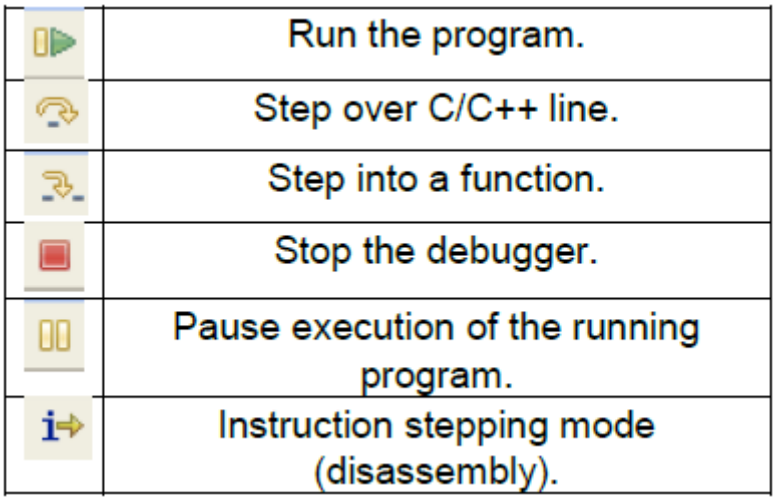


Figure 34. Application printouts in console window

After the execution has reached the end of the main function, click the Terminate button to stop the execution. Otherwise a rerun of the project will be possible.

Buttons in the debug toolbar provide next functionalities:



	Run the program.
	Step over C/C++ line.
	Step into a function.
	Stop the debugger.
	Pause execution of the running program.
	Instruction stepping mode (disassembly).

Figure 35. Dubug buttons

6 Associated projects

All example projects are available for download at the CLRC663 product page [1] in the documents section and are being distributed in one single file.

After downloading the zip file, unzip it and run the installer. The installer makes a copy of all documents and SW on the hard disk.

By default, the projects are preconfigured to be run on the CLEV6630A / CLEV6630B evaluation board. This is defined by preprocessor directive `PHDRIVER_LPC1769RC663_BOARD` (properties-> settings->preprocessor) and by defining the appropriate macro in "*../intfs/ph_NxpBuild_App.h*".

```
//#define NXPBUILD__PHHAL_HW_PN5180
#define NXPBUILD__PHHAL_HW_RC663
```

Running the projects with or without FreeRTOS

All projects described in the following subchapters can be configured to run with or without the FreeRTOS operating system. To enable or disable FreeRTOS support, define a preprocessor directive `PH_OSAL_FREERTOS` or `PH_OSAL_NULLOS` respectively (Figure 36) and rebuild the project.

(1) Project properties -> Settings -> Preprocessor

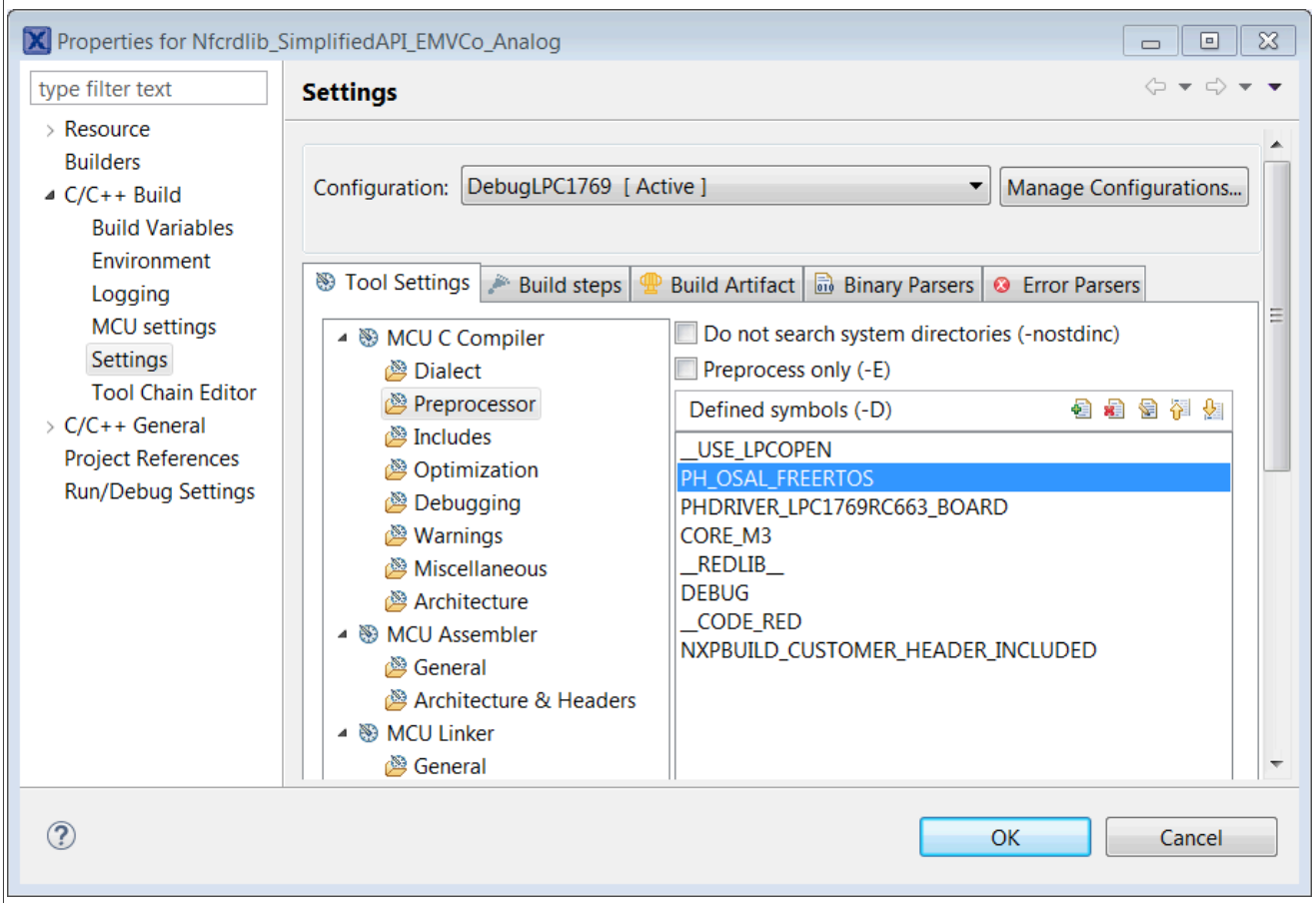


Figure 36. Defining RTOS preprocessor symbols

6.1 Example 1 – Basic Discovery Loop

The Discovery Loop is the entry point when starting to communicate with an NFC tag or device. It scans the close environment for tags and devices of different technologies.

The example is implemented to work in the POLL and LISTEN mode of the discovery loop. Information (like UID, SAK, and Product Type for MIFARE product-based cards) of the detected tags are printed out and it also prints information when it gets activated as a target by an external initiator/reader. Whenever multiple technologies are detected, example select first detected technology and resolve it.

In passive poll mode, Low Power Card Detection (LPCD) is enabled.

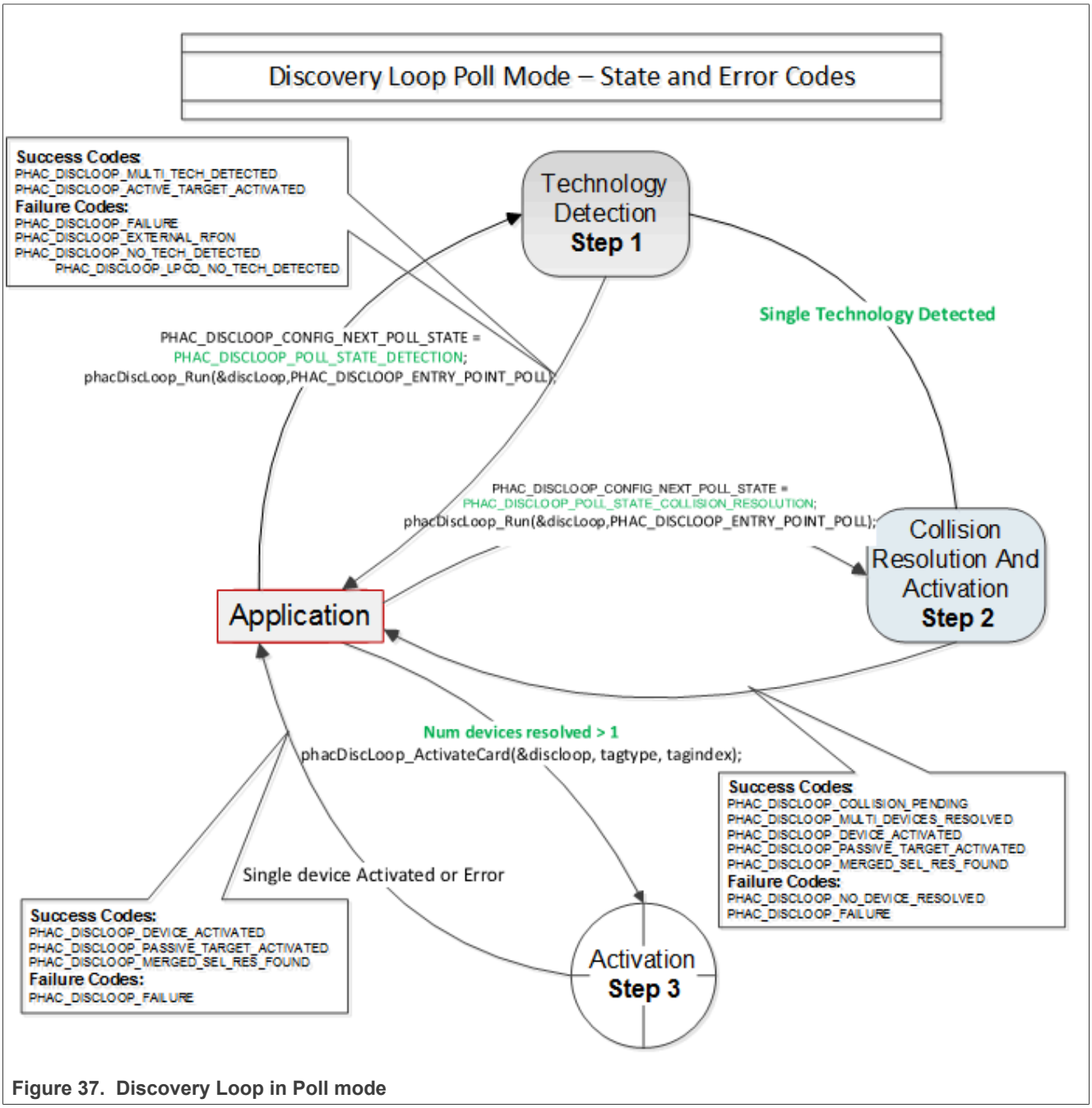


Figure 37. Discovery Loop in Poll mode

The core function of this example is “*BasicDiscoveryLoop_Demo()”,* where initialization of the NFC Reader library and polling for NFC technologies is implemented. After each polling loop, application is checking the polling result and printout information about the detected tags or devices.

This example uses the default DiscoveryLoop configuration, which enables all supported technologies and it is limited to one device for each technology.

Table 2. Supported technologies

ISO14443P3A	ISO15693- SLI	FeliCa	TYPEF_TARGET_PASSIVE
ISO14443P4A	ISO18000P3M3	TYPEA_TARGET_PASSIVE	TYPEF_TARGET_ACTIVE
ISO18092MPI	ISO14443P3B	TYPEA_TARGET_ACTIVE	

6.2 Example 2 – Advanced Discovery Loop

In addition to Example 1, the Advanced Discovery Loop example explains the different configuration options of the Discovery Loop and configure DiscoveryLoop with default values based on the interested profile, NFC, or EMVCo.

The configuration of the “DiscoveryLoop” is implemented in "*LoadProfile()*” function.

6.3 Example 4 – MIFARE Classic

This example demonstrates how to configure “DiscoveryLoop” to poll for only one technology and how to resolve detected card, in this example MIFARE Classic is used.

Once MIFARE Classic card is activated, application printout information like UID, ATQA, and SAK and perform the authentication with MIFARE Classic card default key. After successful authentication, basic read/write operations are implemented.

This example is a good start in case of working with only one card or to see how to manage MIFARE Classic cards.

6.4 Example 5 - ISO/IEC 15693

Similar to the previous example, this example only uses one technology, in that case ISO/IEC 15693. “*DiscoveryLoop*” is configured to resolve only one device and in the example it is shown how to change TX Guard Time for T5T cards, this is implemented in “phApp_Init()” function.

Once ICODE SLI is resolved and activated, the application prints out card information like the type of the card and UID, and it will read and write from/to the memory block.

This example is good start in case of working with only one card or to see how to manage the ISO/IEC 15693 type of the cards.

For a much more extensive example, demonstrating the use of ISO/IEC 15693 and ISO/IEC 18000-3 Mode 3 tags (ICODE SLI and ICODE ILT). In order to assure ICODE SLI and ILT detection, check HAL digital delay define settings as described in Section 4.

6.5 Example 7 – EMVCo Polling

The EMVCo Polling example demonstrates how to configure the NFC Reader Library as specified by EMVCo specifications and starts polling for EMVCo cards.

Once an EMVCo compatible card is resolved and activated, it demonstrates the exchange of APDU commands. This example shall help the developers getting started more quickly when working with EMVCo cards.

6.6 Example 9 – NTAG I²C

The NTAG I²C example demonstrates the use of special features, which are supported by NTAG I²C. By using the POLL mode of the discovery loop, the example detects the NTAG I²C cards and displays detected tag information like UID, ATQA, SAK, Version info and perform "*Page Read*" and "*PageWrite*" commands.

For more details about the NTAG I²C and its functionalities, consult the related product page.

6.7 Example 10 – MIFARE DESFire

The MIFARE DESFire example demonstrates how to use MIFARE DESFire EV1 cards.

Once the MIFARE DESFire card is resolved and activated, it displays MIFARE DESFire applications created by this example previously and it displays a 32-bit signed integer, which is incremented after each successful detection of tag.

In case no application is present on the tag, a new application is created with two new files to hold the NXPNFCRDLIB version used to create this application and another file to hold the 32-bit signed integer.

Note: This example including the required modules of the NFC Reader Library is only available via Secure Files on NXP.com.

6.8 Example 11 – ISO/EC 10373 PCD

This example is used to perform ISO/IEC 10373-6 PCD compliance validation. This example has to be executed in the DUT which has an ISO/IEC 14443 based PCD implementation. The ISO/IEC 10373-6 test methods verify the compliance with the ISO 14443 protocols. An external tool like Microprocess MP300 implements the test methods for the ISO/IEC 10373-6 and is used as the counterpart for this testing.

6.9 Test example 12 – CLRC663 LPCD

This example is a test suite application to test CLRC663 LPCD. This test suite contains test cases for CLRC663 HAL LPCD under different conditions. The test Cases are comprised of combinations of digital filter, charge pump, and detection options. The scenarios/combinations are as follows:

- *Scenarios 1 ==> Digital Filter: Disabled; Charge Pump: Enabled; Detection Option: NA*
- *Scenarios 2 ==> Digital Filter: Disabled; Charge Pump: Disabled; Detection Option: NA*
- *Scenarios 3 ==> Digital Filter: Enabled; Charge Pump: Disabled; Detection Option: Option 1*
- *Scenarios 4 ==> Digital Filter: Enabled; Charge Pump: Disabled; Detection Option: Option 2*
- *Scenarios 5 ==> Digital Filter: Enabled; Charge Pump: Enabled; Detection Option: Option 1*
- *Scenarios 6 ==> Digital Filter: Enabled; Charge Pump: Enabled; Detection Option: Option 2*
- *Scenarios 7 ==> In this scenario, the Calibration is performed with the load on the antennae and the load is removed during Lpcd Loop from the Antennae.*

Note: Not all of the offered LPCD functions might work with the used CLRC66302 (in case of using the CLEV6630A).

6.10 Simplified API EMVCo

This application configures Reader Library as per EMVCo specification and start EMVCo polling. This loop back application sends SELECT_PPSE command and is used to test EMVCo.3.1a(L1) digital compliance. Simplified approach, after library initialization, is using only three commands:

- `phNfcLib_Activate()`
- `phNfcLib_Transmit()`
- `phNfcLib_Receive()`

6.11 Simplified API EMVCo analog

This example contains three modes of operations within itself for the user to choose as below.

- `EMVCo LoopBack Application`
- `Trans send Type A application`
- `Trans send Type B application`

The above application modes are used to perform EMVCo2.6(L1) analog compliance validation.

6.12 Simplified API ISO

This example is a reference application to demonstrate the usage of Simplified API with ISO profile. The application contains example of Type A Layer 4, Type B Layer 4, MIFARE DESFire, MIFARE Ultralight, MIFARE Classic, ISO/IEC 5693, and ISO/IEC 18000p3m3.

The example demonstrates how to use a simplified API, which requires, after successful library initialization, only three commands:

- `phNfcLib_Activate()`
- `phNfcLib_Transmit()`
- `phNfcLib_Receive()`

7 Radio Equipment Directive (RED)

The following information is provided per Article 10.8 of the Radio Equipment Directive 2014/53/EU:

(a) Frequency bands in which the equipment operates.

(b) The maximum RF power transmitted.

Table 3. Characteristics

PN	RF Technology	(a) Freq Ranges (EU)	(b) Max Transmitted Power
CLEV6630A	NFC	13.56 MHz ±7 kHz	-11 dBm
CLEV6630B	NFC	13.56 MHz ±7 kHz	-11 dBm

EUROPEAN DECLARATION OF CONFORMITY (Simplified DoC per Article 10.9 of the Radio Equipment Directive 2014/53/EU). This apparatus, namely CLEV6630B demo board, conforms to the Radio Equipment Directive 2014/53/EU.

The full EU Declaration of Conformity for this apparatus can be found at this location: https://www.nxp.com/products/:OM26630FDK

8 References

[1] Webpage – CLRC663 plus Family: High-Performance NFC Frontends (link)
[2] Data sheet – CLRC663 – High-performance multi-protocol NFC Frontend CLRC663 and CLRC663 plus (link)
[3] Application note – AN11019 – CLRC663, MFRC630, MFRC631, SLRC610 Antenna Design Guide (link)
[4] Application note – AN11783 – CLRC663 Low Power Card Detection (link)
[5] Application note – AN11021 – CLRC663, MFRC631, MFRC630, SLRC610 Software Design Guide for NXPRDLib (link)
[6] Webpage – NFC Reader Library: Software Support for NFC Frontend Solutions (link)
[7] Software – MCUXpresso Integrated Development Environment (IDE) (link)

9 Note about the source code in the document

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10 Revision history

Table 4. Revision history

Document ID	Release date	Description
AN11022 v.1.7	31 July 2024	• Section 2 "Hardware" updated. • Section 2.2.1 "LPC1769": Figure 3, Figure 4, Figure 5 updated for quality reasons. • Section 2.2.2 "Power supply": Figure 6 updated for quality reasons. • Section 2.2.3 "CLRC663": Figure 8 and Figure 9 updated for quality reasons. • Section 7 "Radio Equipment Directive (RED)" updated. • Section 8 "References" updated. • Section 9 "Note about the source code in the document" added.
AN11022 v.1.6	17 May 2023	• Update to latest NFC Reader Library and MCUXpresso IDE • Section 7 "Radio Equipment Directive (RED)" added.
AN11022 v.1.5	28 May 2018	• Including CLEV6630A.
AN11022 v.1.4	15 May 2017	• Section 5 "Managing the CLRC663 SW projects with MCUXpresso IDE" added. • Software example descriptions added.
AN11022 v.1.3	3 May 2017	• Update with new CLEV6630B V2.0 and NFC Cockpit.
AN11022 v.1.2	14 January 2015	• Section 2.2.3 "CLRC663" updated.
AN11022 v.1.1	12 July 2012	• Some figures updated for quality reasons, Section Licenses updated.
AN11022 v.1.0	16 February 2012	• Initial release.

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Tables

Figures

Contents