# Document information

<table>
<thead>
<tr>
<th>Info</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keywords</td>
<td>GreenChip, TEA1792T/TS, TEA1792AT/ATS, Synchronous Rectifier (SR) driver, high-efficiency</td>
</tr>
<tr>
<td>Abstract</td>
<td>The TEA1792T/TS is a member of the new generation of Synchronous Rectifier (SR) controllers for switched mode power supplies. Its high level of integration allows the design of cost-effective power supplies with a very low number of external components. The TEA1792T/TS are controller IC dedicated to synchronous rectification on the secondary side of discontinuous conduction mode and quasi-resonant flyback converters. The dedicated TEA1792AT/ATS version is available for resonant convertors. The TEA1792 versions are fabricated using the Silicon-On-Insulator (SOI) process.</td>
</tr>
</tbody>
</table>
Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com
1. Introduction

The TEA1792T/TS are the controllers for Synchronous Rectification (SR) of quasi-resonant and Discontinuous Conduction Mode (DCM) flyback converters. They are successors to the TEA1791T SR controller and provide:

- improved performance
- the capability to select two different set points for the regulation level

The TEA1792 is available in pin identical packages as the:

- TEA1792T (SO8 package)
- TEA1792TS (TSOP6 package)
- TEA1792AT (SO8 package)
- TEA1792ATS (TSOP6 package)

The main difference between the TEA1792AT/ATS and the TEA1792T/TS is the shorter minimum rectification time. This feature makes the TEA1792AT/ATS ideal for higher switching frequencies (> 250 kHz) which are often used in DCM resonant converters.

Remark: Unless otherwise stated, all values are typical. Refer to the relevant product data sheet (Ref. 1, Ref. 2, Ref. 3, Ref. 4) for more specific information.

1.1 Pinning information

![Fig 1. TEA1792T/AT (SO8) pin configuration](image1)

![Fig 2. TEA1792TS/ATS (TSOP6) pin configuration](image2)

<table>
<thead>
<tr>
<th>Table 1. TEA1792 pin description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>T/AT</td>
</tr>
<tr>
<td>SRSENSE</td>
</tr>
<tr>
<td>GND</td>
</tr>
<tr>
<td>n.c.</td>
</tr>
<tr>
<td>DRIVER</td>
</tr>
<tr>
<td>n.c.</td>
</tr>
<tr>
<td>SELREG</td>
</tr>
<tr>
<td>n.c.</td>
</tr>
<tr>
<td>VCC</td>
</tr>
<tr>
<td>TS/ATS</td>
</tr>
<tr>
<td>SRSENSE</td>
</tr>
<tr>
<td>GND</td>
</tr>
<tr>
<td>n.c.</td>
</tr>
<tr>
<td>DRIVER</td>
</tr>
<tr>
<td>n.c.</td>
</tr>
<tr>
<td>SELREG</td>
</tr>
<tr>
<td>n.c.</td>
</tr>
<tr>
<td>VCC</td>
</tr>
</tbody>
</table>
2. TEA1792T/TS application diagrams

The TEA1792T/TS are developed as dedicated SR controllers for flyback converters. The TEA1792AT/ATS derivatives are developed to provide support for synchronous rectification in resonant converters. The main difference between the two versions is the blanking time after turn-on.

2.1 TEA1792T/TS application for flyback convertors

The application diagrams Figure 3 and Figure 4 show the configuration for high-side and low-side rectification. Both methods are valid for quasi-resonant and discontinuous conduction mode flyback converters using the TEA1792T/TS.

Q\text{prim} and Q\text{sec} are the switches on the primary and secondary side respectively. The primary controller manages Q\text{prim} and the TEA1792 controller manages Q\text{sec}. The TEA1792 controller operates independently of the primary controller.
2.2 TEA1792AT/ATS application for resonant convertors

The application diagrams Figure 5 shows the configuration for a resonant convertor using the TEA1792AT/ATS.

The TEA1792AT/ATS are designed for Discontinuous Conduction Mode (DCM) adapters operating at higher switching frequencies. Resonant converters can also have higher frequency ranges (> 250 kHz). The smaller minimum rectification time of the TEA1792AT/ATS (0.95 \(\mu\)s) guarantees stable operation at switching frequencies > 250 kHz.

The TEA1792T/TS with a minimum rectification time of 2.1 \(\mu\)s is ideally suited for switching frequencies < 250 kHz.
3. Functional description and application overview

3.1 SR control

The TEA1792T/TS uses the SRSENSE pin as an input sense in the control of the drain-source voltage ($V_{DS}$) of the MOSFET. No adjustment is necessary in the SR control.

The SR MOSFET is switched on by the DRIVER pin which is connected to the gate of the MOSFET. When the drain voltage on the SRSENSE pin is $< -220 \text{ mV}$, the SR MOSFET is switched on. When the sensed voltage reaches $-30 \text{ mV}$ or $-42 \text{ mV}$, the driver output voltage is regulated to maintain the sensed voltage on the SRSENSE pin. The regulation voltage level depends on the SELREG pin setting.

At a very low drain current with the $V_{SRSENSE} > -12 \text{ mV}$, the driver is pulled to ground and the SR MOSFET is switched off.

When the secondary stroke of the flyback converter is shorter than the minimum deactivation time $t_{act(sr)(min)} (1.8 \mu s)$, the driver output is disabled. This feature saves energy during flyback converter low-load conditions. When the secondary stroke is $> t_{act(ar)(min)} (2.1 \mu s)$, the driver output is enabled.

In addition, the minimum deactivation time is used to eliminate false switch-off due to high frequency ringing at the start of the secondary stroke. The driver output is enabled when the secondary stroke time is $> 2.1 \mu s$. 

Fig 6. Synchronous rectification signals

The SR MOSFET is switched on by the DRIVER pin which is connected to the gate of the MOSFET. When the drain voltage on the SRSENSE pin is $< -220 \text{ mV}$, the SR MOSFET is switched on. When the sensed voltage reaches $-30 \text{ mV}$ or $-42 \text{ mV}$, the driver output voltage is regulated to maintain the sensed voltage on the SRSENSE pin. The regulation voltage level depends on the SELREG pin setting.

At a very low drain current with the $V_{SRSENSE} > -12 \text{ mV}$, the driver is pulled to ground and the SR MOSFET is switched off.

When the secondary stroke of the flyback converter is shorter than the minimum deactivation time $t_{act(sr)(min)} (1.8 \mu s)$, the driver output is disabled. This feature saves energy during flyback converter low-load conditions. When the secondary stroke is $> t_{act(ar)(min)} (2.1 \mu s)$, the driver output is enabled.

In addition, the minimum deactivation time is used to eliminate false switch-off due to high frequency ringing at the start of the secondary stroke. The driver output is enabled when the secondary stroke time is $> 2.1 \mu s$. 

Fig 6. Synchronous rectification signals

The SR MOSFET is switched on by the DRIVER pin which is connected to the gate of the MOSFET. When the drain voltage on the SRSENSE pin is $< -220 \text{ mV}$, the SR MOSFET is switched on. When the sensed voltage reaches $-30 \text{ mV}$ or $-42 \text{ mV}$, the driver output voltage is regulated to maintain the sensed voltage on the SRSENSE pin. The regulation voltage level depends on the SELREG pin setting.

At a very low drain current with the $V_{SRSENSE} > -12 \text{ mV}$, the driver is pulled to ground and the SR MOSFET is switched off.

When the secondary stroke of the flyback converter is shorter than the minimum deactivation time $t_{act(sr)(min)} (1.8 \mu s)$, the driver output is disabled. This feature saves energy during flyback converter low-load conditions. When the secondary stroke is $> t_{act(ar)(min)} (2.1 \mu s)$, the driver output is enabled.

In addition, the minimum deactivation time is used to eliminate false switch-off due to high frequency ringing at the start of the secondary stroke. The driver output is enabled when the secondary stroke time is $> 2.1 \mu s$. 

Fig 6. Synchronous rectification signals
The best performance is obtained when the SRSENSE pin senses the drain of the SR MOSFET directly using the external 1 kΩ series resistor.

### 3.2 Function of resistors in series with the SRSENSE pin

All TEA1792T/TS pins are protected against ElectroStatic Discharge (ESD) to prevent IC damage when handled. Some application tests can trigger ESD protection.

If the ESD protection on the SRSENSE pin is triggered, the pin is pulled to ground by the internal ESD protection component. As the SRSENSE pin senses the MOSFET drain voltage, protect the pin using a series resistor to limit surge current from a severe ESD event. Figure 3, Figure 4 and Figure 5 show how the current limiting resistor $R_{SRSENSE}$ is used to provide the ESD surge protection. A 1 kΩ resistor value is sufficient to protect the SRSENSE pin.

Sometimes false triggering of the MOSFET can occur, for example due to ringing or crosstalk due to the PCB layout. Increasing the $R_{SRSENSE}$ resistor value provides additional SR input filtering and improves performance. The drawback to this solution is increased activation and deactivation delay time values.

**Remark:** Check the application carefully to achieve the optimal configuration. More information on false triggering of the MOSFET including possible causes and solutions are described in Section 4.2.

### 3.3 VCC supply

The $V_{CC(startup)}$ voltage is 8.5 V and the $V_{CC(stop)}$ voltage is 8 V. Normally, a 1 μF multilayer ceramic capacitor is placed between the $V_{CC}$ and GND pins to smooth the supply voltage.

When the voltage on the $V_{CC}$ pin is above 8.5 V, the IC leaves the UnderVoltage LockOut (UVLO) state and activates the synchronous rectifier circuitry. The UVLO state is triggered when $V_{CC} < 8$ V and the SR driver output is kept active-low.

### 3.4 VCC auxiliary supply

In high-side rectification, the IC is supplied by an auxiliary winding which is tacked on to the secondary output winding. To get the full driver output capability, supply voltage $V_{CC}$ must be > 12 V. A supply voltage of ±15 V is targeted which is set using the power output winding and the AUX winding turns ratio.

\[
V_{CC} = \frac{N_{aux}}{N_{SEC}} \times V_{OUT} - 0.7 \ V
\]  

(1)

The average IC supply current depends on the dynamic gate charge transfer characteristic of the MOSFET.

For example; conditions of 10 V gate-drive amplitude, $V_{DS}$ of < 1 V, $C_{GS}$ 75 nC and $f_{SW} = 100$ kHz results in a drive current of 7.5 mA. The IC only consumes 1 mA. So in this case, the total supply current adds up to 8.5 mA.
3.5 Driver output

The driver circuit to the external power MOSFET gate has a source capability of 400 mA and sink capability of 2.7 A. These capabilities ensure efficient operation, enabling fast switch-on and switch-off of the power MOSFET. The source stage is coupled to a 2.1 \( \mu \text{s} \) timer. When the timer finishes, the source capability is reduced to a 5 mA to maintain the driver output voltage at the required level.

The output voltage of the driver is limited to 10 V. The high-voltage output drives all MOSFET brands to the minimum on-state resistance \( R_{\text{DSon}} \).

During start-up, the conditions \( V_{\text{CC}} < V_{\text{CC(startup)}} \) and UVLO force the driver output voltage LOW prevent false SR MOSFET switch-on.

Design a MOSFET gate series resistor into the track from the TEA1792 DRIVER pin to the SR MOSFET gate input. If this gate series resistor is required due to switching noise reduction, check the SR MOSFET switch-off state. Recheck the MOSFET at a high temperature as well.

When the power MOSFET on the primary side switches on, the drain-source voltage of the SR MOSFET rises with a high \( \text{d}V/\text{d}t \). If the \( \text{d}V/\text{d}t \) is steep, the capacitive current flows from the drain to the gate through the MOSFET capacitor \( C_{\text{DG}} \). The current and a gate resistor increases the gate voltage \( V_{\text{GS}} \). However, the voltage increase must remain well below the SR MOSFET threshold voltage \( V_{\text{th}} \) to prevent switch-on. Therefore, limit the gate series resistor to between 4.7 \( \Omega \) and 10 \( \Omega \).

3.6 SR level select

The driver regulation voltage level \( V_{\text{reg(drv)}} \) is selected using the SELREG pin. When the SELREG pin is grounded, \( V_{\text{reg(drv)}} = -42 \text{ mV} \). When the SELREG pin is left open, \( V_{\text{reg(drv)}} = -30 \text{ mV} \).

The SELREG pin has a 10 \( \mu \text{A} \) internal pull-up current source. When the pin is short-circuited to ground, the pin selects the lowest \( V_{\text{reg(drv)}} \) level. If the pin is left open, the current source creates a logic HIGH-level on this pin and the highest \( V_{\text{reg(drv)}} \) value is selected.

As a guideline, set the SELREG level to the low value of \(-42 \text{ mV}\) for MOSFETs with a high \( R_{\text{DSon}} \) of \( >10 \text{ m}\Omega \). Conversely, use the high value of \(-30 \text{ mV}\) for MOSFETs with a low \( R_{\text{DSon}} \) of \( <10 \text{ m}\Omega \). The choice has a small benefit on the behavior in low load conditions. The low value is the preferred setting when false triggering occurs as a result of large crosstalk or high current spikes in high load conditions. Always check and compare both settings for each application.
4. Recommendations to improve the application

4.1 Layout considerations

Pay careful attention to the PCB layout to ensure the best possible results. Tracks from the MOSFET drain to the SRSENSE pin and from the MOSFET source to the GND pin form a loop. This loop must be as short as possible. To achieve this, route them as close as possible and parallel to each other. This routing prevents incorrect measurement values from being obtained because of the voltage drop over the tracks.

The IC ground is used as reference by the internal circuits but it also shares the high driver output current pulses. In addition, IC ground is part of the very sensitive regulation control loop for the SR MOSFET.

The IC ground copper track must be as wide and as low ohmic as possible. Direct the IC ground track very close to the MOSFET source and position the IC near the MOSFET.

Connect the SRSENSE pin to the drain pin of the SR MOSFET using the series resistor. It is good practice to make the sense track a separate one to guarantee correct sense and regulation of the MOSFET $V_{DS}$.

4.2 Short pulse prevention

The TEA1792 uses the voltage across the MOSFET drain and source to control the gate-drive. The IC measures the $V_{DS}$ through the SRSENSE and GND pins.

As soon as the SRSENSE level is $\leq -220$ mV, the SR MOSFET is switched on. At the end of the $2.1 \, \mu$s blanking time, the SRSENSE level is resampled. When the level is $\geq -12$ mV, the IC assumes that the secondary stroke has ended and the MOSFET is switched off immediately. In the next secondary stroke, the MOSFET driver is also disabled. The blanking timer is enabled for the next cycle. At the end of the blanking time, the SRSENSE level is sampled again. In this way, no SR action is performed at low-load which results in better efficiency for this condition.

False triggering of the short pulse prevention can occur when ringing of the flyback exceeds the $2.1 \, \mu$s blanking time. See Figure 7 for a graphical representation.
At the end of the blanking time, if the SRSENSE level is near to the regulation range level, a small disturbance can trigger the MOSFET to switch off for both the current and next cycle. False triggering is most likely to happen when the following conditions are valid:

- low loads combined with a low $R_{DSon}$ MOSFET and large secondary ringing
- high current spikes in the application as a result of poor PCB-layout in combination with a high frequency source such as PFC switching

There are several solutions to eliminating or decreasing false triggering and unwanted MOSFET switch-off:

- Check both levels of the regulation voltage with the SELREG pin open or connected to ground and select the setting with the best results
- Improve the PCB-layout of the application see Section 4.1
- Use a general-purpose diode instead of a fast-diode in the primary RCD snubber network. This modification reduces the ringing at the beginning of the secondary stroke
- Connect a filtering capacitor (5 pF to 33 pF) from pins SRSENSE to GND close to the IC. Alternatively, increase the series resistor value in the SRSENSE line (see Section 3.2)
- Use a MOSFET with a higher $R_{DSon}$. A higher value of $R_{DSon}$ contributes more margin for low load conditions. In general, MOSFETs with an $R_{DSon}$ as low as 7 m$\Omega$ do not cause problems in a good design. MOSFETs with an $R_{DSon} < 7$ m$\Omega$ only have a very limited contribution to higher efficiency because of the increased capacitive switching losses. In addition, they are more expensive and more sensitive to false triggering

Fig 7. High-side application: false triggering
• Create an offset on the SRSENSE input as shown in Figure 8. The offset also contributes to better performance of low RDSon MOSFETs.

The schematic shown in Figure 8 is drawn for a low-side application for ease of explanation. However, it is valid for high-side applications as well. The explanation of the circuit is based on the component values used in Figure 8.

The components C1, R1, R2 and Z1 are added to create an offset on the SRSENSE pin. They basically form a charge pump circuit that creates –30 V across Zener diode Z1. Resistor R1 limits the peak current through Z1. The –30 V creates a 15 μA current through resistors R2 and R3. This current lowers Vsrsense by 15 mV. The –42 mV or –30 mV regulation level effectively becomes –27 mV or –15 mV. The –12 mV switch-off level is 3 mV on the drain of MOSFET Q1. Changing the value of R2 adjusts the offset.

Place resistors R1 and R2 close to the IC to avoid noise on the SRSENSE pin.

Remark: Evaluate the switch-off timing carefully. The MOSFET switches off later because the –12 mV switch-off level is also raised.
5. References

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer’s sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer’s applications and products planned, as well as for the planned application and use of customer’s third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer’s applications or products, or the application or use by customer’s third party customer(s). Customer is responsible for doing all necessary testing for the customer’s applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer’s third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.
7. Contents

| 1   | Introduction .................................. | 3 |
| 1.1 | Pinning information ........................... | 3 |
| 2   | TEA1792T/TS application diagrams .......... | 4 |
| 2.1 | TEA1792T/TS application for flyback convertors | 4 |
| 2.2 | TEA1792AT/ATS application for resonant convertors | 5 |
| 3   | Functional description and application overview | 6 |
| 3.1 | SR control .................................... | 6 |
| 3.2 | Function of resistors in series with the SRSENSE pin | 7 |
| 3.3 | V_CC supply .................................. | 7 |
| 3.4 | V_CC auxiliary supply ....................... | 7 |
| 3.5 | Driver output ................................ | 8 |
| 3.6 | SR level select ............................. | 8 |
| 4   | Recommendations to improve the application | 9 |
| 4.1 | Layout considerations ...................... | 9 |
| 4.2 | Short pulse prevention ..................... | 9 |
| 5   | References ................................. | 12 |
| 6   | Legal information ........................... | 13 |
| 6.1 | Definitions .................................. | 13 |
| 6.2 | Disclaimers .................................. | 13 |
| 6.3 | Trademarks ................................... | 13 |
| 7   | Contents .................................... | 14 |