### Abstract
This application note describes the schematic and layout requirements for using the BGA3015 as a CATV drop amplifier.
## Revision history

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<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>20121012</td>
<td>First publication</td>
</tr>
<tr>
<td>2</td>
<td>20130108</td>
<td>Updated with improved application circuit and test data</td>
</tr>
</tbody>
</table>

## Contact information

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1. Introduction

The BGA3015 customer evaluation board enables the user to evaluate the performance of the wideband CATV MMIC amplifier BGA3015.

The BGA3015 performance information is available in the BGA3015 datasheet.

This application note describes the evaluation board schematic and layout requirements for using the BGA3015 as a CATV drop amplifier between 40 MHz and 1003 MHz. The BGA3015 is fabricated in the BiCMOS process and packaged in a lead-free 3-pin SOT89 package. The BGA3015 is surface-mounted on an evaluation board with element matching and DC decoupling circuitry. The amplifier MMIC comprises a two stage amplifier with internal bias network and operates over a frequency range of 5 MHz to 1003 MHz with a supply voltage between 5 V and 8 V.

2. System features

- 15 dB gain
- Internally biased
- Flat gain between 40 MHz and 1003 MHz
- Noise figure of 2.5 dB
- High linearity with an IP3 of 40 dBm and IP2 of 60 dBm
- 75 Ω input and output impedance
- Unconditionally stable
- Excellent input and output return loss

3. Customer evaluation kit contents

The evaluation kit contains the following items:

- ESD safe casing
- BGA3015 evaluation board
- BGA3015 SOT89 samples
4. Application Information

For evaluation purposes an evaluation board is available. The evaluation circuit can be seen in figure 1 and the corresponding PCB is shown in figure 2. Table 1 shows the bill of materials.

4.1 Evaluation board circuit

The power supply is applied on the center pin of connector J3 and is applied to the MMIC via chokes L4 and L2 which provides RF blocking to the supply line. Choke L4 is put in series with choke L2 to improve the performance at frequencies below 100 MHz. Capacitors C4 and C5 are supply decoupling capacitors.

At the F-connector J1 the RF input signal is applied where capacitor C1 provides DC-blocking, followed by L1 for input matching (Z = 75 Ω). Resistors R1 and R2 are used as feedback resistors to set the gain and slope. Two resistors are used to lower the influence of the parasitic capacitance from the circuit board. Capacitor C2 provides DC-blocking between the input and output of the MMIC. Inductor L3 provides the output matching (Z = 75 Ω) at the MMICs output followed by C3 for DC-blocking before the RF signal is available at F-connector J2.
4.2 Evaluation board layout

For optimum distortion performance it is important to have enough ground vias underneath and around the MMICs ground pins. This lowers the inductance to the ground plane. The evaluation board is made with two layer FR4 material.
## 4.3 Bill of materials

### Table 1. Evaluation board BOM

<table>
<thead>
<tr>
<th>Circuit Reference</th>
<th>Description</th>
<th>Qty</th>
<th>Mfr</th>
<th>Manufacturer number</th>
<th>Supplier</th>
<th>Supplier part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>BGA3015</td>
<td>1</td>
<td>NXP</td>
<td>BGA3015</td>
<td>NXP</td>
<td>BGA3015</td>
</tr>
<tr>
<td>C1, C2, C3, C4</td>
<td>10 nF</td>
<td>4</td>
<td>Murata</td>
<td>GRM155R71E103KA01D</td>
<td>Digikey</td>
<td>490-1312-1-ND</td>
</tr>
<tr>
<td>C5</td>
<td>100 pF</td>
<td>1</td>
<td>Murata</td>
<td>GRM1555C1H101JZ01D</td>
<td>Digikey</td>
<td>490-3458-1-ND</td>
</tr>
<tr>
<td>L1, L3</td>
<td>3.9 nH</td>
<td>2</td>
<td>Murata</td>
<td>LQG15HS3N9S02D</td>
<td>Digikey</td>
<td>490-2617-1-ND</td>
</tr>
<tr>
<td>L2</td>
<td>Choke</td>
<td>1</td>
<td>Murata</td>
<td>BLM15HD182SN1D</td>
<td>Digikey</td>
<td>490-5196-1-ND</td>
</tr>
<tr>
<td>L4</td>
<td>880nH</td>
<td>1</td>
<td>Murata</td>
<td>LQH31HNR88K03L</td>
<td>Digikey</td>
<td>LQH31HNR88K03L-ND</td>
</tr>
<tr>
<td>R1, R2</td>
<td>300 Ω</td>
<td>1</td>
<td>Yageo</td>
<td>RC0402FR-07300RL</td>
<td>Digikey</td>
<td>311-300LRCT-ND</td>
</tr>
<tr>
<td>J1, J2</td>
<td>75 Ω F-connector</td>
<td>2</td>
<td>Bomar</td>
<td>861V509ER6</td>
<td>Mouser</td>
<td>678-861V509ER6</td>
</tr>
<tr>
<td>J3</td>
<td>Header 3</td>
<td>1</td>
<td>Molex</td>
<td>90121-0763</td>
<td>Digikey</td>
<td>WM8109-ND</td>
</tr>
</tbody>
</table>
5. Measurement results at Vcc = 8 V

5.1 S-Parameters

Fig 3. Input matching (S11); Vcc = 8 V

Fig 4. Output matching (S22); Vcc = 8 V
**Fig 5.**  Gain ($S_{21}$); $V_{cc} = 8$ V

<table>
<thead>
<tr>
<th>Frequency MHz</th>
<th>$S_{21}$ dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) -40 °C</td>
<td>13.0</td>
</tr>
<tr>
<td>(2) +25 °C</td>
<td>13.5</td>
</tr>
<tr>
<td>(3) +85 °C</td>
<td>14.0</td>
</tr>
</tbody>
</table>

**Fig 6.**  K-factor; $V_{cc} = 8$ V

<table>
<thead>
<tr>
<th>Frequency MHz</th>
<th>K-factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) -40 °C</td>
<td>1.3</td>
</tr>
<tr>
<td>(2) +25 °C</td>
<td>1.2</td>
</tr>
<tr>
<td>(3) +85 °C</td>
<td>1.1</td>
</tr>
</tbody>
</table>
5.2 Distortion

Fig 7. Composite triple beat (CTB); Vcc = 8 V

Fig 8. Composite second order (CSO); Vcc = 8 V

(1) Tamb = +25 °C

132 channels NTSC, Vo = 30 dBmV
5.3 Noise figure

Fig 9. Cross modulation (XMOD); Vcc = 8 V

(1) Tamb = +25 °C

132 channels NTSC, Vo = 30 dBmV

Fig 10. Noise figure (NF); Vcc = 8 V

(1) Tamb = -40 °C
(2) Tamb = +25 °C
(3) Tamb = +85 °C
5.4 Output P1dB

![Graph showing Output P1dB vs Frequency for different Tamb temperatures.]

- (1) Tamb = -40 °C
- (2) Tamb = +25 °C
- (3) Tamb = +85 °C

Fig 11. Output P1dB; Vcc = 8 V

5.5 Output IP2

![Graph showing Output IP2 vs Frequency for different Tamb temperatures.]

- (1) Tamb = -40 °C
- (2) Tamb = +25 °C
- (3) Tamb = +85 °C

f2 = f1 ± 6 MHz, input power = -20 dBm

Fig 12. Output IP2; Vcc = 8 V
5.6 Output IP3

![Output IP3 graph]

(1) Tamb = -40 °C  
(2) Tamb = +25 °C  
(3) Tamb = +85 °C

\[ f_2 = f_1 \pm 6 \text{ MHz}, \text{ input power} = -20 \text{ dBm} \]

**Fig 13. Output IP3; Vcc = 8 V**
6. Measurement results at Vcc = 5V

6.1 S-Parameters

![Graph 1: Input matching (S11); Vcc = 5V](image_url)

- (1) Tamb = -40 °C
- (2) Tamb = +25 °C
- (3) Tamb = +85 °C

Fig 14. Input matching (S11); Vcc = 5 V

![Graph 2: Output matching (S22); Vcc = 5V](image_url)

- (1) Tamb = -40 °C
- (2) Tamb = +25 °C
- (3) Tamb = +85 °C

Fig 15. Output matching (S22); Vcc = 5 V
Fig 16. Gain (S21); Vcc = 5 V

Fig 17. K-factor; Vcc = 5 V

(1) Tamb = -40 °C
(2) Tamb = +25 °C
(3) Tamb = +85 °C
6.2 Distortion

(1) Tamb = +25 °C

132 channels NTSC, Vo = 30 dBmV

Fig 18. Composite triple beat (CTB); Vcc = 5 V

(1) Tamb = +25 °C

132 channels NTSC, Vo = 30 dBmV

Fig 19. Composite second order (CSO); Vcc = 5 V
6.3 Noise figure

Fig 20. Cross modulation (XMOD); Vcc = 5 V

Fig 21. Noise figure (NF); Vcc = 5 V
6.4 Output P1dB

![Graph showing Output P1dB vs Frequency for different temperatures.]

- (1) Tamb = -40 °C
- (2) Tamb = +25 °C
- (3) Tamb = +85 °C

**Fig 22. Output P1dB; Vcc = 5 V**

6.5 Output IP2

![Graph showing Output IP2 vs Frequency for different temperatures.]

- (1) Tamb = -40 °C
- (2) Tamb = +25 °C
- (3) Tamb = +85 °C

f2 = f1 ± 6 MHz, input power = -20 dBm

**Fig 23. Output IP2; Vcc = 5 V**
6.6 Output IP3

![Graph showing Output IP3 vs Frequency](image)

(1) Tamb = -40 °C  
(2) Tamb = +25 °C  
(3) Tamb = +85 °C

\[ f_2 = f_1 \pm 6 \text{ MHz}, \text{ input power } = -20 \text{ dBm} \]

**Fig 24. Output IP3; Vcc = 5 V**
### 7. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>CATV</td>
<td>Community Antenna TeleVision</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>ESD</td>
<td>Electro Static Discharge</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>NTSC</td>
<td>National Television Standards Committee</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SMD</td>
<td>Surface Mounted Device</td>
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</table>
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<td>12</td>
</tr>
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<td>13</td>
</tr>
<tr>
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<td>Output matching (S22); Vcc = 5 V</td>
<td>13</td>
</tr>
<tr>
<td>Fig 16</td>
<td>Gain (S21); Vcc = 5 V</td>
<td>14</td>
</tr>
<tr>
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<td>K-factor; Vcc = 5 V</td>
<td>14</td>
</tr>
<tr>
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<td>15</td>
</tr>
<tr>
<td>Fig 19</td>
<td>Composite second order (CSO); Vcc = 5 V</td>
<td>15</td>
</tr>
<tr>
<td>Fig 20</td>
<td>Cross modulation (XMOD); Vcc = 5 V</td>
<td>16</td>
</tr>
<tr>
<td>Fig 21</td>
<td>Noise figure (NF); Vcc = 5 V</td>
<td>16</td>
</tr>
<tr>
<td>Fig 22</td>
<td>Output P1dB; Vcc = 5 V</td>
<td>17</td>
</tr>
<tr>
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