

# AN11377

## BFU520A ISM 433 MHz LNA design

Rev. 1 — 20 January 2014

Application note

### Document information

Info	Content
<b>Keywords</b>	BFU520, BFU530, BFU550 series, ISM-band, 433MHz 866MHz
<b>Abstract</b>	This document describes an ISM Frequency LNA design on BFU5xxA Starter kit
<b>Ordering info</b>	BFU5xxA Starter kit OM7961, 12nc 9340 678 69598
<b>Contact information</b>	For more information, please visit: <a href="http://www.nxp.com">http://www.nxp.com</a>



## Revision history

Rev	Date	Description
1	20140120	First publication

## Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Abstract

In this application note an ISM band (industrial, scientific and medical) LNA design (low noise amplifier) using a BFU5xx transistor from NXP latest wideband transistor range is described. It shows the design, simulation and implementation phases. Together with measurement results, parameters measured over temperature are shown.

The application note (AN) can be a starting point for new design(s), and/or derivative designs.

## 2. Introduction

The BFU5xxA transistor family is designed to meet the latest requirements on high frequency applications (up to approximately 2 GHz) such as communication, automotive and industrial equipment.

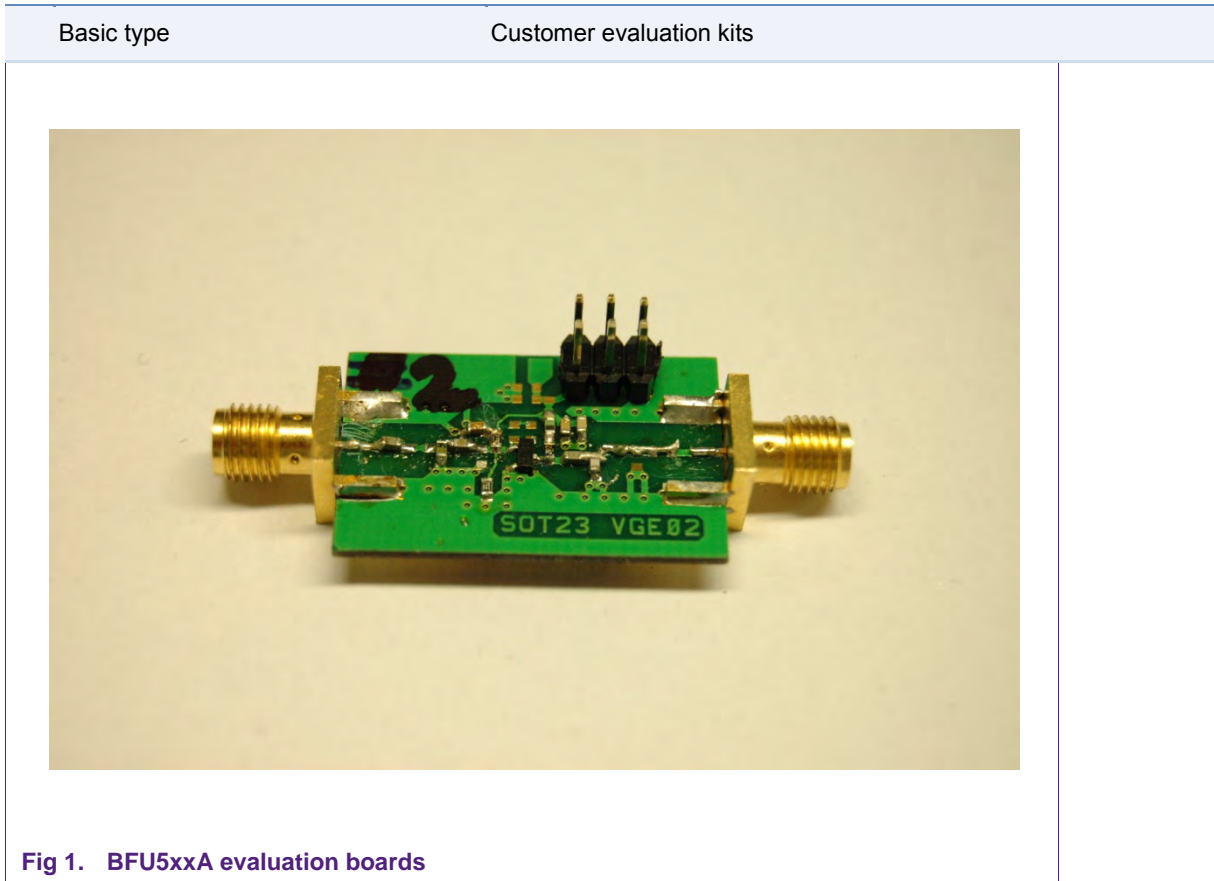
As soon as fast, low noise analogue signal processing is required, combined with medium to high voltage swings the BFU5xxA transistors are the perfect choice. Due to the high gain at low supply current those types can also be applied very well in battery powered equipment.

Compared to previous Philips / NXP transistor generations and competitor products' improvements on gain, noise and thermal properties are realized. BFU5xxA transistors are available in various packages.

The transistors are promoted with a full promotion package, called "starter kits" (one kit type per package-type). Those kits include two PCB's (one with grounded emitter, one with emitter degeneration provision), RF connectors, transistors and simulation model parameters required to perform simulations. See the overview of available starter kits in the table below.

**Table 1. Customer evaluation kits**

	Basic type	Customer evaluation kits
1	BFU520W, BFU530W, BFU550W	OM7960, starter kit for transistors in SOT323 package
2	BFU520A, BFU530A, BFU550A	OM7961, starter kit for transistors in SOT23 package
3	BFU520, BFU530, BFU550	OM7962, starter kit for transistors in SOT143 package
4	BFU520X, BFU530X, BFU550X	OM7963, starter kit for transistors in SOT143X package
5	BFU520XR, BFU530XR, BFU550XR	OM7964, starter kit for transistors in SOT143XR package
6	BFU580Q, BFU590Q	OM7965, starter kit for transistors in SOT89 package
7	BFU580G, BFU590G	OM7966, starter kit for transistors in SOT223 package



### 3. Requirements

The demonstrator circuit is designed to show the BFU520A capabilities for a 433 MHz ISM LNA with strong focus on best possible Noise Figure at low to medium supply current. The aim of the demonstrator circuit was to design a LNA optimized for the ISM band for battery powered equipment meeting following requirements:

Supply Voltage: 3.6 Volts nominal  
 Supply current: 7mA at ambient temperature  
 Noise Figure: < 1.2dB  
 Gain: approx. 17dB  
 OIP3: priority on NF but preferably >+10dBm  
 Input Return-Loss: < -8dB  
 Output Return-Loss: < -10dB

The design is aimed at low BOM cost and small PCB area, inductors are SMD types (preferable low cost multilayer types) to enable simple tuning to other frequency bands.

### 4. Design considerations

In order to achieve minimum Noise Figure, with Gain still close to the maximum available gain, the source impedance has to be close to the optimum for Noise Figure and not too far from to the maximum gain impedance. Designing for optimum Noise Figure will compromise, for example, the input return loss, but this is assumed to be acceptable.

At any time the circuit should be stable, hence during the design phase the K-factor needs to be observed carefully.

## 5. Design approach

The design starts in the simulation phase, applying the Mextram Model (available at <http://www.nxp.com>). Agilent "Advanced Design System" (ADS) was used for this but other simulation software packages should give equal results. Spice / Gummel Poon models are available.

Once simulation results meet the requirements, the circuit is built on a universal Printed Circuit Board (PCB) and evaluated. If measurement results show significant offset from simulated results, fine tuning is required until required performance is met. To achieve better matching between simulations and measurements, the PCB parasitic properties were added in the simulation template.

Following blocks of passive components can be identified:

- 1) resistors for DC biasing
- 2) passives set up collector load
- 3) passives for output matching
- 4) passives for input matching
- 5) passives required to ensure stable operation

Each block will be discussed separately below.

### 5.1 Simulation steps

Following simulation / design approach can be useful:

- 1) Configure the DC bias set-up, ensuring the  $I_{cc}$  is set around desired value.
- 2) Configure the collector load circuit and output matching circuitry, optimizing the output Return Loss (RL).
- 3) Check stability.
- 4) Configure the input matching, for LNA optimize for minimum noise figure (NF) but keep close to optimum gain, if possible optimum NF gain points should be close.
- 5) Check stability.

Assumptions:

- Realistic passives are used by applying Murata design kit (0603 / 0402)
- PCB tracks represented by strip-lines

### 5.2 Implementation / evaluation steps

Following implementation / evaluation steps have been executed:

- 1) Implement simulated design on universal PCB.
- 2) Evaluate LNA on Gain / NF / matching / Stability at ambient temperature.
- 3) Fine tune passives if required.
- 4) In case significant differences between simulations and measured results are observed, try to modify parasitic properties in the simulation template.
- 5) Measure LNA design on RF parameters over temperature.

5.3 Setting up the DC bias circuit

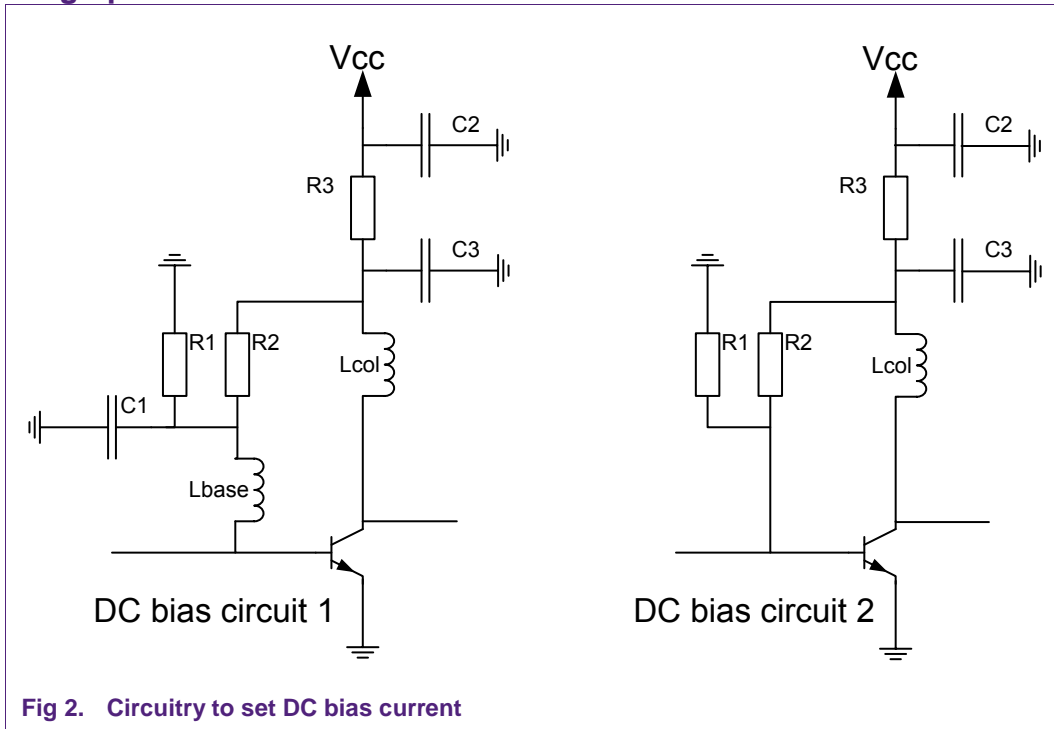


Fig 2. Circuitry to set DC bias current

Circuit 1 has the advantage that resistive noise from the resistors R1 and R2 is suppressed by capacitor C1, but at the cost of an extra inductor. This inductor can be part of the input matching.

Circuit 2 is commonly used and saves two passive components. Both circuits tend to have increasing collector current (Icc) with increasing temperature, partly stabilized by R3. Increasing R3 will have impact on the linearity (OIP3, P1dB).

### 5.4 Definition of collector load and output match

The configuration used and simulation display is shown below (ADS).

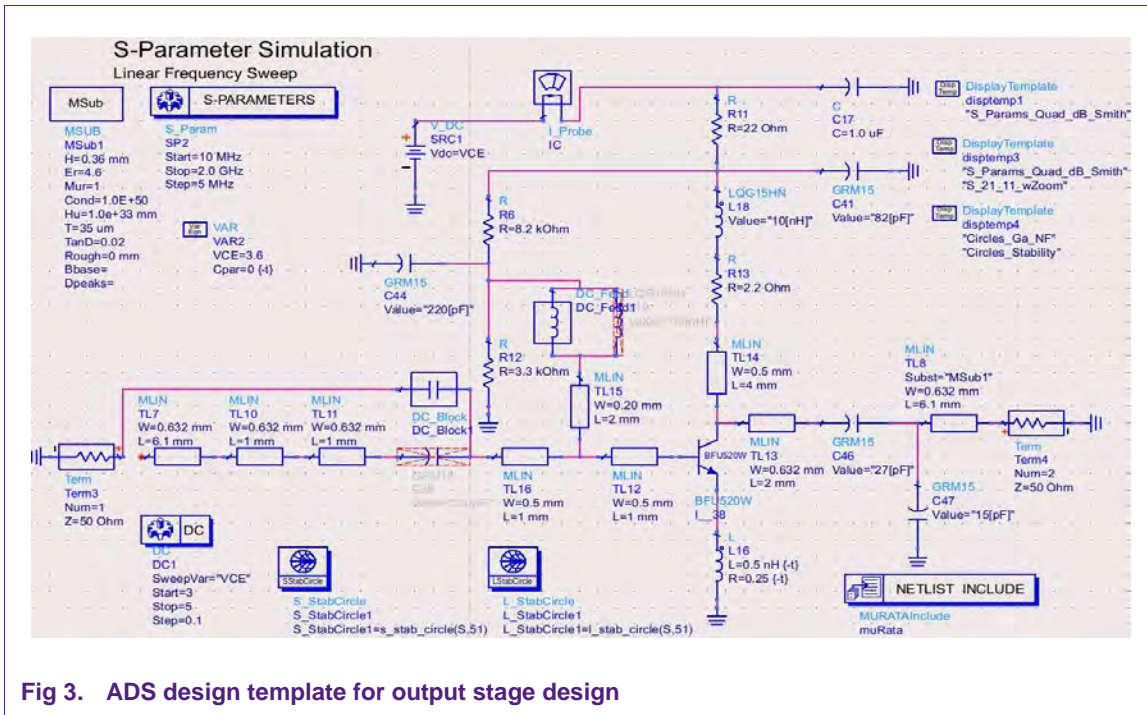
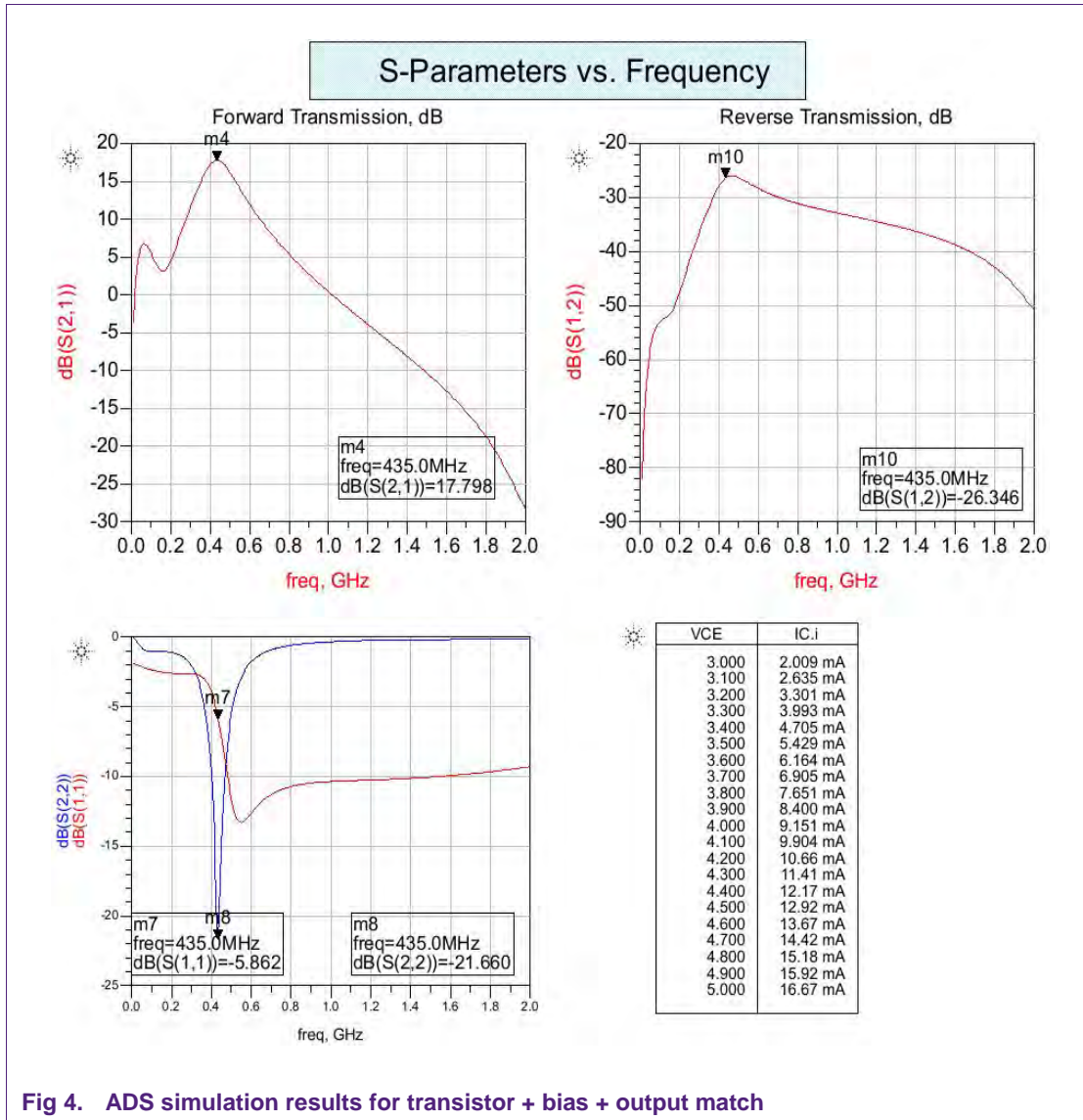


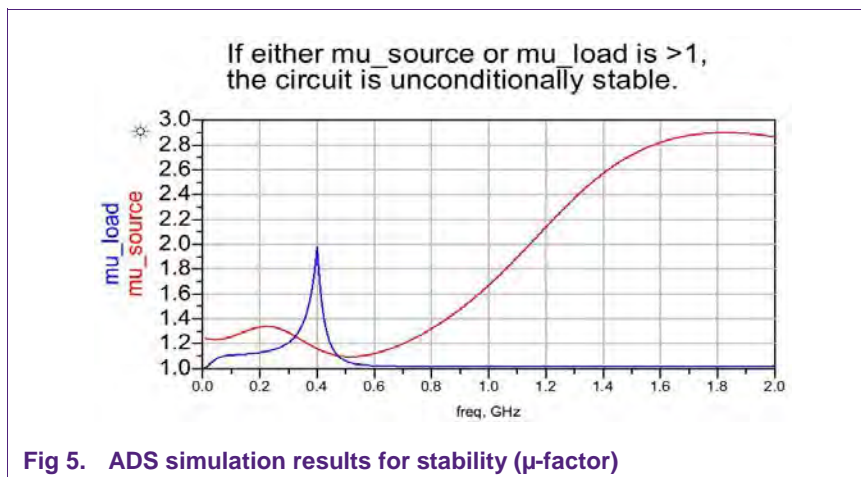
Fig 3. ADS design template for output stage design

In this simulation for the 433 MHz ISM Band the input matching circuit is bypassed. The components L18, C46, C47 are tuned to get a match in the required frequency band.





After defining the configuration for the collector load / output matching network and tuning the component values, a simulation is executed to observe the amplifiers stability. See figure below.





5.5 Definition of input / source matching circuit

In case the amplifier has to be designed to get minimum noise figure, the “noise and gain circles” can be applied.

See figure below: In the noise circles plot you can find the area for optimum source impedance, as should be seen by the base of the transistor, to achieve lowest noise figure.

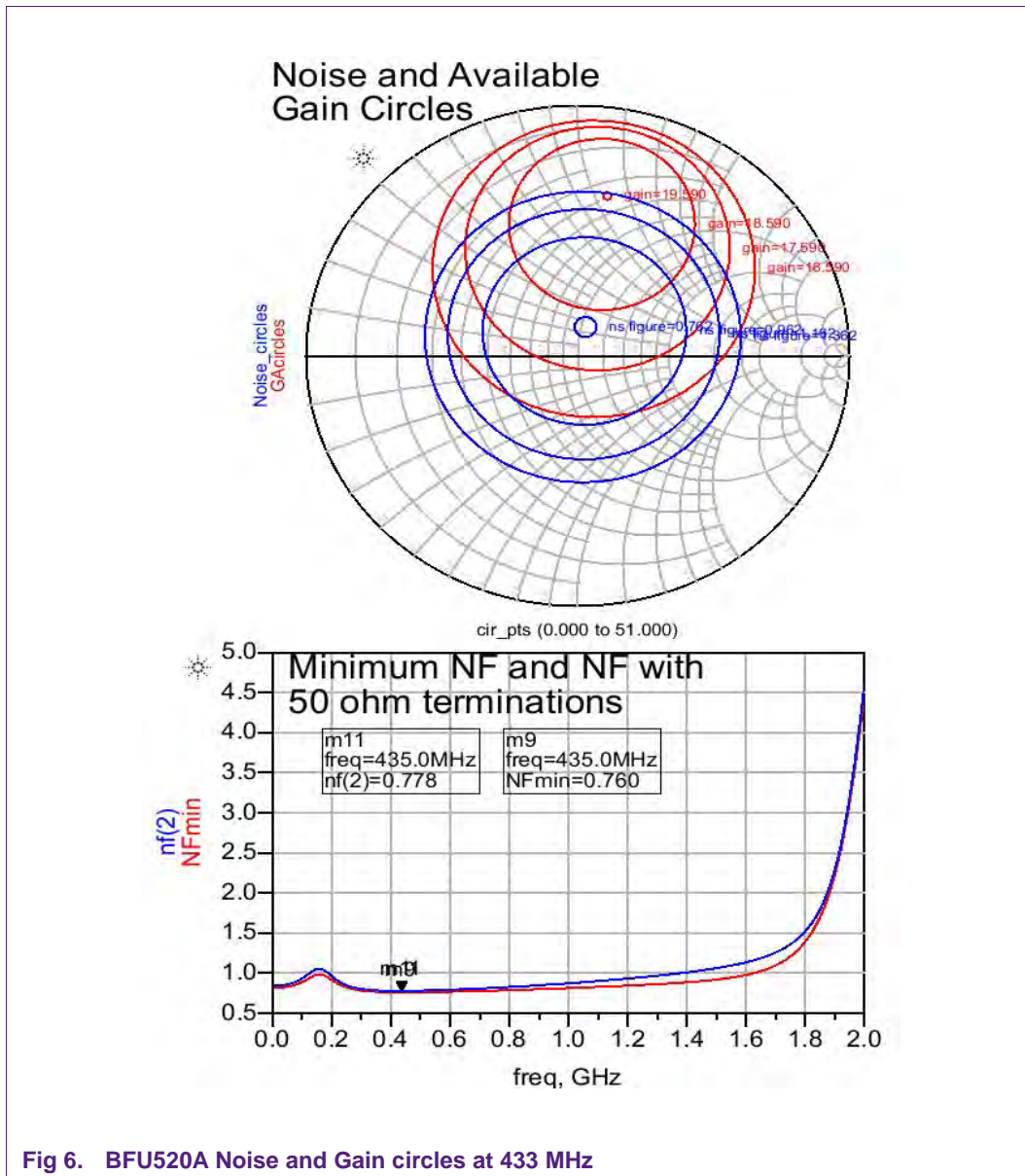


Fig 6. BFU520A Noise and Gain circles at 433 MHz

This is the result from simulations of the set-up as shown in section 5.4, Fig 3.

In this Smith Chart you can find the optimum load impedance for optimum noise in the smallest blue circle, NF 0.76dB (this is the expected NF for the transistor without matching/PCB losses). In case the source impedance is shifted into the region of the second blue circle, the NF will be increased by approximately 0.2dB.

The same applies to the Gain, but in that case the red circles needs to be considered.

The input matching network needs to be set up such that the source impedance as seen by the transistor is close to the optimum for NF, preferably also close to optimum gain circle.

In the next figure the simulation template to optimize for best source impedance is shown. Please note that the active part of the circuit is bypassed. We want to observe the S22 which is the source impedance for the transistor applied.

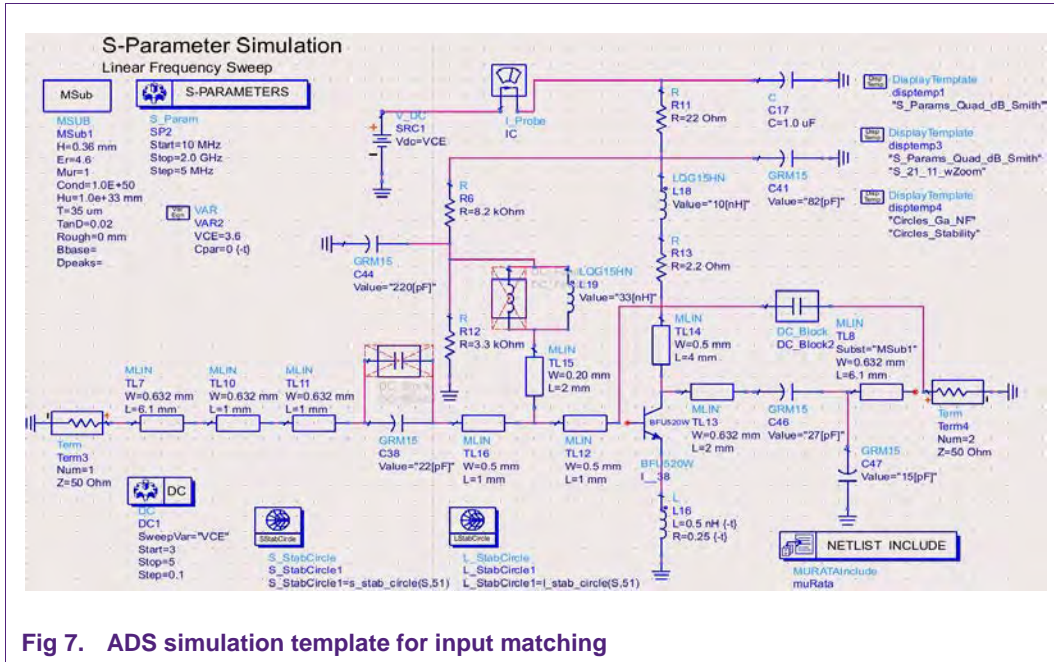


Fig 7. ADS simulation template for input matching

By tuning the components L19, C38 you could move the source impedance towards required area.

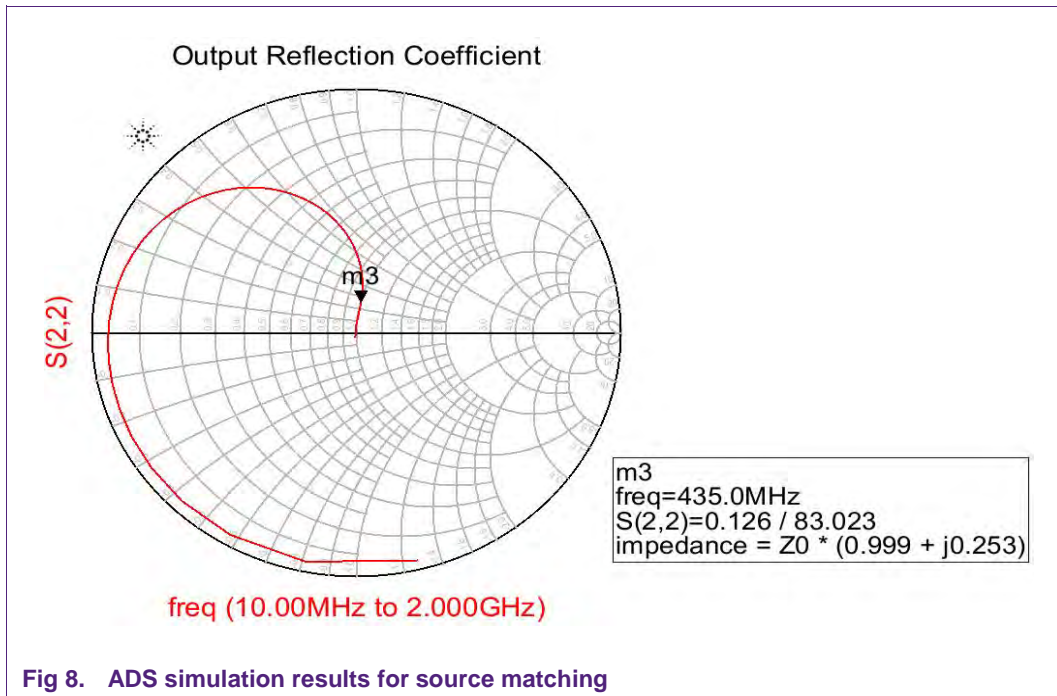


Fig 8. ADS simulation results for source matching

From this figure we see the source impedance at 433 MHz is in the area we want.

### 5.6 Overall LNA simulation

ADS template used:

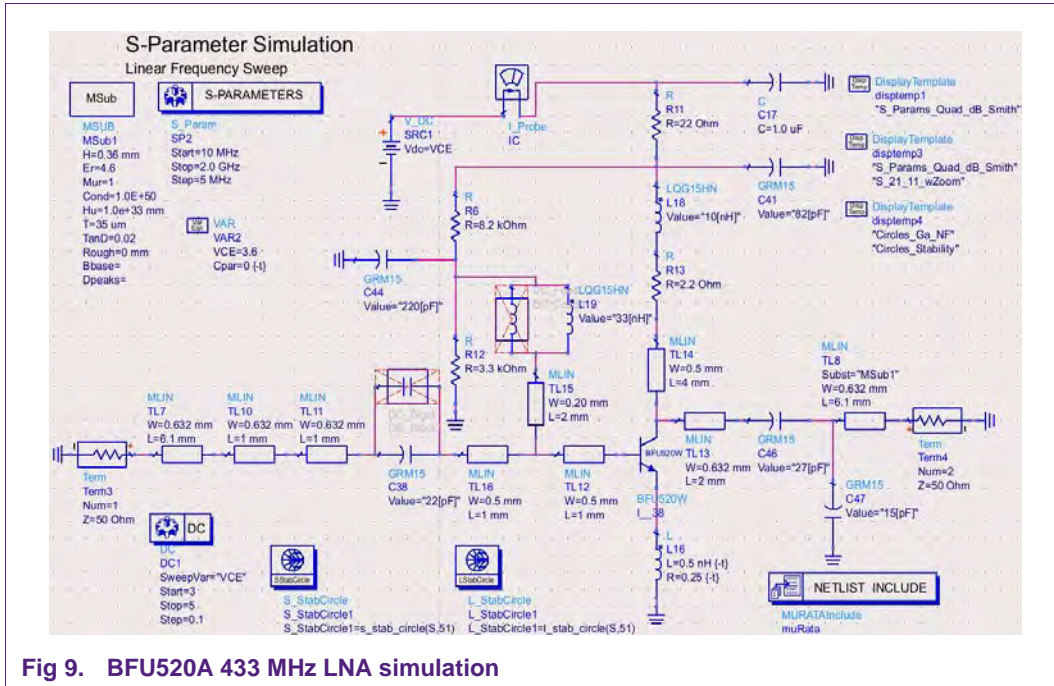


Fig 9. BFU520A 433 MHz LNA simulation

Simulation results:

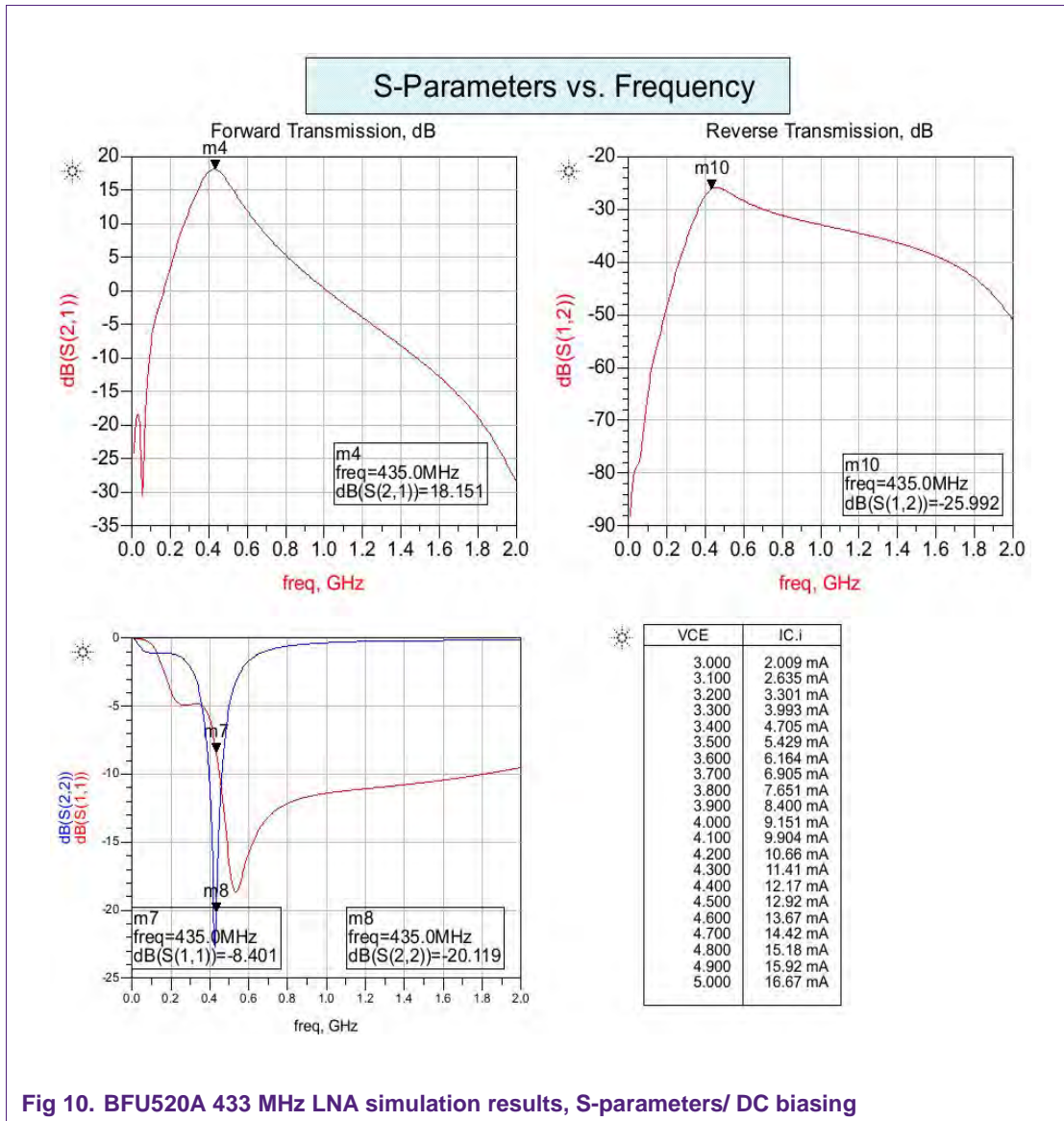


Fig 10. BFU520A 435 MHz LNA simulation results, S-parameters/ DC biasing

S-parameters at 3.6 Volt.



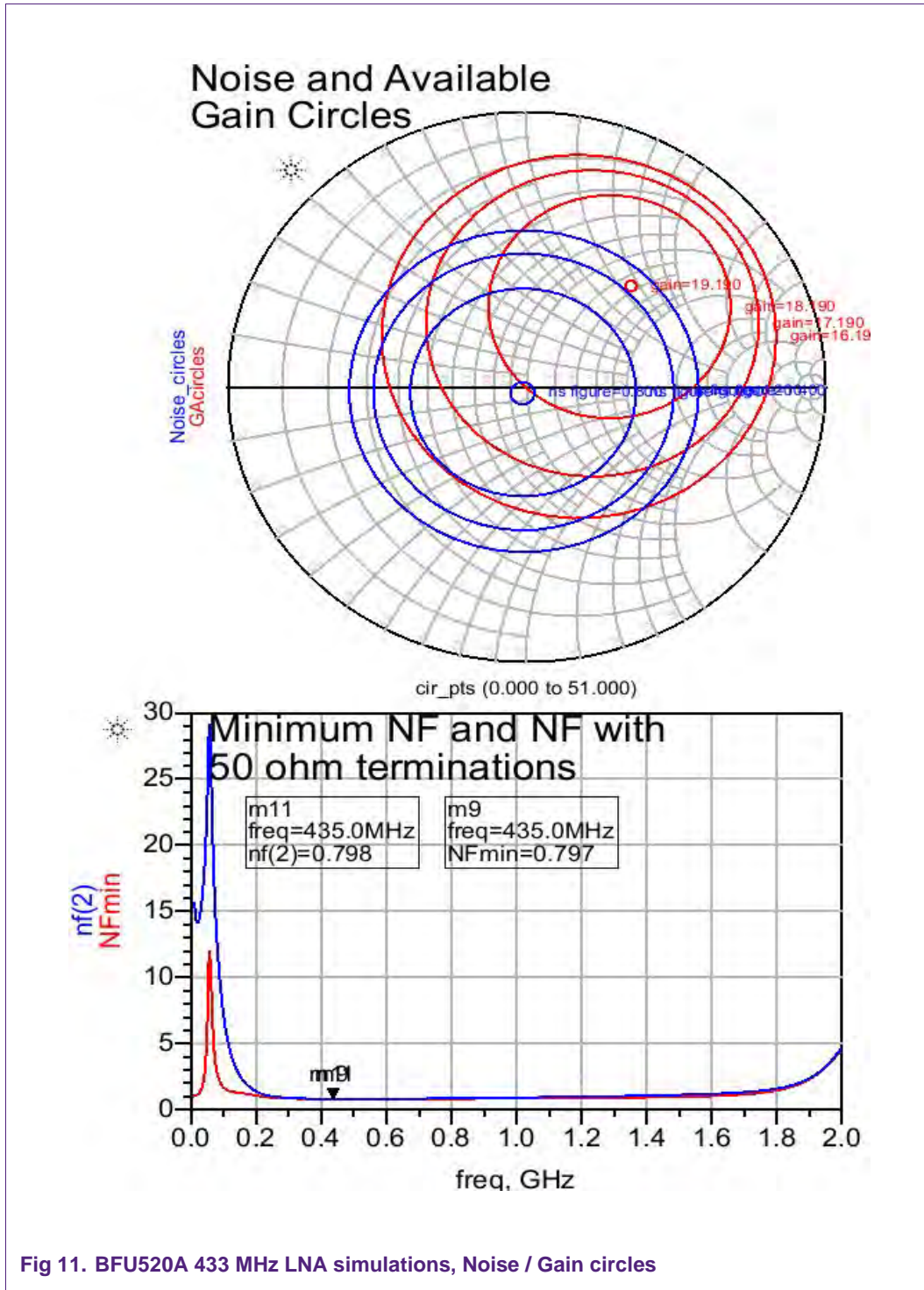


Fig 11. BFU520A 433 MHz LNA simulations, Noise / Gain circles

Compared to the noise circles of the unmatched circuit (section 5.5), we can clearly see the optimum noise point has moved towards the ideal 50R point.

## 6. Application circuit

The circuit diagram of the evaluation board is shown in Fig 12 PCB schematic.

### 6.1 BFU520A 433 MHz ISM LNA schematic

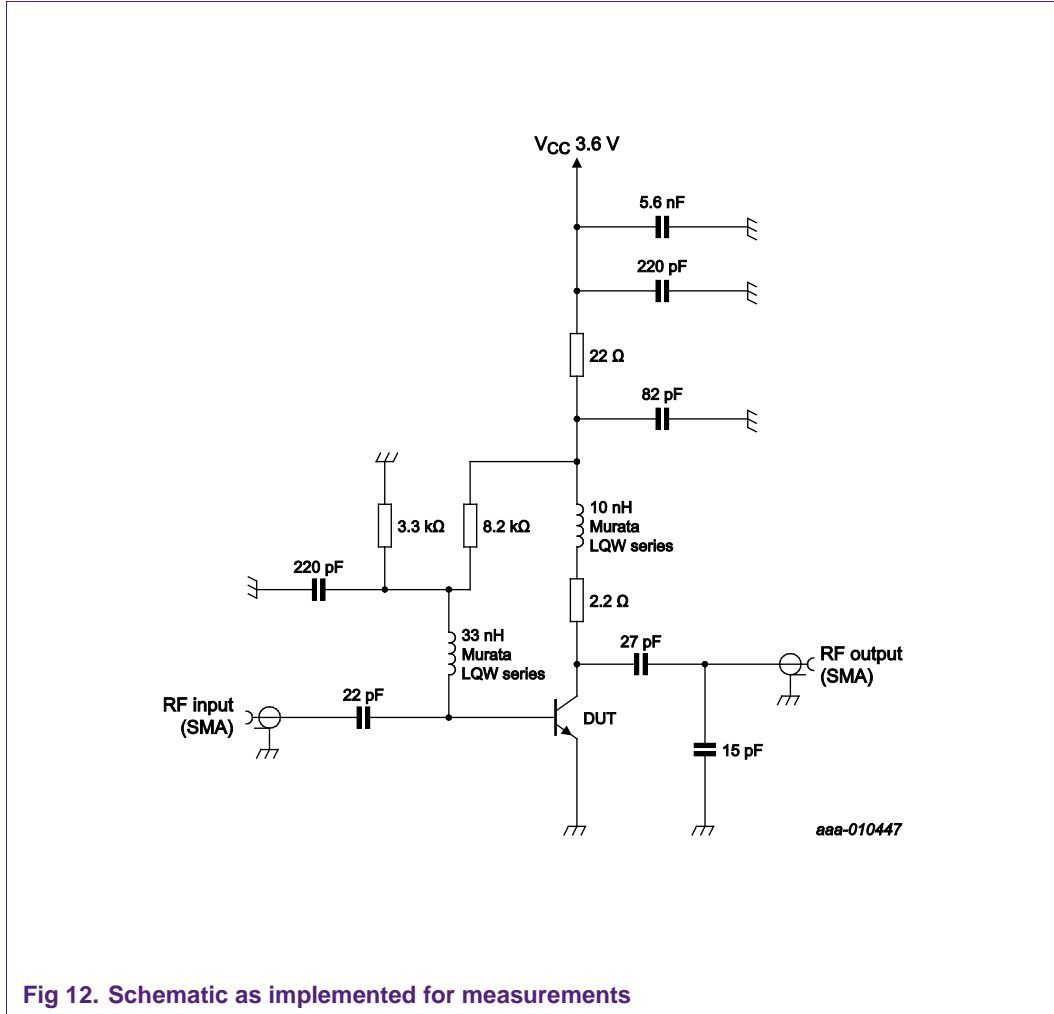


Fig 12. Schematic as implemented for measurements

The PCB layout used for our internal evaluations did not accommodate the 33nH inductor to be in the bias path (as shown in the ADS schematics) the input matching inductor was placed to ground (GND) and an additional DC blocking capacitor (220pF) was used. This should give equal results and a slight improvement on the Noise Figure can be expected as the resistive noise from the two bias resistors is not suppressed by a blocking capacitor to GND.

6.2 BFU520A 433 MHz ISM LNA PCB drawing

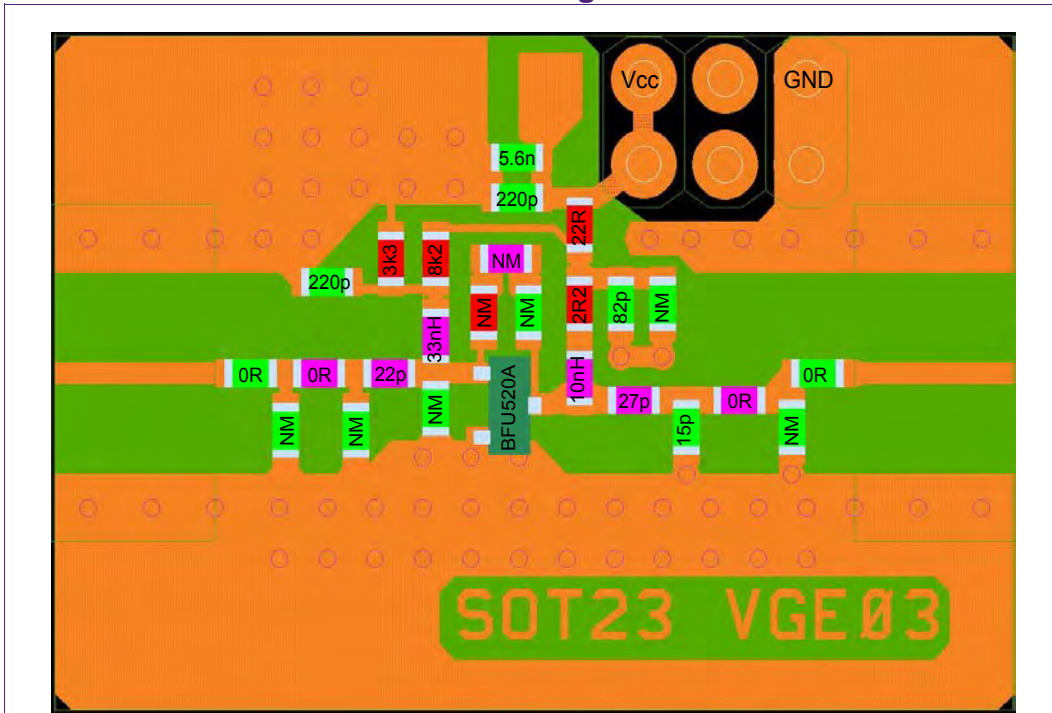


Fig 13. PCB implementation for measurements

Remarks:

0R = SMD jumper

NM = component not mounted.

This layout, as delivered with the Starter kit, accommodates the possibility to implement the biasing as shown in the ADS schematics.

6.3 PCB properties, layer stack



Fig 14. PCB layers used for Evaluation Boards in Starter kit



## 6.1 Typical LNA evaluation board results

**Table 2. Typical results measured on the evaluation boards**

*Operating Frequency is  $f = 433$  MHz unless otherwise specified; Temp = 25 °C*

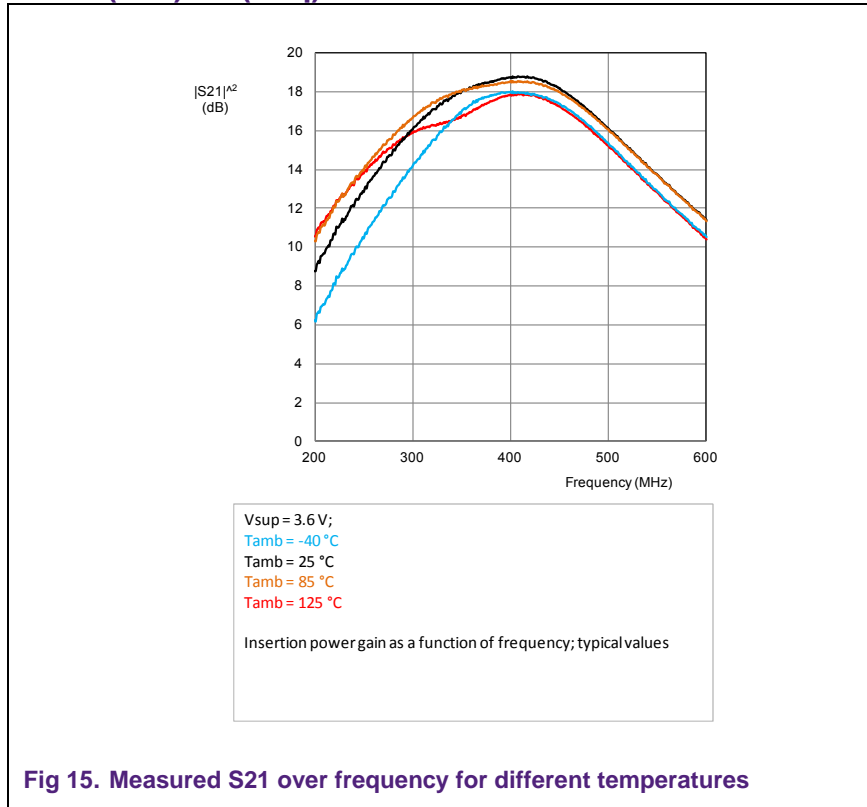
Parameter	Symbol	EVB	Unit	Remarks
Supply Voltage	$V_{CC}$	3.6	V	
Supply Current	$I_{CC}$	7	mA	
Noise Figure	NF	1	dB	
Power Gain	$G_p$	19	dB	
Input Return Loss	$RL_{in}$	-8	dB	
Output Return Loss	$RL_{out}$	-12	dB	
Output third order intercept point	OIP3	11	dBm	

**Table 3. Bill Of Materials**

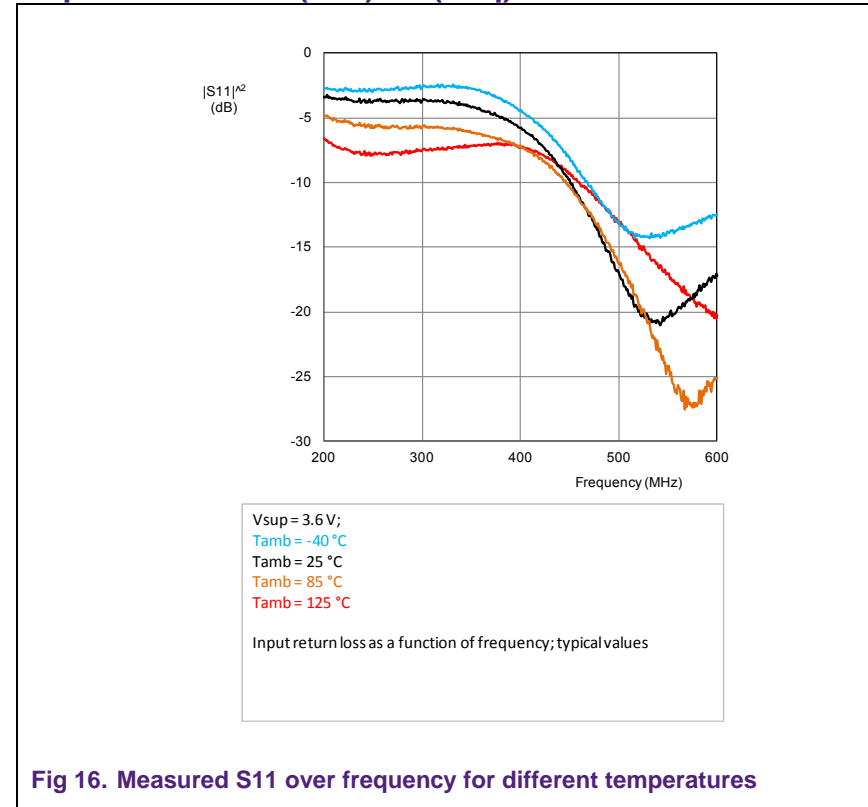
Value	Description	Footprint	Manufacturer
BFU520A	Transistor	SOT23	NXP Semiconductors
15 pF	Capacitor	0603	Various
22 pF	Capacitor	0603	Various
27 pF	Capacitor	0603	Various
82 pF	Capacitor	0603	Various
220 pF	Capacitor	0603	Various
220 pF	Capacitor	0603	Various
5.6 nF	Capacitor	0603	Various
2.2 $\Omega$	Resistor	0603	Various
22 $\Omega$	Resistor	0603	Various
3.3 k $\Omega$	Resistor	0603	Various
8.2 k $\Omega$	Resistor	0603	Various
10 nH	Inductor	0603	Murata LQW18A
33 nH	Inductor	0603	Murata LQW18A

7. Characterization of LNA over temperature and supply voltage

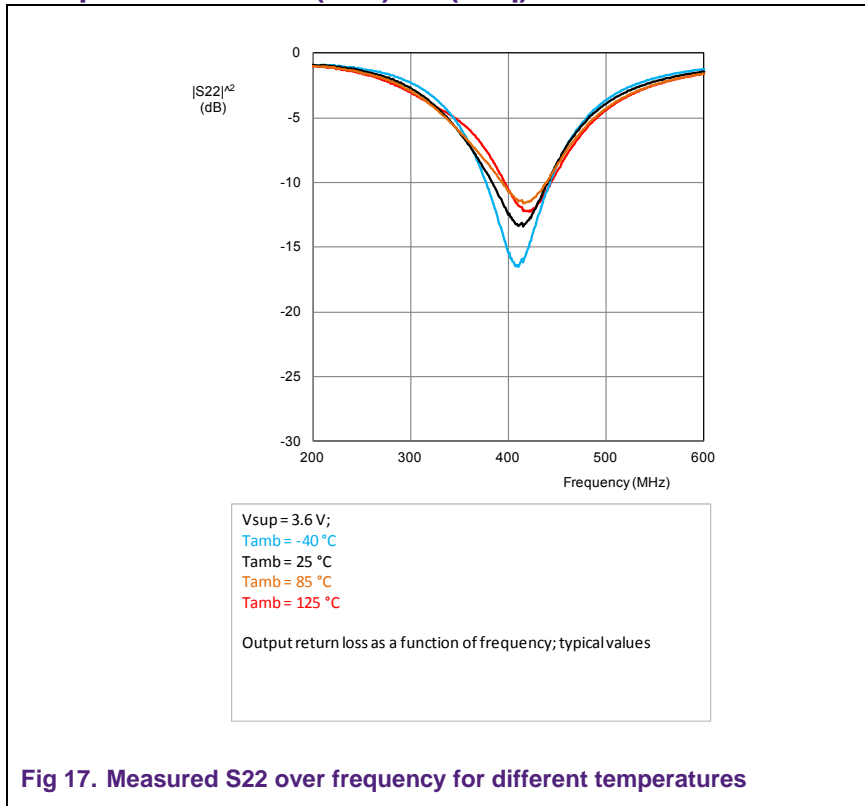
7.1 Gain (S21) = f (freq)



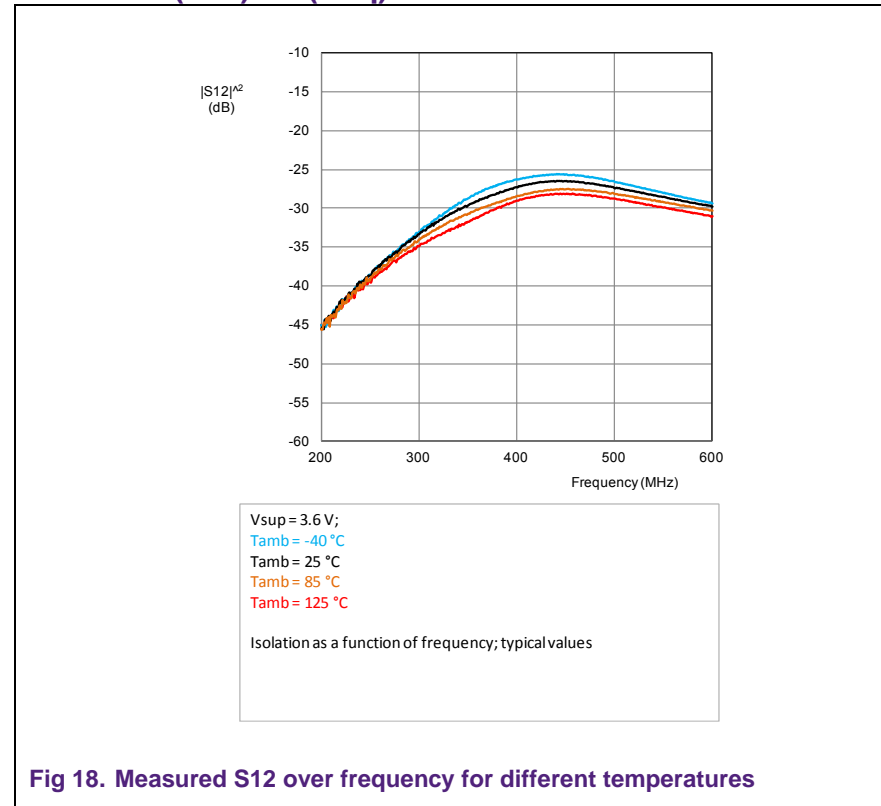
7.2 Input return-loss (S11) = f (freq)



### 7.3 Output return-loss (S22) = f (freq)



### 7.4 Isolation (S12) = f (freq)



7.5 Output third-order intercept point (OIP3) = f (Tamb)

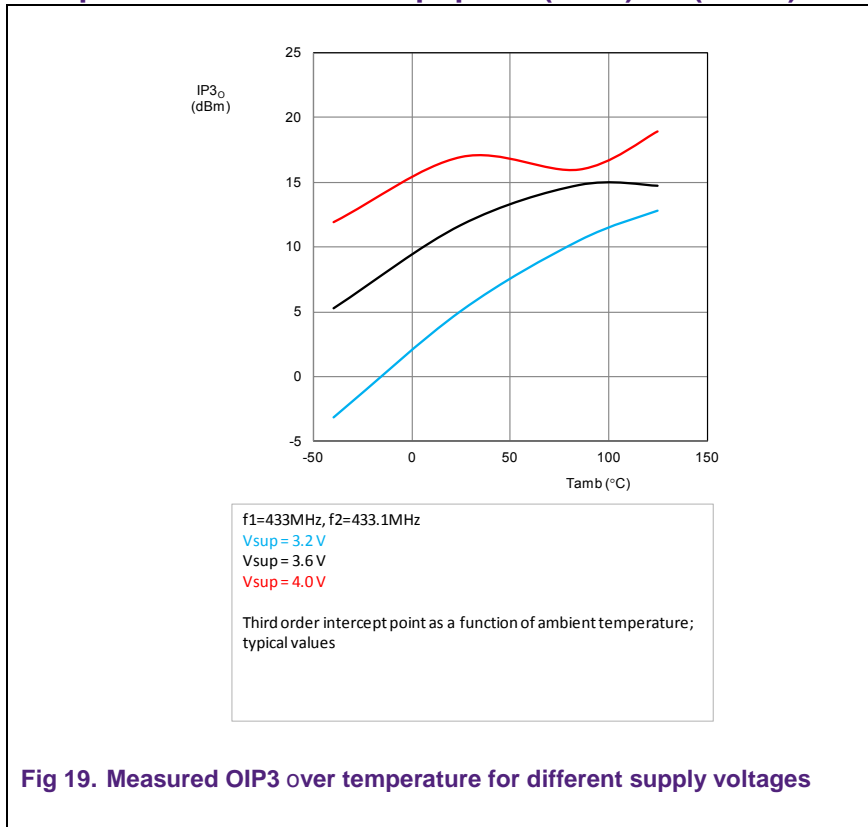


Fig 19. Measured OIP3 over temperature for different supply voltages

7.6 Output Power at 1 dB compression (P1dB) = f (Tamb)

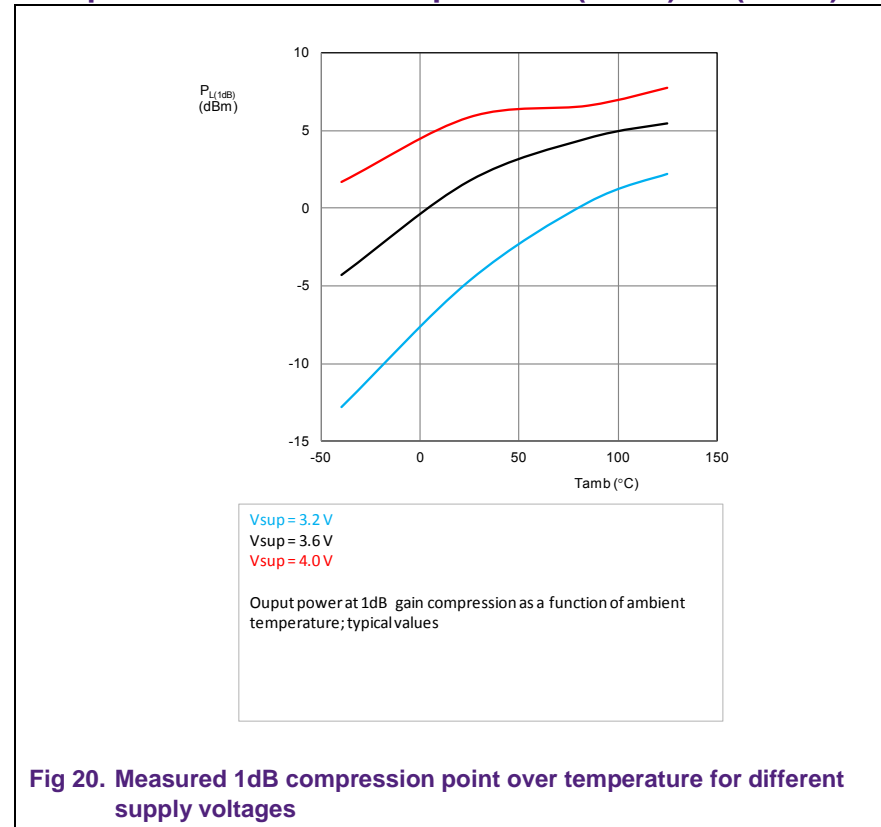
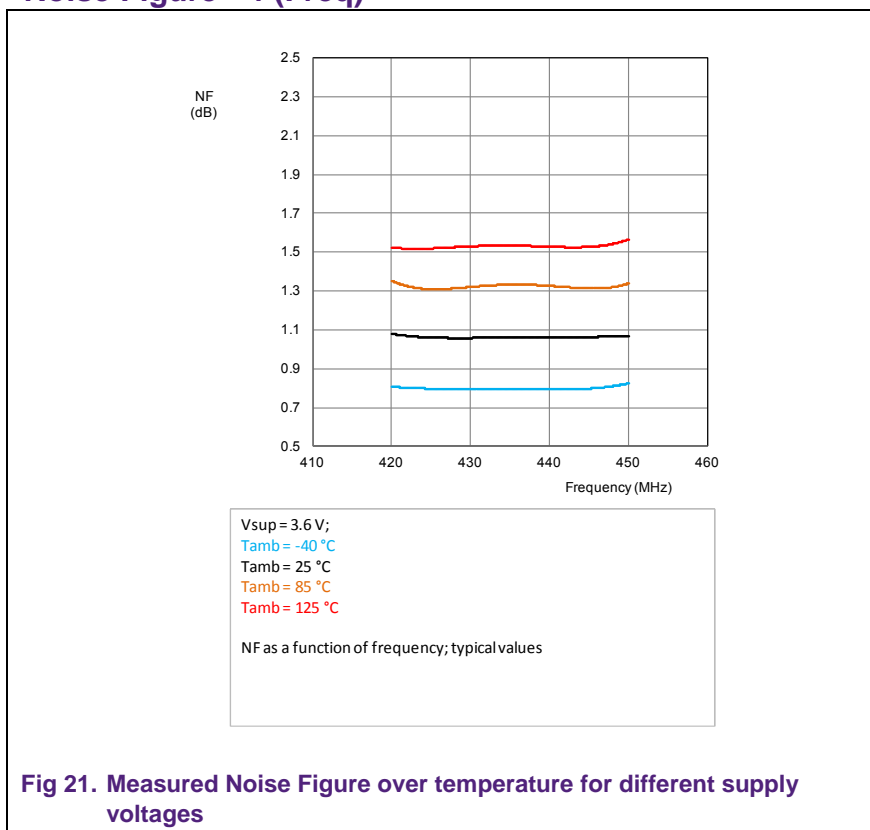


Fig 20. Measured 1dB compression point over temperature for different supply voltages

7.7 Noise Figure = f (Freq)



## 8. Conclusions / recommendations

With BFU520A a ISM 433 MHz LNA design with NF close to 1.2dB can be implemented, for this the input return loss has to be compromised. The circuit can be used as a base for derivative designs, matching to other frequencies can be done by tuning relevant capacitors and inductors.

For improvements on linearity it could be recommended to increase the DC biasing current and increase values for decoupling capacitors to GND, for example on the biasing network in case the matching inductor is in the configuration as shown in the ADS schematics.

	BFU520 series	BFU530 series	BFU550 series
Lowest Noise at low supply current	x		
Low Noise and medium Linearity		x	
Low Noise and high Linearity, high Icc			x

### 8.1 Tuning the design for other frequencies

This LNA can be tuned to other frequencies as well. The presented configuration has been designed for a low bandwidth application (Center frequency/required bandwidth = approx 10-100 depending on the used components).

The LNA can be tuned to other frequencies following section 5.4 till 5.6. The use of printed inductors or micro-strip elements is recommended above 1GHz to prevent gain drop.

For wideband amplifiers a feedback is recommended which can be implemented on the existing board.

A reference design for a wideband amplifier, applying feedback, is planned to be issued. Please regularly visit the NXP PIP pages to monitor availability of BFU5- series related AN's.

## 9. References

BFU520A datasheet

BFU5xxA starter-kit (OM7961) User Manual, UM10772

## 10. Legal information

### 10.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 10.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

### 10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.



## 11. List of figures

---

Fig 1.	BFU5xxA evaluation boards.....	4
Fig 2.	Circuitry to set DC bias current .....	6
Fig 3.	ADS design template for output stage design ...	7
Fig 4.	ADS simulation results for transistor + bias + output match .....	8
Fig 5.	ADS simulation results for stability ( $\mu$ -factor) ....	8
Fig 6.	BFU520A Noise and Gain circles at 433 MHz...9	
Fig 7.	ADS simulation template for input matching....	10
Fig 8.	ADS simulation results for source matching....	10
Fig 9.	BFU520A 433 MHz LNA simulation .....	11
Fig 10.	BFU520A 433 MHz LNA simulation results, S-parameters/ DC biasing .....	12
Fig 11.	BFU520A 433 MHz LNA simulations, Noise / Gain circles .....	13
Fig 12.	Schematic as implemented for measurements	14
Fig 13.	PCB implementation for measurements.....	15
Fig 14.	PCB layers used for Evaluation Boards in Starter kit .....	15
Fig 15.	Measured S21 over frequency for different temperatures .....	17
Fig 16.	Measured S11 over frequency for different temperatures .....	17
Fig 17.	Measured S22 over frequency for different temperatures .....	18
Fig 18.	Measured S12 over frequency for different temperatures .....	18
Fig 19.	Measured OIP3 over temperature for different supply voltages .....	19
Fig 20.	Measured 1dB compression point over temperature for different supply voltages .....	19
Fig 21.	Measured Noise Figure over temperature for different supply voltages .....	20

12. List of tables

Table 1. Customer evaluation kits .....3  
Table 2. Typical results measured on the evaluation boards  
..... 16  
Table 3. Bill Of Materials ..... 16

## 13. Contents

---

1.	<b>Abstract</b> .....	3
2.	<b>Introduction</b> .....	3
3.	<b>Requirements</b> .....	4
4.	<b>Design considerations</b> .....	4
5.	<b>Design approach</b> .....	5
5.1	Simulation steps .....	5
5.2	Implementation / evaluation steps .....	5
5.3	Setting up the DC bias circuit .....	6
5.4	Definition of collector load and output match.....	7
5.5	Definition of input / source matching circuit .....	9
5.6	Overall LNA simulation .....	11
6.	<b>Application circuit</b> .....	14
6.1	BFU520A 433 MHz ISM LNA schematic .....	14
6.2	BFU520A 433 MHz ISM LNA PCB drawing .....	15
6.3	PCB properties, layer stack .....	15
6.1	Typical LNA evaluation board results .....	16
7.	<b>Characterization of LNA over temperature and supply voltage</b> .....	17
7.1	Gain ( $S_{21}$ ) = f (freq) .....	17
7.2	Input return-loss ( $S_{11}$ ) = f (freq) .....	17
7.3	Output return-loss ( $S_{22}$ ) = f (freq) .....	18
7.4	Isolation ( $S_{12}$ ) = f (freq).....	18
7.5	Output third-order intercept point (OIP3) = f ( $T_{amb}$ ) .....	19
7.6	Output Power at 1 dB compression (P1dB) = f ( $T_{amb}$ ).....	19
7.7	Noise Figure = f (Freq) .....	20
8.	<b>Conclusions / recommendations</b> .....	21
8.1	Tuning the design for other frequencies .....	21
9.	<b>References</b> .....	21
10.	<b>Legal information</b> .....	22
10.1	Definitions.....	22
10.2	Disclaimers.....	22
10.3	Trademarks .....	22
11.	<b>List of figures</b> .....	23
12.	<b>List of tables</b> .....	24
13.	<b>Contents</b> .....	25

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.

---

© NXP B.V. 2014.

All rights reserved.

For more information, visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 20 January 2014

Document identifier: AN11377