AN11397

PTN3363/65/66 PCB layout guidelines

Rev. 3 — 25 April 2017 Application note

Document information

Information	Content
Keywords	DisplayPort, HDMI, PTN3363/65/66, PCB, layout, signal integrity, symmetry, loss, jitter
Abstract	This document provides a practical guideline for incorporating the level shifter ICs layout into PCB designs.

Revision history

Rev	Date	Description
v.3	20170425	Modifications: • Added PTN3365 and PTN3366 device information
v.2	20140415	Modifications: • Application note corrected by removing type number PTN3366
v.1	20131003	Initial version

1 Introduction

PTN3363/65/66 are high-speed active HDMI/DVI level shifters that convert four low-swing AC-coupled differential inputs to DVI version 1.0 and HDMI version 1.4b compliant differential output signals, up to 3.4 Gbit/s per lane to support 36-bit deep color, 4K × 2K video format or 3D data transport. PTN3363/66 are low power (72 mW typ), while PTN3365 consumes 230 mW typ.

To support HDMI speeds up to 3.0 Gbit/s (PTN3365/66) or 3.4 Gbit/s (PTN3363), some strict layout considerations must be followed to reduce signal impairments such as reflection due to impedance mismatch, crosstalk, high frequency noises, timing jitters.

2 HDMI interface PCB layout

2.1 Bypass capacitors

Bypass capacitors are placed between the power pin and ground to shunt the high-frequency noise to ground. A real capacitor always behaves as a resonant circuit due to the inherent manufactured parasitic inductance and resistance, as well as the inductance of the trace between the capacitor and the power pin.

Below the resonant frequency the capacitor behaves as a low AC impedance to reduce high-frequency noise, but above the resonant frequency the inductance characteristic dominates and the capacitor impedance increases with frequency. This behavior couples high-frequency noise into the power pin rather than reducing the high frequency noise.

2.1.1 Bypass capacitors layout guidelines

- 0402 size bypass capacitors referred to reduce the inheritance parasitic inductance and resistance.
- Single capacitor is referred over capacitor array to reduce crosstalk.
- To reduce the trace inductance and to increase the resonant frequency, place the bypass capacitor as close as possible to the power pin.
- Connect the pads of the capacitor with vias directly to the ground plane and power plane, then connect the capacitor to the power and ground pins with wide traces.

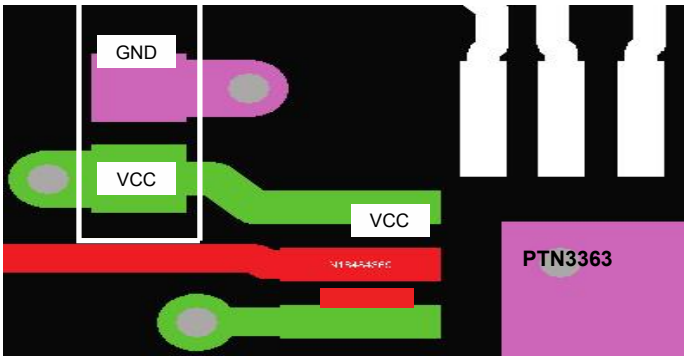

Figure 1. Bypass capacitor routing

2.2 Device center pad

Ground pins are not available on the PTN3363/65/66. Instead, the supply ground is connected to the exposed center pad of the package. Therefore, the exposed center pad must be connected to the supply ground for proper device operation. For enhanced thermal, electrical, and board level performance the exposed center pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

During reflow soldering, solder paste melts and gas or trapped air is released causing spattering or solder balling. If the solder paste is printed as a number of individual dots instead of one large deposit, solder balling and splatter can be minimized.

The solder paste pattern area should cover 35% of the solder land area. When printing solder paste on the exposed center pad, the solder paste dot area should not cover more than 20% of the solder land area. Furthermore, the paste should be printed away from the solder pad edges.

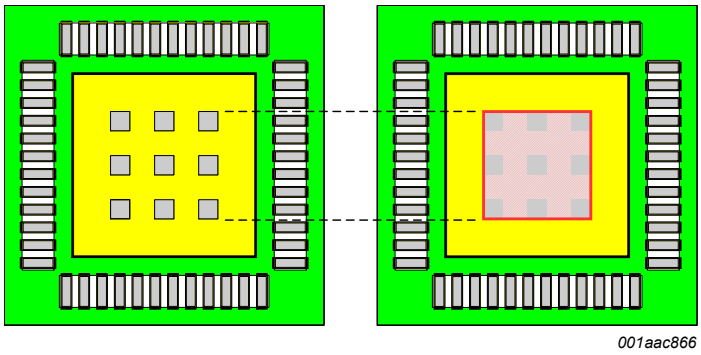

Figure 2. Paste deposit (left) and paste pattern area (right)

2.3 PCB trace impedance

If the differential trace impedance from the PTN3363/65/66 (to the HDMI connector) and the HDMI connector impedance are closely matched to 100Ω, then there would be minimal signal reflection off the HDMI connector. But if the HDMI connector impedance and the trace impedance from the PTN3363/65/66 are not closely matched, then there would be reflections between the connector and the output of the PTN3363/65/66. These reflections cause overshoot and undershoot, preventing the differential output signal to reach the full swing level, reducing the eye high, and prolong the rise and fall times.

Figure 3 shows a simulation case where PTN3363 is used to drive a 100Ω load with 80Ω and 90Ω PCB traces to connect PTN3363 to the load. The blue trace in the figure shows the signal captured at the 100Ω HDMI connector when the PCB trace has 80Ω characteristic impedance. The red trace in the figure shows the signal captured at the 100Ω HDMI connector when the PCB trace has 90Ω characteristic impedance.

In both cases, the signal at the 100Ω load does not reach 1 V differential swing, but clearly the blue trace is 100 mV lower in amplitude than the red trace.

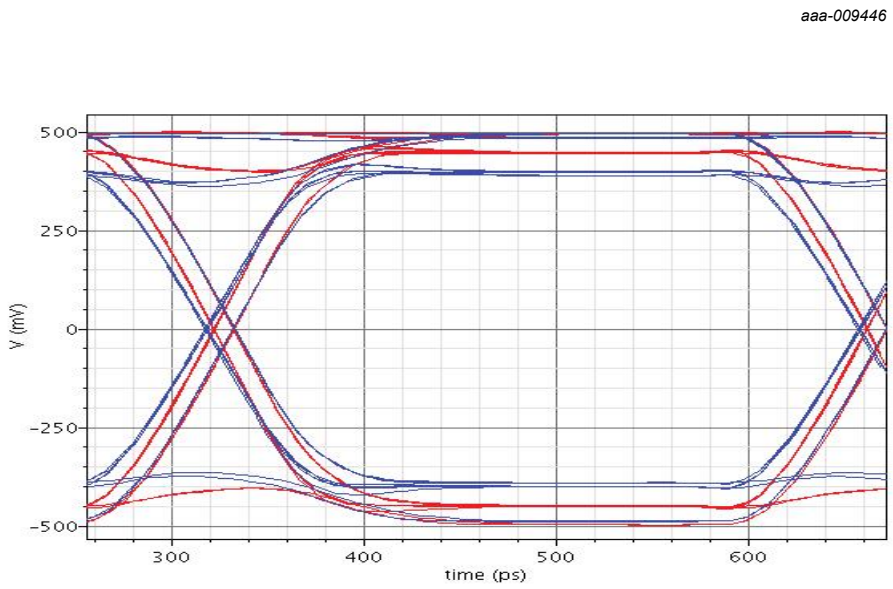

Figure 3. PCB trace impedance mismatch with HDMI

2.4 Internal layer routing

When internal routing is done, blind via or imbedded via must be used to eliminate via stub.

If standard vias are used, then the signals must be routed on the signal layer just above the layer where the vias are ended to reduce the length of the stub. In Figure 4, the signal must be routed on Layer 3 instead of Layer 2.

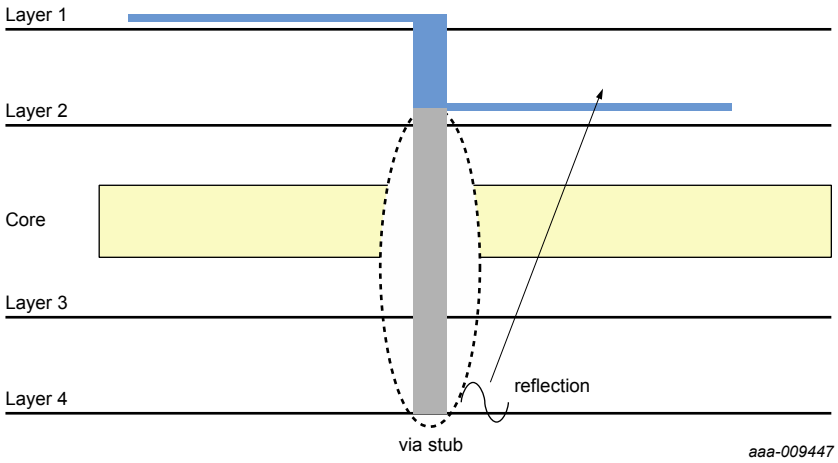

Figure 4. Reflection caused by via

Via creates discontinuity of PCB traces. At the discontinuity, the trace impedance is lowered. Widening the distance between the barrel and the ground plane can lower the capacitance between the via and the ground plane, therefore, increases the trace impedance.

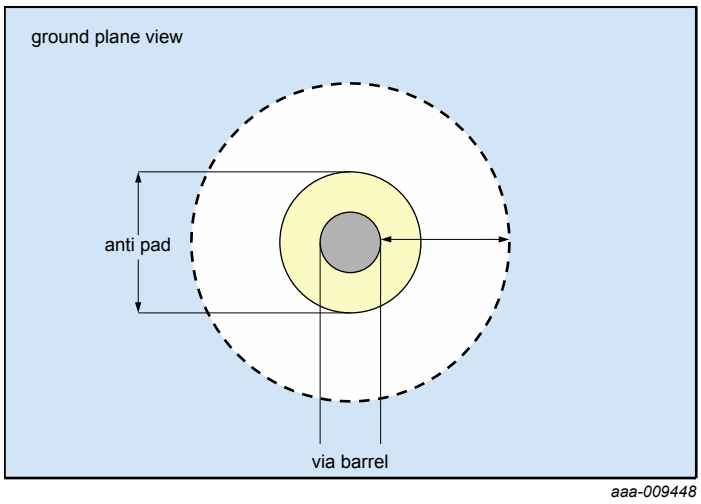

Figure 5. Via layout on ground plane

Another issue with via is current loop — large loop current can create EMI problem and might induce crosstalk to nearby circuit. Once the current goes through the via, the current return path might be diverted a long way before it returns to the source. The designer has to make sure that the return current always flows directly under the signal trace to keep the current loop minimal. A good way to make sure that the return current flow directly under the signal trace is to add a ground via next to the signal via. For differential traces, there would be two ground vias — one next to each signal via.

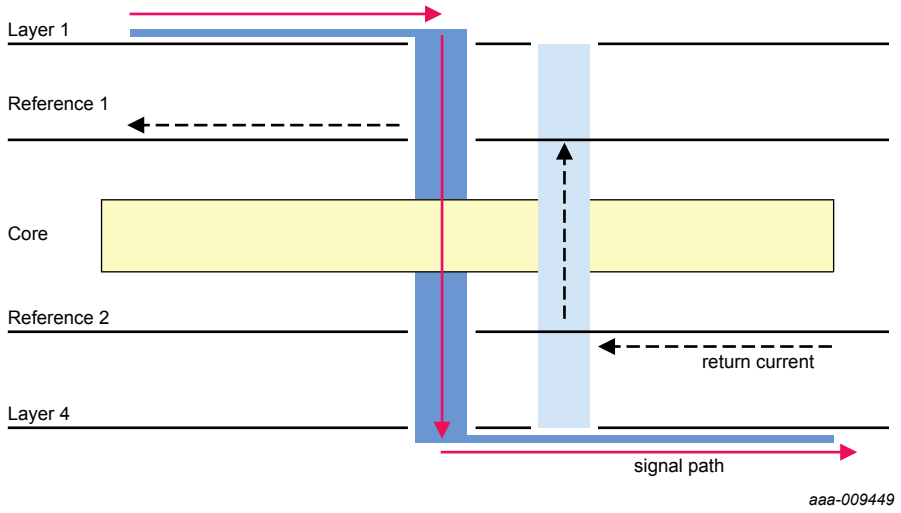

Figure 6. Ground via reduces current loop

2.5 Crosstalk

Decreasing the coupling of the intra-pair differential signals and increasing the spacing to neighboring signals help to minimize harmful crosstalk impacts and electromagnetic interference (EMI) effects. In the microstrip case, two differential traces should be routed as a pair as close together as possible, and air gap spacing between this differential pair to the neighboring pair should be as wide as possible.

The spacing (D) between pairs and to all other signals should be at least four times the dielectric height (h). If the other signals have significantly higher voltage levels or edge rate than the differential signal, the space should increase to 30 mil to avoid coupling.

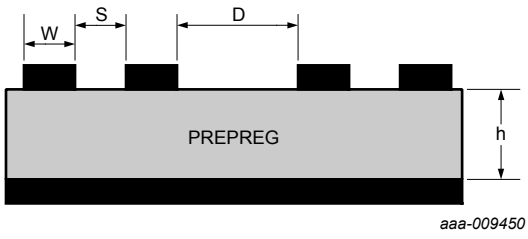

Figure 7. Differential pair-to-pair spacing

2.6 HDMI surface mount connector

Surface mount HDMI connector pads have the tendency to reduce the trace impedance due to their rather long and wide geometry. These surface mount pads create an impedance discontinuity along the signal path, and the effect of this discontinuity appears as excess capacitance because the surface mount pads act as parallel plates with the reference plane.

When surface mount HDMI connectors are used, the reference plane portion directly underneath these pads must be removed to reduce the excess capacitance. In Figure 8, the pads with colored rectangles around them are high-speed HDMI differential pads. The reference plane underneath these pads must be removed.

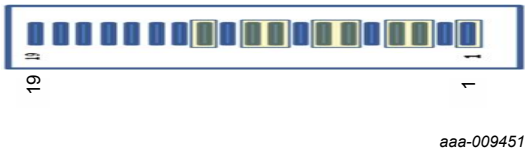

Figure 8. Surface mount pad ground plane

3 DisplayPort interface PCB layout

3.1 DC blocking capacitors

DC blocking capacitors are employed on the DisplayPort interface to isolate the DC bias between the source and the sink. Small capacitors such as 0402 are strongly recommended, as small solder pads have less of an impact on the trace impedance discontinuity. The large area of the solder pads acts as parallel plates with the reference plane directly underneath to create excess capacitance.

To remove this excess capacitance, the reference plan underneath these pads can be removed. Simulations (Altera Application Note 530, Reference [1]) shows that the optimal cutout for 0402 size capacitor is 25 mil wide. The impedance of this structure gives 95Ω differential. The impedance of the structure without the cut-off can be as low as 75Ω differential.

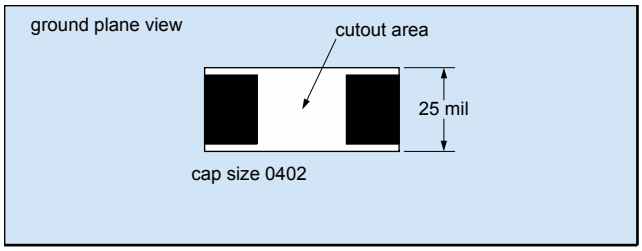

Figure 9. DC blocking capacitor ground plane cutout

Capacitor arrays are not recommended because of excessive crosstalk at high speed.

3.2 PCB trace

The differential trace impedance of DisplayPort signals is specified as 100Ω ± 20%. Ideally, the inter-connect channel (PCB traces, cable, etc.) between DP source and DP sink should also be 100Ω.

But in a high pin-count package, the routing channel gets used up very quickly, and becomes a limiting factor. To deal with this, silicon manufacturers use 85Ω packages and recommend PCB traces to be routed with 85Ω. There are benefits when reducing the system impedance to 85Ω:

- Reduced board thickness — lower cost
- Reduced trace spacing — more routing space
- Increased trace width — lower trace loss

Intel motherboard PCB design guideline requests 85Ω differential impedance for DisplayPort signals. When PTN3363/65/66 is used in such a platform, the differential signals between the GPU and the PTN3363/65/66 should be routed as 85Ω differential.

4 PTN3363/65/66 pinout comparison

PTN3363/65/66 are all in HVQFN32 package, with similar pinouts. The differences are in pins 3, 23, 24. Their pinouts are shown side by side below for easy comparison.

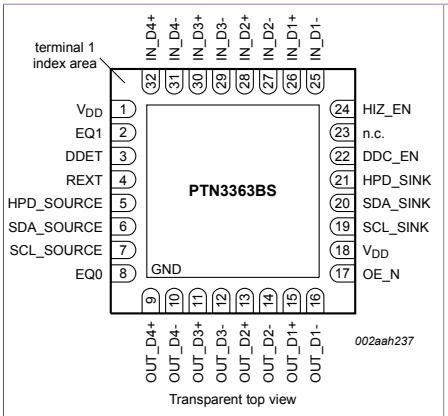

Figure 10. PTN3363 pinout

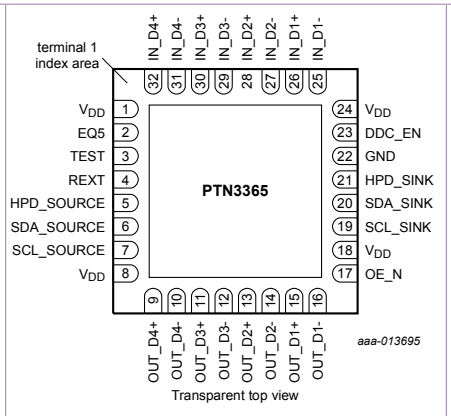

Figure 11. PTN3365 pinout

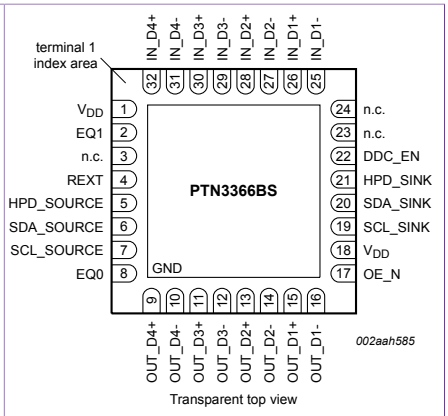

Figure 12. PTN3366 pinout

5 HDMI layout example

PCB has 4-layers, the stack up is shown in Figure 13:

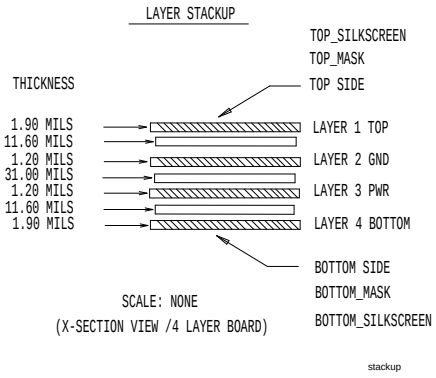

Figure 13. Layer stackup

Impedance details: All 20 mil traces require 50Ω,+/-10% single ended impedance on top & bottom layers. All 8.5/6.6/8.5 traces require 100Ω,+/-10% differential impedance on top layers.

An HDMI layout example is shown in Figure 14.

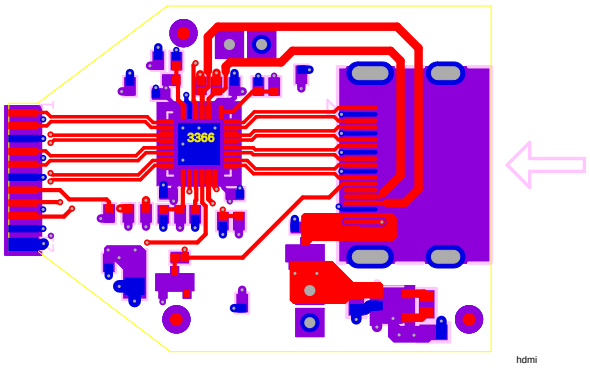

Figure 14. HDMI layout example

6 Summary

PTN3363 supports HDMI speeds up to 3.4 Gbit/s, PTN3365/66 supports HDMI speeds up to 3.0 Gbit/s. The high data rate requires strict layout implementation. If these guidelines are followed, the pronounced effect of impedance discontinuity on high-speed serial signals can be minimized.

7 Abbreviations

Table 1. Abbreviations

Acronym	Description
DP	DisplayPort
DVI	Digital Visual Interface
EMI	ElectroMagnetic Interference
GPU	Graphics Processor Unit
HDMI	High Definition Media Interface
IC	Integrated Circuit
PCB	Printed-Circuit Board

8 References

[1] Altera Application Note 530, May 2008, version 1.0

[2] Calpella platform design guide, Rev.0.8, Aug. 2008

[3] DisplayPort Standard, Version 1.1

[4] NXP AN10373, “PCI Express PHY PCB Layout Guideline”, Rev.01

9 Legal information

9.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

9.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Tables

Tab. 1. Abbreviations 10

Figures

Fig. 1. Bypass capacitor routing 4
Fig. 2. Paste deposit (left) and paste pattern area (right) 4
Fig. 3. PCB trace impedance mismatch with HDMI 5
Fig. 4. Reflection caused by via 6
Fig. 5. Via layout on ground plane 6
Fig. 6. Ground via reduces current loop 7
Fig. 7. Differential pair-to-pair spacing 7
Fig. 8. Surface mount pad ground plane 8
Fig. 9. DC blocking capacitor ground plane cutout 8
Fig. 10. PTN3363 pinout 9
Fig. 11. PTN3365 pinout 9
Fig. 12. PTN3366 pinout 9
Fig. 13. Layer stackup 9
Fig. 14. HDMI layout example 10

Contents

1 Introduction 3
2 HDMI interface PCB layout 3
2.1 Bypass capacitors 3
2.1.1 Bypass capacitors layout guidelines 3
2.2 Device center pad 4
2.3 PCB trace impedance 5
2.4 Internal layer routing 5
2.5 Crosstalk 7
2.6 HDMI surface mount connector 7
3 DisplayPort interface PCB layout 8
3.1 DC blocking capacitors 8
3.2 PCB trace 8
4 PTN3363/65/66 pinout comparison 9
5 HDMI layout example 9
6 Summary 10
7 Abbreviations 10
8 References 10
9 Legal information 11

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 April 2017
Document identifier: AN11397